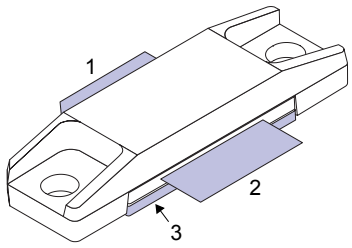
STAC0912-250

Datasheet

LDMOS avionics radar transistor



STAC780-2B

Features

Order code	Frequency	V_{DD}	P_{OUT}	Gain	Efficiency
STAC0912-250	960 to 1215 MHz	28 V	250 W	16 dB	58 %

- Excellent thermal stability
- Common source configuration
- P_{OUT} = 250W with 16 dB gain over 960 to 1215 MHz
- ST air-cavity STAC packaging technology

Applications

- Avionics

Description

The STAC0912-250 is a common source N-channel enhancement-mode lateral field-effect RF power transistor designed for avionics applications at frequencies range 960 to 1215 MHz.

Pin connection	
Pin	**Connection**
1	Drain
2	Gate
3	Source (bottom side)

Product status link
STAC0912-250

Product summary	
Order code	STAC0912-250
Marking	0912-250
Package	STAC780-2B
Packing	Tube
Base/bulk quantity	15/90

1 Electrical data

1.1 Maximum ratings

Table 1. Absolute maximum ratings (T_{CASE}= 25 °C)

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-source voltage	80	V
V_{GS}	Gate-source voltage	±20	V
P_{DISS}	Power dissipation (at T_{CASE} = +70 °C)	928	W
T_J	Maximum operating junction temperature	+200	°C
T_{STG}	Storage temperature range	-65 to +150	°C

1.2 Thermal data

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Junction-case thermal resistance	0.14	°C/W

Note: Thermal data at 100 µs - 10%

1.3 ESD protection characteristics

Table 3. ESD protection

Symbol	Test methodology	Class
HBM	Human body model (per JESD22-A114)	2

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

2.1 Static

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_{DS} = 10 mA	80			V
I_{DSS}	Zero gate voltage drain leakage current	V_{GS} = 0 V, V_{DS} = 28 V			2	µA
I_{GSS}	Gate-source leakage current	V_{GS} = 15 V, V_{DS} = 0 V			1	µA
$V_{GS(Q)}$	Gate quiescent voltage	V_{DS} = 28 V, I_{DS} = 150 mA	2.0		5.0	V
$V_{DS(on)}$	Drain-source on voltage	V_{GS} = 10 V, I_{DS} = 6 A		550	600	mV
G_{FS}	Forward transconductance	V_{DS} = 10 V, I_{DS} = 6 A	2.5			S

2.2 Dynamic

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f	Frequency		960		1215	MHz
P_{OUT}	Output power	P_{IN} = 12 W	250	285		W
G_{PS}	Power gain	P_{OUT} = 250 W	14	16.3		dB
ηD	Drain efficiency	P_{OUT} = 250 W	50	58		%
t_r	Rise time	P_{OUT} = 250 W			25	ns
t_f	Fall time	P_{OUT} = 250 W			10	ns
ΔG_{PS}	Gain variation	P_{OUT} = 250 W, gain droop within the pulse			0.2	dB
VSWR	Load mismatch	All phase angles at P_{OUT} = 250 W			10:1	

Note: V_{DD} = 36 V, I_{DQ} = 150 mA, pulse width = 100 µs, duty cycle = 10%.

Table 6. Reference data

Mode operat.	Pulse cond.	V_{DD} (V)	P_{OUT} (W)	Gain (dB)	Delta gain (dB)	Eff. (%)	Pulse droop (dB)	TR (ns)	TF (ns)	$R_{thj\text{-}case}$ (°C/W)
All modes	100 µs - 10%	36	250	16	0.7	58	0.1	25	5	0.14
TCAS 1030 to 1090 MHz	32 µs - 1%	36	250	16	0.3	57	0.1	25	5	0.06
Mode-S 1030 to 1090 MHz	128 µs - 2%	36	250	15.5	0.3	56	0.2	25	5	0.125
	340 µs - 1%	36	250	15.5	0.3	56	0.25	25	5	0.17

Note: Typical RF performance measured in common source class-AB broadband circuit 960 to 1215 MHz frequency band. Th = 25 °C; $R_{thj\text{-}case}$ = 0.15 °C/W; unless specified otherwise.

3 Impedance data

Figure 1. **Impedance data**

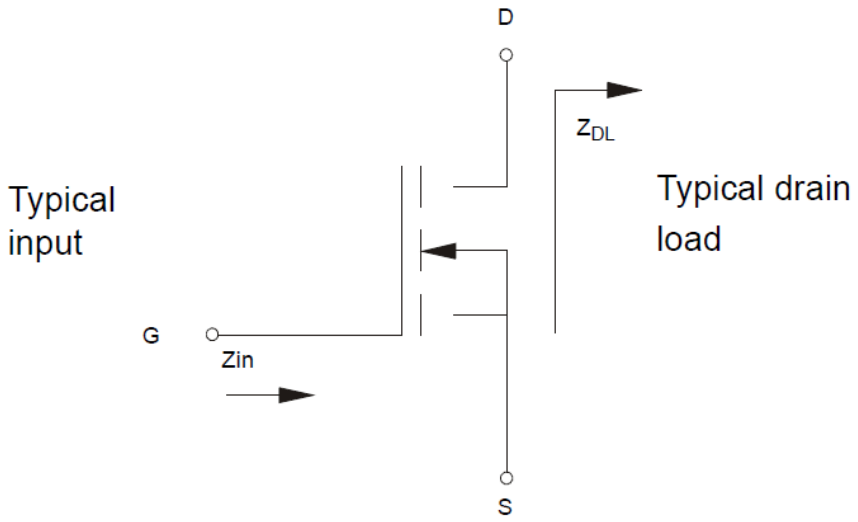


Table 7. **Impedance data**

Frequency (MHz)	Z_{source} (Ohm)	Z_{load} (Ohm)
960	2.437 - j2.029	1.865 - j2.469
1030	2.332 - j1.106	1.827 - j1.972
1090	2.278 - j0.369	1.765 - j1.643
1140	2.246 - j0.214	1.664 - j 1.413
1215	2.193 -j1.042	1.401 - j1.065

4 Typical performances

Figure 2. Gain vs output power

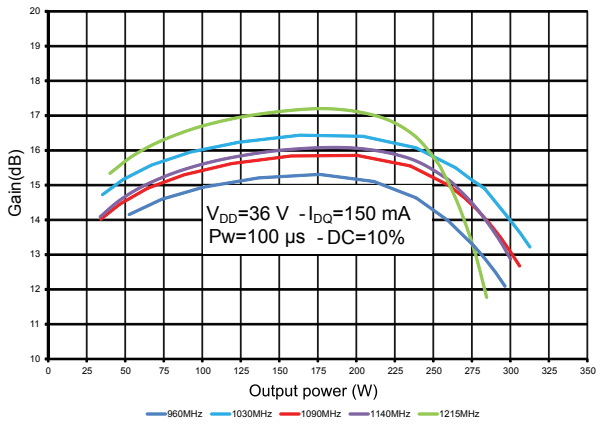


Figure 3. Efficiency vs output power

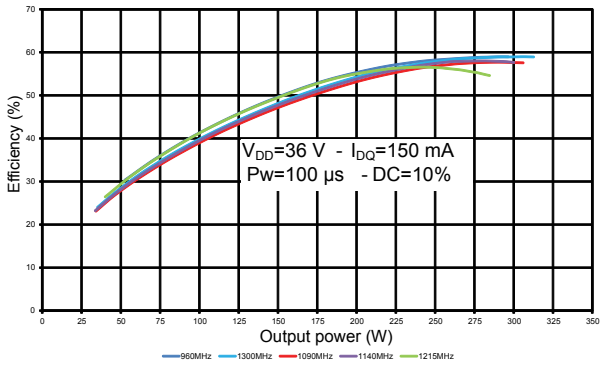
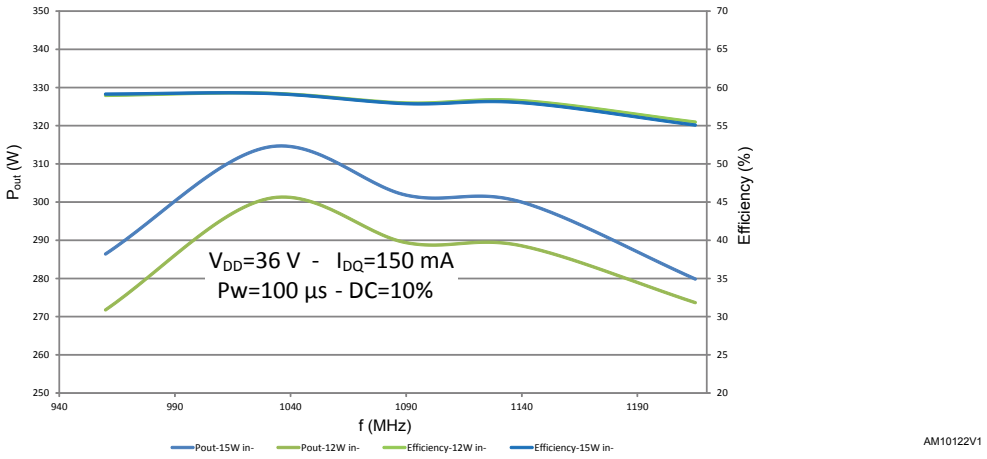


Figure 4. Output power and efficiency vs frequency



5 Test circuit

5.1 Electrical schematic and BOM

Figure 5. Electrical schematic

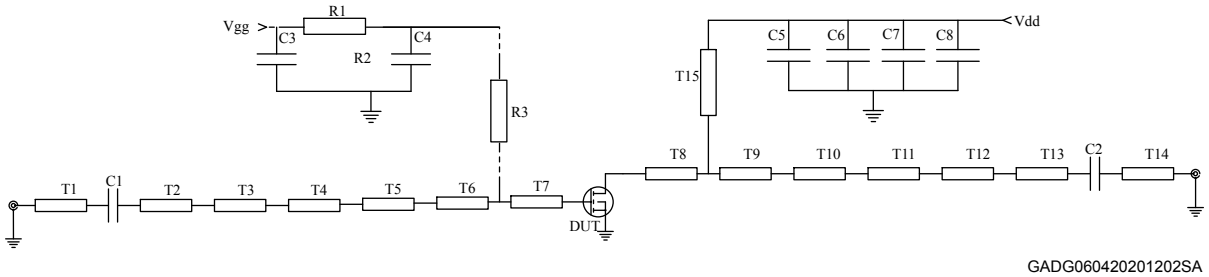


Table 8. Component list

Component	Qty	Part number	Vendor	Description, dimension (x,y)
C1, C16,C17,C18	4	1111C360G501X	Passive Plus Inc.	36 pF chip ceramic capacitor
C2	1	1111C2R2G501X	Passive Plus Inc.	2.2 pF chip ceramic capacitor
C3	1	1111C3R0G501X	Passive Plus Inc.	3.0 pF chip ceramic capacitor
C4, C5	2	1111C5R6G501X	Passive Plus Inc.	5.6 pF chip ceramic capacitor
C6, C9	2	1111C1R4G501X	Passive Plus Inc.	1.4 pF chip ceramic capacitor
C7, C10	2	1111C3R9G501X	Passive Plus Inc.	3.9 pF chip ceramic capacitor
C8, C11	2	1111C4R7G501X	Passive Plus Inc.	4.7 pF chip ceramic capacitor
C12, C13	2	1111C1R7G501X	Passive Plus Inc.	1.7 pF chip ceramic capacitor
C14, C15	2	1111C1R6G501X	Passive Plus Inc.	1.6 pF chip ceramic capacitor
C19	1	UPW1E331MPD	Nichicon	230 µF, 25 V electrolytic capacitor
C20	1	TVX1J102MCD	Nichicon	1000 µF, 63 V electrolytic capacitor
C21	1	TVA1346	Vishay Sprague	100 µF, 100 V electrolytic capacitor
R1	1	CR1206-4W-681JB	Venkel	390 Ω surface mount resistor
R2	1	CR1206-4W-821JB	Venkel	820 Ω surface mount resistor
L1	1	1606-9G	Coil Craft	9.85 nH air core inductor
T1				L= 0.278 in, W=0.082 in
T2				L= 0.134 in, W=0.082 in

Component	Qty	Part number	Vendor	Description, dimension (x,y)
T3				L= 0.736 in, W=0.748 in
T4				L= 0.674 in, W=0.748 in
T5				L= 0.100 in, W=0.082 in
T6				L= 0.365 in, W=0.082 in
T7				L= 1.160 in, W=0.082 in
Board 3X5	1		Rogers Corp	0.030 THK, Er=2.5, 2Oz Cu both sides

5.2 Test circuit layout

Figure 6. **Broadband 960-1215 MHz circuit**

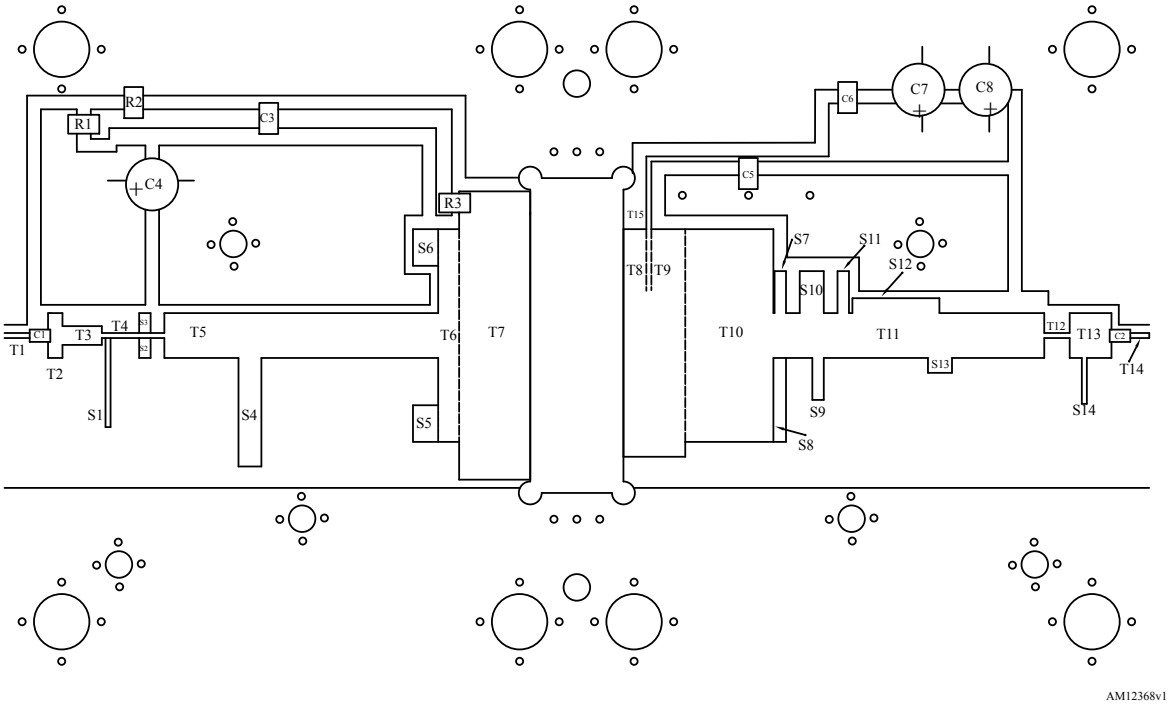
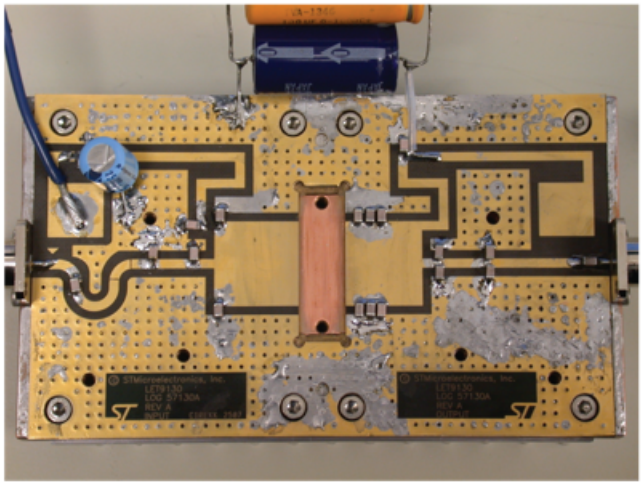


Figure 7. **Demonstration board picture**

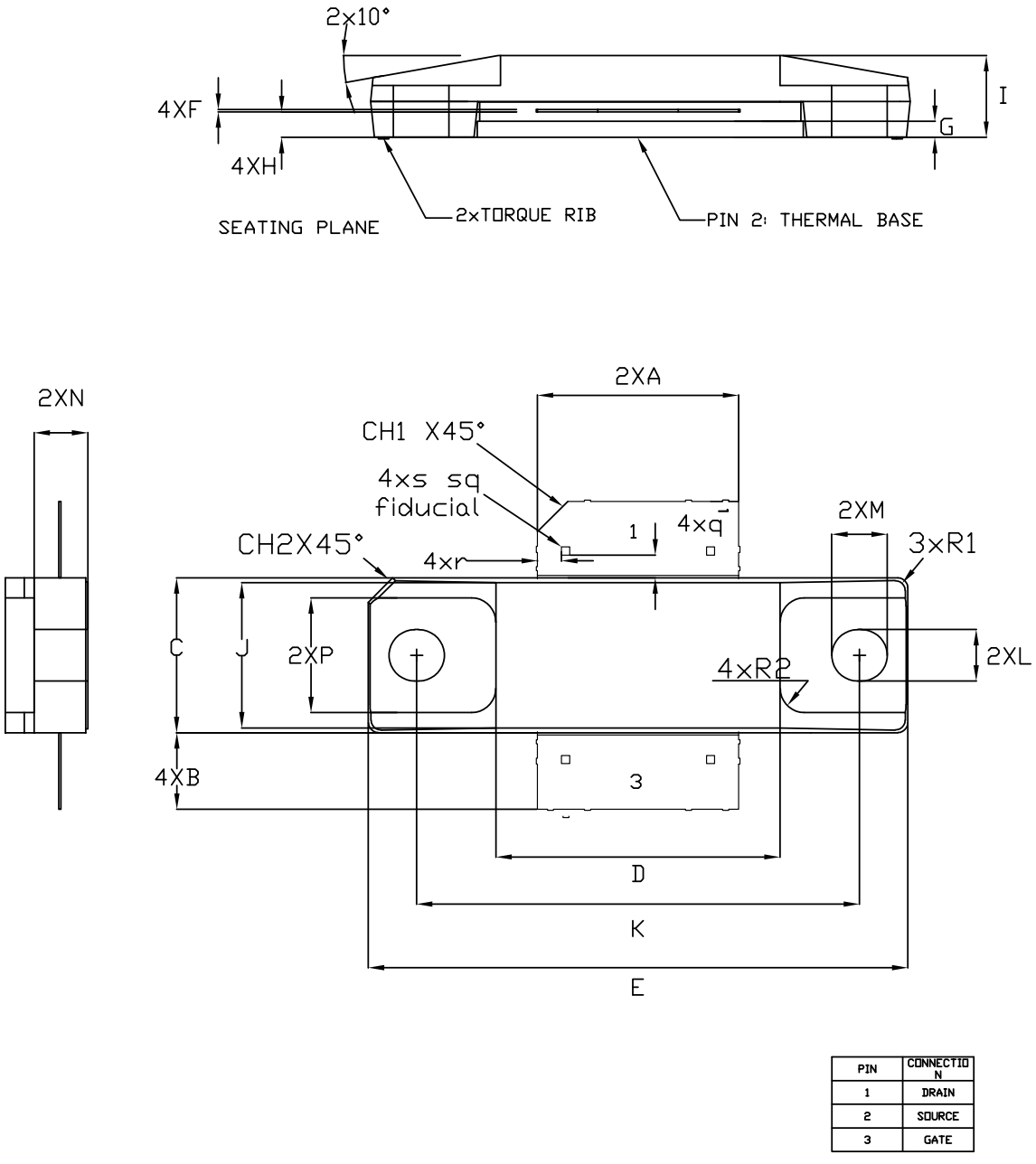


6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 STAC780-2B package information

Figure 8. **STAC780-2B package outline**



PIN	CONNECTION
1	DRAIN
2	SOURCE
3	GATE

DM00481924_2

Table 9. **STAC780-2B mechanical data**

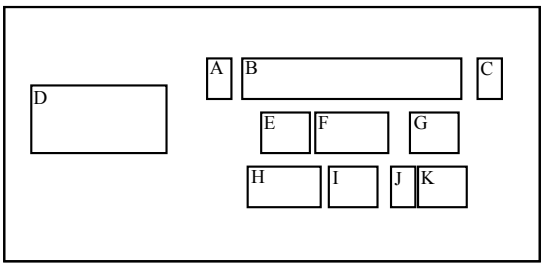
Ref.	Millimeters		
	Min.	Typ.	Max.
A	12.65		12.75
B	4.57		5.08
C	9.65		9.91
D	17.78		18.08
E	33.88		34.19
F	0.11		0.17
G	0.97		1.14
H	1.52		1.70
I	4.83		5.33
J	9.52		9.78
K	27.69		28.19
L	3.20	3.25	3.30
M	3.43	3.51	3.58
N	3.30	3.38	3.45
p	7.14	7.21	7.29
q		1.37	
r		1.52	
R1		0.63	
R2		1.52	
s		0.51	
θ		10°	
CH1		2.72	
CH2		1.52	

6.2 STAC780-2B marking information

Figure 9. **STAC780-2B marking information**

Product

PACKAGE FACE : TOP



LEGEND

Unmarkable Surface

Marking Composition Field

A ADDITIONAL INFORMATION
(MAX CHAR ALLOWED = 1)

B MARKING AREA

C ADDITIONAL INFORMATION
(MAX CHAR ALLOWED = 1)

D STANDARD ST LOGO
(0000093)

E Assy Plant
(PP)

F FE Sequence
(nnn)

G Diffusion Traceability
Plant
(WX)

H COUNTRY OF ORIGIN
(MAX CHAR ALLOWED = 3)

I Test & Finishing Plant
(TF)

J Assy Year
(Y)

K Assy Week
(WW)

CD00362879_13

Revision history

Table 10. **Document revision history**

Date	Version	Changes
20-Apr-2011	1	First release
09-Aug-2011	2	– Updated features on cover page. – Updated P_{DISS} value in *Table 2: Absolute maximum ratings*, R_{thJC} value in *Table 3: Thermal data @ 100 µs - 10 %*. – Updated typical and maximum values in *Table 5: Dynamic* – Inserted new T*able 6: Reference data* and *Section 3: Impedance data.* – Updated *figures: 3, 4* and *5*. – Minor text changes.
13-Sep-2011	3	Added *Section 5: Circuit and BOM*.
06-Jun-2012	4	– Modified: *Figure 6* – Added: *Figure 7* – Updated the entire *Table 8*
24-Sep-2012	5	Updated title on the cover page. Updated *Table 4.*
15-May-2014	6	Updated *Figure 8: Package dimensions*. Minor text changes. Document status promoted from preliminary to production data.
11-Jun-2015	7	Updated *Section 3: Impedance data*, *Section 4: Typical performance*and *Section 5: Circuit* and *BOM.*
09-Apr-2020	8	Updated Section 6.1 STAC780-2B package information. Added Table 3. ESD protection. Minor text changes.

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