ADVANCE DATA SHEET

SigmaTel, Inc.

Integrating Mixed-Signal Solutions

STAC9744

Stereo AC'97 Codec
With Multi-Codec Option and On-Chip SRCs

GENERAL DESCRIPTION:

SigmaTel's **STAC9744** is a general-purpose 18-bit stereo, full duplex, audio codec that conforms to the analog component specification of AC'97 (Audio Codec 97 Component Specification Rev. 2.1). The **STAC9744** incorporates ***SigmaTel's*** proprietary Sigma-Delta technology to achieve a DAC SNR in excess of 95dB and line through SNR of greater than 100dB. The DACs, ADCs, and mixer are integrated with analog I/Os, which include four analog line-level stereo inputs, two analog line-level mono inputs, two stereo outputs, and one mono output channel. Also included are ***SigmaTel's*** 3D stereo enhancement (***SS3D***), Variable Sample Rate Converters, and an extra true line-level out for headphones or speaker amplifiers. The **STAC9744** may be used as a secondary codec, with the **STAC9704/07/21/23** or a 4-channel **STAC9708** as the primary, in multiple codec configurations conforming to the AC'97 Rev. 2.1 specification. This configuration can provide up to six-channel output, delivering AC-3 playback for DVD applications. The **STAC9744** communicates via the five-wire AC-Link interface with any AC-Link capable controller or advanced core logic chip-set. Packaged in an AC'97 compliant 48-pin TQFP, the **STAC9744** can be placed on motherboards, daughter boards, add-on cards or docking stations.

FEATURES:

- **High performance ΣΔ technology**
- **Energy saving power down modes**
- **18-bit full duplex stereo ADC, DACs**
- **AC-Link protocol compliance**
- **Variable Sample Rate architecture**
- **Windows® Soft Audio Drivers Available**
- **Pin compatible with the STAC9700/21**
- **SigmaTel Surround (SS3D) Stereo Enhancement**
- **EAPD – External Amplifier Power Down Control**
- **Multi-Codec option (Intel AC'97 rev 2.1)**
- **Six analog line-level inputs**
- **48-pin TQFP**
- **LINE to LINE SNR 103dB**
- **DAC SNR 95 dB**
- **Simplified AMR MDC and MB operation**
- **+3.3V and +5V operation**

ORDERING INFORMATION:

Part Number	PACKAGE	TEMPERATURE RANGE	SUPPLY RANGE
STAC9744T	48-pin TQFP 7mm x 7mm x 1.4mm	0^{O} C to $+70^{O}$ C	DVdd = 3.3V or 5V, AVdd = 5V
STAC9745T	48-pin TQFP 7mm x 7mm x 1.4mm	0^{O} C to $+70^{O}$ C	DVdd = 3.3V, AVdd = 3.3V

SigmaTel reserves the right to change specifications without notice.

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Figure 1. Package Outline

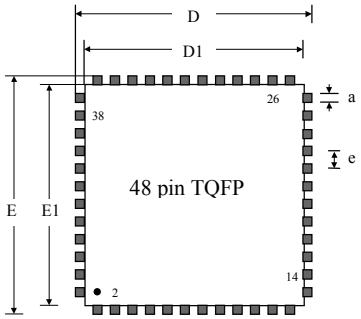


Table 1. Package Dimensions

Key	48-Pin TQFP Dimensions
D	9.00 mm
D1	7.00 mm
E	9.00 mm
E1	7.00 mm
a (lead width)	0.20 mm
e (pitch)	0.50 mm
thickness	1.6 mm

Table 2. Pin Designation

PIN #	Signal Name	PIN #	Signal Name	PIN #	Signal Name	PIN #	Signal Name
1	DVdd1	13	PHONE	25	AVdd1	37	MONO_OUT
2	XTL_IN	14	AUX_L	26	AVss1	38	AVdd2
3	XTL_OUT	15	AUX_R	27	Vref	39	LNLVL_OUT_L
4	DVss1	16	VIDEO_L	28	Vrefout	40	NC
5	SDATA_OUT	17	VIDEO_R	29	AFILT1	41	LNLVL_OUT_R
6	BIT_CLK	18	CD_L	30	AFILT2	42	AVss2
7	DVss2	19	CD_GND	31	SRC	43	NC
8	SDATA_IN0	20	CD_R	32	CAP2	44	NC
9	DVdd2	21	MIC1	33	ENABLE	45	CID0
10	SYNC	22	MIC2	34	PRIMARY_DN#	46	CID1
11	RESET#	23	LINE_IN_L	35	LINE_OUT_L	47	EAPD
12	PC_BEEP	24	LINE_IN_R	36	LINE_OUT_R	48	SDATA_IN1

# denotes active low

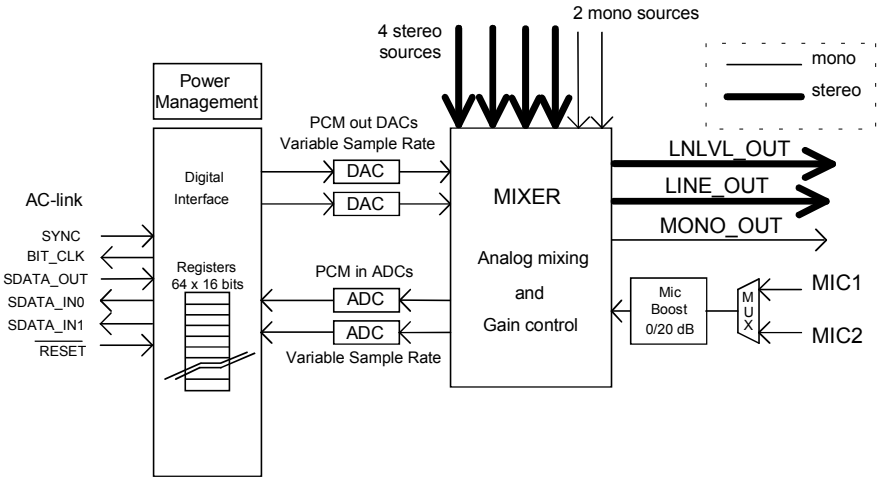


Figure 2. STAC9744 Block Diagram

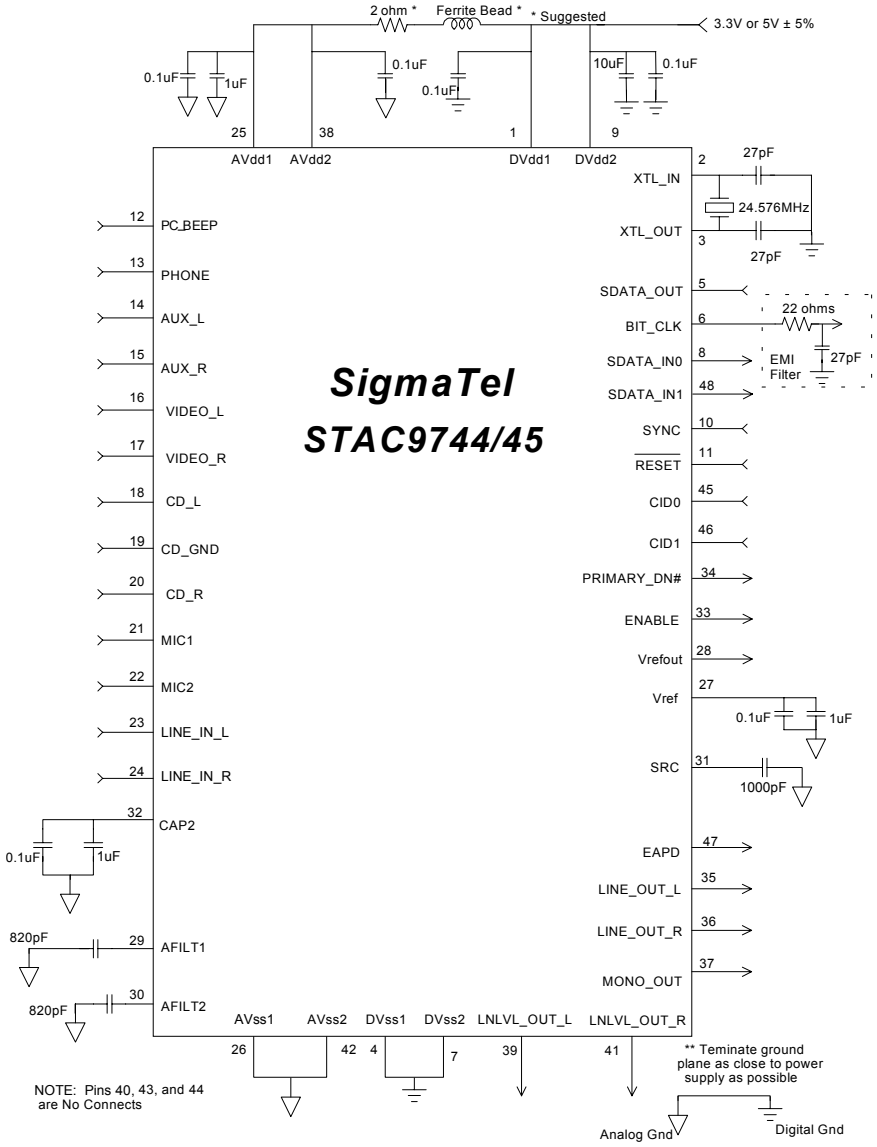
The **STAC9744** block diagram is illustrated above. It provides variable sample rate D-A & A-D conversion, mixing, and analog processing. Supported audio sample rates include 48kHz, 44.1kHz, 22.05kHz, 16kHz, 11.025kHz, and 8kHz; additional rates are supported in the **STAC9744** soft audio drivers. The digital interface communicates with the AC'97 controller via the five-wire AC-Link and contains the 64-word by 16-bit registers. The two DACs convert the digital stereo PCM-out content to audio. The MIXER block combines the PCM_OUT with any analog sources, to drive the LINE_OUT and LNLVL_OUT outputs. The MONO_OUT delivers either mic only, or a mono mix of sources from the MIXER. The two variable sample rate ADC's provide record capability for any mix of mono or stereo sources, and deliver a digital stereo PCM-in signal back to the AC-Link. All ADC's and DAC's operate at 18-bit resolution.

The **STAC9744** is designed primarily to support stereo, 2-speaker audio. However, true AC-3 playback can be achieved for 6-speaker applications by taking advantage of the multi-codec option in the **STAC9744**. Using this option with a **STAC9704/07/21/23** or the 4-channel **STAC9708** as the primary codec, and the **STAC9744** as the secondary codec, 6-channel output can be achieved in an AC'97 architecture. Also, the **STAC9744** provides for a stereo enhancement feature, ***SigmaTel Surround 3D or SS3D.*** ***SS3D*** provides the listener with several options for improved speaker separation beyond the normal 2-speaker arrangement.

Together, with the logic component (controller or advanced core logic chip-set) of AC'97, the **STAC9744** is DirectSound, SoundBlaster® and Windows Sound System® compatible. SoundBlaster® is a registered trademark of Creative Labs. Windows® is a registered trademark of Microsoft Corporation.

Figure 3. Connection Diagram

See Appendix A for an alternative connection diagram when using separate supplies.
See Appendix B for specific connection requirements prior to operation.



1. PIN/SIGNAL DESCRIPTIONS

1.1 Digital I/O

These signals connect the **STAC9744** to its AC'97 controller counterpart, an external crystal, multi-codec selection and external audio amplifier.

Table 3. Digital Signal List

Signal Name	Type	Description
RESET #	I	AC'97 Master H/W Reset
XTL_IN	I	24.576 MHz Crystal or external clock source
XTL_OUT	O	24.576 MHz Crystal
SYNC	I	48 kHz fixed rate sample sync
BIT_CLK	O	12.288 MHz serial data clock
SDATA_OUT	I	Serial, time division multiplexed, AC'97 input stream
SDATA__IN0	O	Serial, time division multiplexed, AC'97 output stream
SDATA__IN1	O	Alternate serial, time division multiplexed, AC'97 output stream
CID0	I	Multi-Codec ID select – bit 0
CID1	I	Multi-Codec ID select – bit 1
EAPD	O	External Amplifier Power Down
ENABLE	I	Codec enable control (normally left floating)
PRIMARY_DN#	I/O	Primary Codec “Down” Control/Input

# denotes active low

1.2 Analog I/O

These signals connect the **STAC9744** to analog sources and sinks, including microphones and speakers.

Table 4. Analog Signal List

Signal Name	Type	Description
PC_BEEP	I	PC Speaker beep pass-through
PHONE	I	From telephony subsystem speakerphone (or DLP - Down Line Phone)
MIC1	I	Desktop Microphone Input
MIC2	I	Second Microphone Input
LINE_IN_L	I	Line In Left Channel
LINE_IN_R	I	Line In Right Channel
CD_L	I	CD Audio Left Channel
CD_GND	I	CD Audio analog ground
CD_R	I	CD Audio Right Channel
VIDEO_L	I	Video Audio Left Channel
VIDEO_R	I	Video Audio Right Channel
AUX_L	I	Aux Left Channel
AUX_R	I	Aux Right Channel
LINE_OUT_L	O	Line Out Left Channel
LINE_OUT_R	O	Line Out Right Channel
MONO_OUT	O	To telephony subsystem speakerphone (or DLP – Down Line Phone)
LNLVL_OUT_L	O	True Line Level Out Left Channel, and POP mode monitor
LNLVL_OUT_R	O	True Line Level Out Right Channel, and POP mode monitor

* Note: any unused input pins should be tied together and connected to ground with a capacitor (0.1 uF suggested), except the MIC1 and MIC2 inputs which require their own 0.1 uF capacitors to ground if not used.

1.3 Filter/References/GPIO

These signals are connected to resistors, capacitors, specific voltages, or provide general purpose I/O.

Table 5. Filtering and Voltage References

Signal Name	Type	Description
Vref	O	Reference Voltage
Vrefout	O	Reference Voltage out 5mA drive (intended for mic bias)
AFILT1	O	Anti-Aliasing Filter Cap - ADC channel
AFILT2	O	Anti-Aliasing Filter Cap - ADC channel
SRC	O	SRC Bias Cap
CAP2	O	ADC reference Cap
EAPD	O	External Amplifier Power Down Control

1.4 Power and Ground Signals

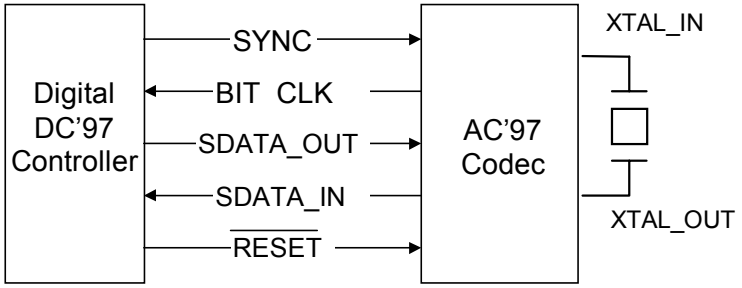
Table 6. Power Signal List STAC9744

Signal Name	Type	STAC9744	STAC9745
AVdd1	I	Analog Vdd = 5.0V	Analog Vdd = 3.3V
AVdd2	I	Analog Vdd = 5.0V	Analog Vdd = 3.3V
AVss1	I	Analog Gnd	Analog Gnd
AVss2	I	Analog Gnd	Analog Gnd
DVdd1	I	Digital Vdd = 5.0V or 3.3V	Digital Vdd = 3.3V
DVdd2	I	Digital Vdd = 5.0V or 3.3V	Digital Vdd = 3.3V
DVss1	I	Digital Gnd	Digital Gnd
DVss2	I	Digital Gnd	Digital Gnd

2. AC-LINK

Below is the figure of the AC-Link point to point serial interconnect between the **STAC9744** and its companion controller or advance core logic chipset. All digital audio streams and command/status data are communicated over this AC-Link. Please refer to the "Digital Interface" section 3 for details.

Figure 4. AC-Link to its companion controller



2.1 Clocking

STAC9744 derives its clock internally from an externally connected 24.576 MHz crystal or an oscillator through the XTAL_IN pin. Synchronization with the AC'97 controller is achieved through the BIT_CLK pin at 12.288 MHz (half of crystal frequency).

The beginning of all audio sample packets, or "Audio Frames", transferred over AC-Link is synchronized to the rising edge of the "SYNC" signal driven by the AC'97 controller. Data is transitioned on AC-Link on every rising edge of BIT_CLK, and subsequently sampled by the receiving side on each immediately following falling edge of BIT_CLK.

2.2 Reset

There are 3 types of resets as detailed under "Timing Characteristics".

1. a "cold" reset where all **STAC9744** logic and registers are initialized to their default state

2. a "warm" reset where the contents of the **STAC9744** register set are left unaltered

3. a “register” reset which only initializes the **STAC9744** registers to their default states

After signaling a reset to the **STAC9744,** the AC'97 controller should not attempt to play or capture audio data until it has sampled a “Codec Ready” indication via register 26h from the **STAC9744.**

For proper reset operation SDATA_OUT should be “0” during “cold” reset. See “Testability” section for more information.

3. DIGITAL INTERFACE

3.1 AC-Link Digital Serial Interface Protocol

The **STAC9744** communicates to the AC'97 controller via a 5-pin digital serial AC-Link interface, which is a bi-directional, fixed rate, serial PCM digital stream. All digital audio streams, commands and status information are communicated over this point-to-point serial interconnect. The AC-Link handles multiple inputs, and output audio streams, as well as control register accesses using a time division multiplexed (TDM) scheme. The AC'97 controller synchronizes all AC-Link data transaction. The following data streams are available on the **STAC9744:**

- **PCM Playback** **2 output slots** 2 Channel composite PCM output stream
- **PCM Record data** **2 input slots** 2 Channel composite PCM input stream
- **Control** **2 output slots** Control register write port
- **Status** **2 input slots** Control register read port

Synchronization of all AC-Link data transactions is handled by the AC'97 controller. The **STAC9744** drives the serial bit clock onto AC-Link. The AC'97 controller then qualifies with a synchronization signal to construct audio frames.

SYNC, fixed at 48 kHz, is derived by dividing down the serial bit clock (BIT_CLK). BIT_CLK, fixed at 12.288 MHz, provides the necessary clocking granularity to support 12, 20-bit outgoing and incoming time slots. AC-Link serial data is transitioned on each rising edge of BIT_CLK. The receiver of AC-Link data, **STAC9744** for outgoing data and AC'97 controller for incoming data, samples each serial bit on the falling edges of BIT_CLK.

The AC-Link protocol provides for a special 16-bit (13-bits defined, with 3 reserved trailing bit positions) time slot (Slot 0) wherein each bit conveys a valid tag for its corresponding time slot within the current audio frame. A “1” in a given bit position of slot 0 indicates that the corresponding time slot within the current audio frame has been assigned to a data stream, and contains valid data. If a slot is

"tagged" invalid, it is the responsibility of the source of the data (**STAC9744** for the input stream, AC'97 controller for the output stream) to stuff all bit positions with 0's during that slot's active time.

SYNC remains high for a total duration of 16 BIT_CLKs at the beginning of each audio frame. The portion of the audio frame where SYNC is high is defined as the "Tag Phase". The remainder of the audio frame where SYNC is low is defined as the "Data Phase".

Additionally, for power savings, all clock, sync, and data signals can be halted.

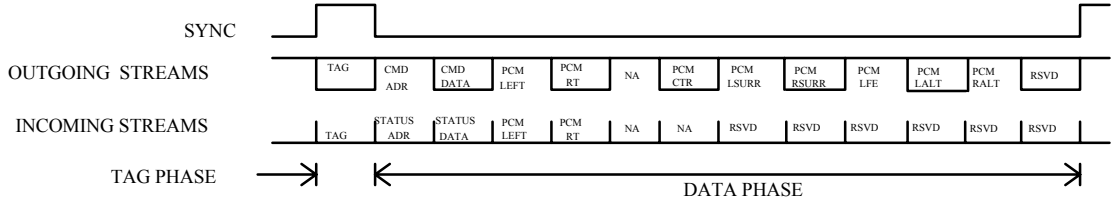


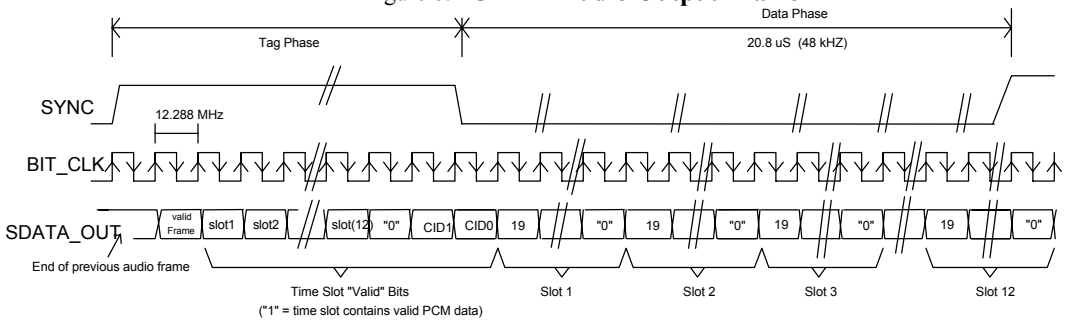
Figure 5. AC'97 Standard Bi-directional Audio Frame

3.2 AC-Link Audio Output Frame (SDATA_OUT)

The audio output frame data streams correspond to the multiplexed bundles of all digital output data targeting the **STAC9744** DAC inputs, and control registers. Each audio output frame supports up to 12 20-bit outgoing data time slots. Slot 0 is a special reserved time slot containing 16 bits that are used for AC-Link protocol infrastructure.

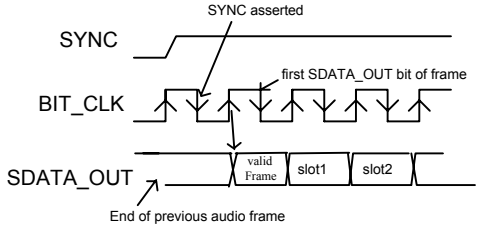
Within slot 0, the first bit is a global bit (SDATA_OUT slot 0, bit 15) which flags the validity for the entire audio frame. If the "Valid Frame" bit is a 1, this indicates that the current audio frame contains at least one slot time of valid data. The next 12 bit positions sampled by the **STAC9744** indicate which of the corresponding 12 times slots contain valid data. In this way data streams of differing sample rates can be transmitted across AC-Link at its fixed 48kHz audio frame rate. The following diagram illustrates the time slot based AC-Link protocol.

Figure 6.**AC-Link Audio Output Frame**



A new audio output frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, the **STAC9744** samples the assertion of SYNC. This following edge marks the time when both sides of AC-Link are aware of the start of a new audio frame. On the next rising edge of BIT_CLK, the AC'97 controller transitions SDATA_OUT into the first bit position of slot 0 (Valid Frame bit). Each new bit position is presented to AC-Link on a rising edge of BIT_CLK, and subsequently sampled by the **STAC9744** on the following falling edge of BIT_CLK. This sequence ensures that data transitions, and subsequent sample points for both incoming and outgoing data streams are time aligned.

Figure 7. Start of an Audio Output Frame



SDATA_OUT's composite stream is MSB justified (MSB first) with all non-valid slots' bit positions stuffed with 0's by the AC'97 controller. When mono audio sample streams are sent from the AC'97 controller it is necessary that BOTH left and right sample stream time slots be filled with the same data.

3.2.1.1 Slot 1: Command Address Port

The command port is used to control features, and monitor status (see Audio Input Frame Slots 1 and 2) of the **STAC9744** functions including, but not limited to, mixer settings, and power management (refer to the control register section of this specification).

The control interface architecture supports up to 64 16-bit read/write registers, addressable on even byte boundaries. Only the even registers (00h, 02h, etc.) are valid.

Audio output frame slot 1 communicates control register address, and write/read command information to the **STAC9744**.

Command Address Port bit assignments:

Bit (19) Read/Write command (1= read, 0=write)
Bit (18:12) Control Register Index (64 16-bit locations, addressed on even byte boundaries)
Bit (11:0) Reserved (Stuffed with 0's)

The first bit (MSB) sampled by **STAC9744** indicates whether the current control transaction is a read or a write operation. The following 7 bit positions communicate the targeted control register address. The trailing 12 bit positions within the slot are reserved and must he stuffed with 0's by the AC'97 controller.

3.2.1.2 Slot 2: Command Data Port

The command data port is used to deliver 16-bit control register write data in the event that the current command port operation is a write cycle. (as indicated by Slot 1, bit 19)

Bit (19:4)	Control Register Write Data	(Stuffed with 0's if current operation is a read)
Bit (3 :0)	Reserved	(Stuffed with 0's)

If the current command port operation is a read then the entire slot time must be stuffed with 0's by the AC'97 controller.

3.2.1.3 Slot 3: PCM Playback Left Channel

Audio output frame slot 3 is the composite digital audio left playback stream. In a typical “Games Compatible" PC this slot is composed of standard PCM (.wav) output samples digitally mixed (by the AC'97 controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20-bits is transferred, the AC'97 controller must stuff all trailing non-valid bit positions within this time slot with 0's. Please refer to the register programming section for details on the multi-channel programming options.

3.2.1.4 Slot 4: PCM Playback Right Channel

Audio output frame slot 4 is the composite digital audio right playback stream. In a typical “Games Compatible" PC this slot is composed of standard PCM (.wav) output samples

digitally mixed (by the AC'97 controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20-bits is transferred, the AC'97 controller must stuff all trailing non-valid bit positions within this time slot with 0's. Please refer to the register programming section for details on the multi-channel programming options.

3.2.1.5 Slot 5: Reserved

Audio output frame slot 5 is reserved for modem operation and is not used by the **STAC9744**.

3.2.1.6 Slot 6: PCM Center Channel

Audio output frame slot 6 is the composite digital audio center stream used in a multi-channel application where the **STAC9744** is programmed to accept the DAC PCM data from slots 6 and 9. Please refer to the register programming section for details on the multi-channel programming options.

3.2.1.7 Slot 7: PCM Left Surround Channel

Audio output frame slot 7 is the composite digital audio left stream used in a multi-channel application where the **STAC9744** is programmed to accept the DAC PCM data from slots 7 and 8. Please refer to the register programming section for details on the multi-channel programming options.

3.2.1.8 Slot 8: PCM Right Surround Channel

Audio output frame slot 8 is the composite digital audio right stream used in a multi-channel application where the **STAC9744** is programmed to accept the DAC PCM data from slots 7 and 8. Please refer to the register programming section for details on the multi-channel programming options.

3.2.1.9 Slot 9: PCM Low Frequency Channel

Audio output frame slot 9 is the composite digital audio low frequency stream used in a multi-channel application where the **STAC9744** is programmed to accept the DAC PCM data from slots 6 and 9. Please refer to the register programming section for details on the multi-channel programming options.

3.2.1.10 Slot 10: PCM Alternate Left

Audio output frame slot 10 is the composite digital audio alternate left stream used in a multi-channel application where the **STAC9744** is programmed to accept the primary DAC PCM data from slots 10 and 11. Please refer to the register programming section for details on the multi channel programming options.

3.2.1.11 Slot 11: PCM Alternate Right

Audio output frame slot 11 is the composite digital audio alternate right stream used in a multi-channel application where the **STAC9744** is programmed to accept the primary DAC

PCM data from slots 10 and 11. Please refer to the register programming section for details on the multi channel programming options.

3.1.1.12 Slot 12: Reserved

Audio output frame slot 12 is reserved for modem operations and is not used by the **STAC9744**.

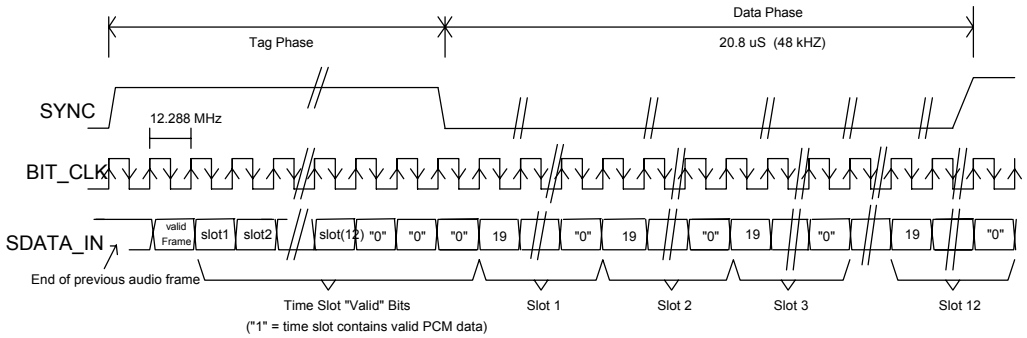
3.2.2 AC-Link Audio Input Frame (SDATA_IN)

The audio input frame data streams correspond to the multiplexed bundles of all digital input data targeting the AC'97 controller. As is the case for audio output frame, each AC-Link audio input frame consists of 12, 20-bit time slots. Slot 0 is a special reserved time slot containing 16 bits that are used for AC-Link protocol infrastructure.

Within slot 0 the first bit is a global bit (SDATA_IN slot 0, bit 15) which flags whether the **STAC9744** is in the "Codec Ready" state or not. If the “Codec Ready” bit is a 0, this indicates that **STAC9744** is not ready for normal operation. This condition is normal following the de-assertion of power on reset, for example, while **STAC9744**’s voltage references settle. When the AC-Link "Codec Ready" indicator bit is a 1, it indicates that the AC-Link and **STAC9744** control/status registers are in a fully operational state. The AC'97 controller must further probe the Powerdown Control Status Register index 26h (refer to Mixer Register section) to determine exactly which subsections, if any, are ready.

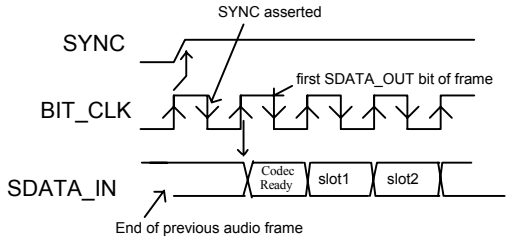
Prior to any attempts at putting **STAC9744** into operation the AC'97 controller should poll the first bit in the audio input frame (SDATA_IN slot 0, bit 15) for an indication that **STAC9744** has become "Codec Ready". Once the **STAC9744** is sampled "Codec Ready", the next 12 bit positions sampled by the AC'97 controller indicate which of the corresponding 12 time slots are assigned to input data streams, and that they contain valid data. The following diagram illustrates the time slot based AC-Link protocol.

Figure 8. STAC9744 Audio Input Frame



A new audio input frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, **STAC9744** samples the assertion of SYNC. This falling edge marks the time when both sides of AC-Link are aware of the start of a new audio frame. On the next rising of BIT_CLK, the **STAC9744** transitions SDATA_IN into the first bit position of slot 0 ("Codec Ready" bit). Each new bit position is presented to AC-Link on a rising edge of BIT_CLK and subsequently sampled by the AC'97 controller on the following falling edge of BIT_CLK. This sequence ensures that data transitions, and subsequent sample points for both incoming and outgoing data streams are time aligned.

Figure 9. Start of an Audio Input Frame



SDATA_IN's composite stream is MSB justified (MSB first) with all non-valid bit positions (for assigned and/or unassigned time slots) stuffed with 0's by **STAC9744**. SDATA_IN data is sampled on the falling edges of BIT_CLK.

3.2.2.1 Slot 1: Status Address Port

The status port is used to monitor status for **STAC9744** functions including, but not limited to, mixer settings, and power management.

Audio input frame slot 1's stream echoes the control register index, for historical reference, for the data to be returned in slot 2. (Assuming that slots 1 and 2 had been tagged "valid" by **STAC9744** during slot 0)

Status Address Port hit assignments:

Bit (19)	RESERVED	(Stuffed with 0)
Bit (18;12)	Control Register Index	(Echo of register index for which data is being returned)
Bit (11:0)	RESERVED	(Stuffed with 0's)

The first bit (MSB) generated by **STAC9744** is always stuffed with a 0. The following 7 bit positions communicate the associated control register address, and the trailing 12 bit positions are stuffed with 0's by **STAC9744**.

3.2.2.2 Slot 2: Status Data Port

The status data port delivers 16-bit control register read data.

Bit (19:4)	Control Register Read Data	(Stuffed with 0's if tagged "invalid")
Bit (3 :0)	RESERVED	(Stuffed with 0's)

If Slot 2 is tagged "invalid" by **STAC9744,** then the entire slot will be stuffed with 0's.

3.2.2.3 Slot 3: PCM Record Left Channel

Audio input frame slot 3 is the left channel output of **STAC9744** input MUX, post-ADC. **STAC9744** ADCs are implemented to support 18-bit resolution.

STAC9744 outputs its ADC data (MSB first), and stuffs any trailing non-valid bit positions with 0's to fill out its 20-bit time slot.

3.2.2.4 Slot 4: PCM Record Right Channel

Audio input frame slot 4 is the right channel output of **STAC9744** input MUX, post-ADC. **STAC9744** outputs its ADC data (MSB first), and stuffs any trailing non-valid bit positions with 0's to fill out its 20-bit time slot.

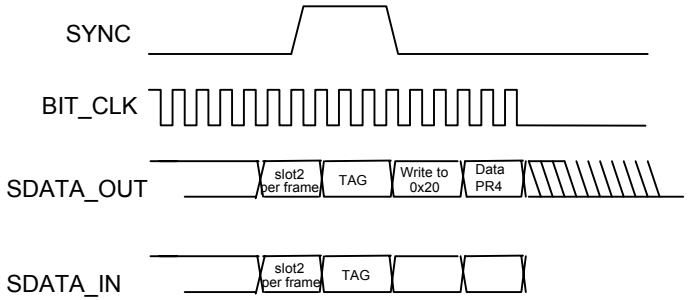
3.2.2.5 Slots 5-12: Reserved

Audio input frame slots 5-12 are not used by the **STAC9744/45** and are always stuffed with 0's.

3.3 AC-Link Low Power Mode

The **STAC9744** AC-Link can be placed in the low power mode by programming register 26h to the appropriate value. Both BIT_CLK and SDATA_IN will be brought to, and held at a logic low voltage level. The AC'97 controller can wake up the **STAC9744** by providing the appropriate reset signals.

Figure 10. STAC9744 Powerdown Timing



Note: BIT_CLK not to scale

BIT_CLK and SDATA_IN are transitioned low immediately (within the maximum specified time) following the decode of the write to the Powerdown Register (26h) with PR4. When the AC'97 controller driver is at the point where it is ready to program the AC-Link into its low power mode, slots (1 and 2) are assumed to be the only valid stream in the audio output frame (all sources of audio input have been neutralized).

The AC'97 controller should also drive SYNC and SDATA_OUT low after programming the **STAC9744** to this low power mode.

3.3.1 Waking up the AC-Link

Once the **STAC9744** has halted BIT_CLK, there are only two ways to "wake up" the AC-Link. Both methods must be activated by the AC'97 controller. The AC-Link protocol provides for a "Cold AC'97 Reset", and a "Warm AC'97 Reset". The current power down state would ultimately dictate which form of reset is appropriate. Unless a "cold" or "register" reset (a write to the Reset register) is performed, wherein the AC'97 registers are initialized to their default values, registers are required to keep state during all power down modes. Once powered down, re-activation of the AC-Link via re-assertion of the SYNC signal must not occur for a minimum of 4 audio frame times following the frame in which the power down was triggered. When AC-Link powers up it indicates readiness via the Codec Ready bit (input slot 0, bit 15).

Cold Reset - a cold reset is achieved by asserting RESET# for the minimum specified time. By driving RESET# low, BIT_CLK, and SDATA_IN will be activated, or re-activated as the case may be, and all **STAC9744** control registers will be initialized to their default power on reset values.

Note: RESET# is an asynchronous input. # denotes active low

Warm Reset - a warm reset will re-activate the AC-Link without altering the current **STAC9744** register values. A warm reset is signaled by driving SYNC high for a minimum of 1us in the absence of BIT_CLK.

Note: Within normal audio frames, SYNC is a synchronous input. However, in the absence of BIT_CLK, SYNC is treated as an asynchronous input used in the generation of a warm reset to the **STAC9744**.

4. STAC9744 MIXER

The **STAC9744** mixer is designed to the AC'97 specification to manage the playback and record of all digital and analog audio sources in the PC environment. These include:

- **System Audio**: digital PCM input and output for business, games and multimedia
- **CD/DVD**: analog CD/DVD-ROM Redbook audio with internal connections to Codec mixer
- **Mono microphone**: choice of desktop mic, with programmable boost and gain
- **Speakerphone**: use of system mic and speakers for telephone, DSVD, and video conferencing
- **Video**: TV tuner or video capture card with internal connections to Codec mixer
- **AUX/synth**: analog FM or wavetable synthesizer, or other internal source

Figure 11. STAC9744 Mixer Functional Diagram

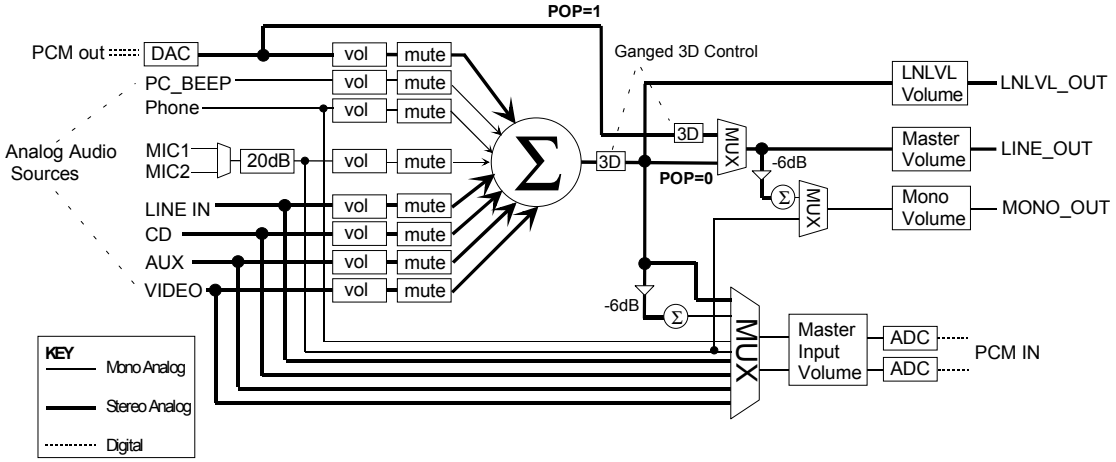


Table 7. Mixer Functional Connections

Source	Function	Connection
PC_Beep	PC beep pass thru	from PC beeper output
PHONE	speakerphone or DLP in	from telephony subsystem
MIC1	desktop microphone	from mic jack
MIC2	second microphone	from second mic jack
LINE_IN	external audio source	from line-in jack
CD	audio from CD-ROM	cable from CD-ROM
VIDEO	audio from TV tuner or video camera	cable from TV or VidCap card
AUX	upgrade synth or other external source	internal connector
PCM out	digital audio output from AC'97 Controller	AC-Link
LINE_OUT	stereo mix of all sources	To output jack
LNLVL_OUT	Additional stereo mix of all sources	To output jack
MONO_OUT	mic or mix for speakerphone or DLP out	to telephony subsystem
PCM in	digital audio input to AC'97 Controller	AC-Link

4.1 Mixer Input

The mixer provides recording and playback of any audio source or an output mix of all sources. The **STAC9744** supports the following input sources:

- any mono or stereo source
- mono or stereo mix of all sources
- 2-channel input w/mono output reference (mic + stereo mix)

* Note: any unused input pins should be tied together and connected to ground with a capacitor (0.1 uF suggested), except the MIC1 and MIC2 inputs which require their own 0.1 uF capacitors to ground if not used.

4.2 Mixer Output

The mixer generates several distinct outputs:

- a stereo mix of all sources for output to the LINE_OUT
- a stereo mix of all sources for output to the LNLVL_OUT
- a mono, mic only or mix of all sources for MONO_OUT
- DAC POP-BYPASS mode routes the PCM DAC output to the LINE_OUT and the MON_OUT, while the standard mixer output is routed to the ADC and the LNLVL_OUT for monitoring.

4.3 PC Beep Implementation

PC Beep is active on power up and defaults to an unmuted state. The user should mute this input before using any other mixer input because the PC Beep input can contribute noise to the LINE_OUT during normal operation. When the codec is disabled using the ENABLE control, the PC_BEEP is routed to the MONO_OUT even though the other codec outputs are disabled.

4.4 Programming Registers:

Table 8. Programming Registers

REG #	NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DE-FAULT
00h	Reset	X	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	6940h
02h	Master Volume	Mute	X	X	ML4	ML3	ML2	ML1	ML0	X	X	X	MR4	MR3	MR2	MR1	MR0	8000h
04h	LNLVL Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8000h
06h	Master Volume Mono	Mute	X	X	X	X	X	X	X	X	X	X	MM4	MM3	MM2	MM1	MM0	8000h
0Ah	PC_BEEP Volume	Mute	X	X	X	X	X	X	X	X	X	X	PV3	PV2	PV1	PV0	X	0000h
0Ch	Phone volume	Mute	X	X	X	X	X	X	X	X	X	X	GN4	GN3	GN2	GN1	GN0	8008h
0Eh	Mic Volume	Mute	X	X	X	X	X	X	X	X	20dB	X	GN4	GN3	GN2	GN1	GN0	8008h
10h	Line In Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
12h	CD Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
14h	Video Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
16h	AUX Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
18h	PCM Out Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
1Ah	Record Select	X	X	X	X	X	SL2	SL1	SL0	X	X	X	X	X	SR2	SR1	SR0	0000h
1Ch	Record Gain	Mute	X	X	X	GL3	GL2	GL1	GL0	X	X	X	X	GR3	GR2	GR1	GR0	8000h
20h	General Purpose	POP	X	3D	X	X	X	MIX	MS	LPBK	X	X	X	X	X	X	X	0000h
22h	3D Control	X	X	X	X	X	X	X	X	X	X	X	X	DP3	DP2	X	X	0000h
26h	Powerdown Ctrl/Stat	EAPD	PR6	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	000Fh
28h	Extended Audio ID	ID1	ID0	X	X	X	X	AMAP	X	X	X	X	X	X	X	X	VRA	X201h
2Ah	Extended Audio Control/Status	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	VRA	0000h
2Ch	PCM DAC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
32h	PCM LR ADC Rate	SR15	SR14	SR13	SR12	SR11	SR10	SR9	SR8	SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0	BB80h
6Ch	Revision Code	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000h
6Eh	Analog Special	X	X	X	X	X	X	X	X	X	X	X	X	X	X	DAC -6dB	ADC -6dB	0000h
70h	72h Enable	EN15	EN14	EN13	EN12	EN11	EN10	EN9	EN8	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0	0000h
72h	Analog Current Adjust	X	X	X	X	X	X	X	X	X	X	X	X	X	Bias1	Bias0	X	0000h
74h	Multi-Channel Selection	X	X	X	X	X	X	X	X	X	X	X	X	X	X	MC1	MC0	0000h
76h	78h Enable	EN15	EN14	EN13	EN12	EN11	EN10	EN9	EN8	EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0	0000h
78h	Clock Access	X	X	ALT CLK	X	CLK INV	DCT DIS	X	X	X	X	X	X	X	X	OSC PWD	X	0000h
7Ch	Vendor ID1	1	0	0	0	0	0	1	1	1	0	0	0	0	1	0	0	8384h
7Eh	Vendor ID2	0	1	1	1	0	1	1	0	0	1	0	0	0	1	0	0	7644h

1. All registers not shown and bits containing an X are reserved, and should not be written to.

2. PC_BEEP defaults to 0000h, un-muted.

3. If optional bits D13 and D5 of register 02h and 04h, or D5 of register 06h are set to 1, then the corresponding attenuation is set to 46dB and the register reads will produce 1Fh as a value for this attenuation/gain block.

4.4.1 Reset Register (Index 00h)

Writing any value to this register performs a register reset, which causes all registers to revert to their default values. Reading this register returns the AC'97 ID code of the part.

4.4.2 Play Master Volume Registers (Index 02h, 04h, and 06h)

These registers manage the output signal volumes. Register 02h controls the stereo master volume (both right and left channels), register 04h controls the optional stereo true line level out, and register 06h controls the mono volume output. Each step corresponds to 1.5 dB. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at -∞ dB. ML5 through ML0 is for left channel level, MR5 through MR0 is for the right channel and MM5 through MM0 is for the mono out channel. If optional bits D13 and D5 of register 02h and 04h, or D5 of register 06h are set to 1, then the corresponding attenuation is set to 46dB and the register reads will produce 1Fh as a value for this attenuation/gain block.

The default value is 8000h for registers 02h, 04h and 06h corresponding to 0 dB attenuation with mute on.

Table 9. Play Master Volume Register

Mute	Mx5…Mx0	Function	Range
0	00 0000	0dB Attenuation	Req.
0	01 1111	46.5 Attenuation	Req.
1	xx xxxx	∞ dB Attenuation	Req.

4.4.3 PC Beep Register (Index 0Ah)

This register controls the level for the PC Beep input. Each step corresponds to approximately 3 dB of attenuation. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at -∞ dB. PC_BEEP supports motherboard implementations. The intention of routing PC_BEEP through the **STAC9744** mixer is to eliminate the requirement for an onboard speaker by guaranteeing a connection to speakers connected via the output jack. In order for this to be viable the PC_BEEP signal needs to reach the output jack at all times. PC_BEEP should be routed to L & R Line outputs even when the **STAC9744** is in a RESET state. Power On Self Test (POST) codes can be heard by the user when PC_BEEP is un-muted in case of a hardware problem with the PC. For further PC_BEEP implementation details please refer to the AC'97 Technical FAQ sheet. The default value is 0000h, which corresponds to 0 dB attenuation with mute off.

Table 10. PC_BEEP Register

Mute	PV3…PV0	Function
0	0000	0 dB Attenuation
0	1111	45 dB Attenuation
1	xxxx	∞ dB Attenuation

4.4.4 Analog Mixer Input Gain Registers (Index 0Ch - 18h)

The analog mixer input registers control the gain/attenuation for each of the analog inputs. Each step corresponds to approximately 1.5 dB. The MSB of the register is the mute bit. When the MSB is set to 1 the level for that channel is set at -∞ dB. Register 0Eh (Mic Volume Register) has an extra bit which enables a 20dB gain boost. When bit 6 is set to 1, the 20 dB boost is on. The default value for the MIC and PHONE registers is 8008h, which corresponds to 0dB gain with mute on. The default value for stereo registers is 8808h, which corresponds to 0 dB gain with mute on.

Table 11. Analog Mixer Input Gain Register

Mute	Gx4…Gx0	Function
0	00000	+12 dB gain
0	01000	0 dB gain
0	11111	-34.5 dB gain
1	xxxxx	-∞ dB gain

4.4.5 Record Select Control Register (Index 1Ah)

Used to select the record source independently for right and left. The default value is 0000h, which corresponds to MIC in.

Table 12. Record Select Control Registers

SR2…SR0	Right Record Source
0	MIC
1	CD IN (right)
2	VIDEO IN (right)
3	AUX IN (right)
4	LINE_IN (right)
5	Stereo Mix (right)
6	Mono Mix
7	PHONE

SL2…SL0	Left Record Source
0	MIC
1	CD IN (left)
2	VIDEO IN (left)
3	AUX IN (left)
4	LINE_IN (left)
5	Stereo Mix (left)
6	Mono Mix
7	PHONE

4.4.6 Record Gain Registers (Index 1Ch)

The 1Ch register adjusts the stereo input record gain. Each step corresponds to 1.5 dB. The 22.5 dB setting corresponds to 0F0Fh. The MSB of the register is the mute bit. When this bit is set to 1, the level for that channel(s) is set at -∞ dB.

The default value is 8000h, which corresponds to 0 dB gain with mute on.

Table 13. Record Gain Registers

Mute	Gx3… Gx0	Function
0	1111	+22.5 dB gain
0	0000	0 dB gain
1	xxxx	-∞ gain

4.4.7 General Purpose Register (Index 20h)

This register is used to control some miscellaneous functions. Below is a summary of each bit and its function. The MS bit controls the MIC1/MIC2 selector, and the MIX bit controls the Mix/MIC selector. The LPBK bit enables loopback of the ADC output to the DAC input without involving the AC-Link, allowing for full system performance measurements. The 3D bit enables or disables the SS3D speaker separation 3D enhancement. The POP bit allows the PCM DAC signal to pass directly to the output without first going through the mixer. This features allows independent playback and recording which facilitates the handling of local and remote analog sources in multi-codec systems as is often the case in docking station applications. Note that the 3D can remain active when the mixer bypass mode is active. If the 3D is not desired during mixer bypass operations it should also be disabled. The LINE_OUT and MONO outputs are directly driven by the PCM DAC in POP bypass mode, while the LNLVL_OUT acts as a record monitor.

Table 14. General Purpose Register

Bit	Function
POP	PCM Mixer bypass 0 = normal mode, 1 = PCM DAC output bypassed directly to the outputs
3D	3D Stereo Enhancement 0 = off, 1 = on
MIX	Mono output select 0 = Mix, 1= MIC
MS	Mic select 0 = MIC1, 1 = MIC2
LPBK	ADC/DAC loopback mode

4.4.8 3D Control Register (Index 22h)

This register is used to control the 3D stereo enhancement function, ***SigmaTel Surround 3D (SS3D),*** built into the codec. ***SS3D*** provides for a wider soundstage and speaker separation for 2-speaker arrangements. Register bits, DP3-DP2 are used to control the separation ratios in the 3D control for LINE_OUT. The 3D bit in the general purpose register (register 20h bit D13) must be set to 1 to enable SS3D functionality and for the bits in 22h to take effect.

Table 15. 3D Control Registers

DP3..DP0	LINE_OUT Separation Ratio
00XX	0 (Off)
01XX	3 (Low)
10XX	4.5 (Med.)
11XX	6.0 (High)

The three separation ratios are implemented as shown above. The separation ratio defines a series of equations that determine the amount of depth difference (High, Medium, and Low) perceived during two-channel playback. The ratios provide an indication of how much soundstage increase can be expected.

4.4.9 Powerdown Control/Status Register (Index 26h)

This read/write register is used to program powerdown states and monitor subsystem readiness. The lower half of this register is read only status, a "1" indicating that the subsection is "ready". *Ready* is defined as the subsection's ability to perform in its nominal state. When this register is written, bits D7:D0 will not be affected. Bit D15 controls the External Amplifier Power Down pin.

When the AC-Link "Codec Ready" indicator bit (SDATA_IN slot 0, bit 15) is a 1, it indicates that the AC-Link and AC'97 control and status registers are in a fully operational state. The AC'97 controller must further probe this Powerdown Control/Status Register (D3:D0) to determine exactly which subsections, if any are ready.

Table 16. Powerdown Status Registers

BIT	FUNCTION
EAPD	External Amplifier Power Down
REF	Indicates VREF is at nominal level
ANL	Analog mixers, etc. ready
DAC	DAC section ready to playback data
ADC	ADC section ready to playback data

4.4.9.1 External Amplifier Power Down Control

The EAPD bit D15 of the Powerdown Control/Status Register (Index 26h) directly controls the output of the EAPD output, pin 45, and produces a logical "1" when this bit is set to logic high. This function is used to control an external audio amplifier power down. EAPD = 0 places approximately 0V on the output pin, enabling an external audio amplifier. EAPD = 1 places approximately DVDD on the output pin, disabling the external audio amplifier. Audio amplifiers that operate with reverse polarity will likely require an external inverter to maintain software driver compatibility.

4.4.10 Extended Audio ID Register (Index 28h)

The Extended Audio ID register is a read only register. ID1 and ID0 echo the configuration of the codec as defined by the programming of pins 45 and 46 externally. "00" returned defines the codec as the primary codec, while any other code identifies the codec as one of three secondary codec possibilities. The AMAP bit, D9, will return a 1 indicating that the codec supports the optional "AC'97 2.1 compliant AC-link slot to audio DAC mappings". The default condition assumes that 0, 0 are loaded in the MC1

and MC0 bits of the Multi-Channel Programming Register (Index 74h). With 0s in the MCx bits, the codec slot assignments are as per the AC'97 specification recommendations. If the MCx bits do not contain 0s, the slot assignments are as per the table in the section describing the Multi-Channel Programming Register (Index 74h). The VRA bit, D0, will return a 1 indicating that the codec supports the optional variable sample rate conversion as defined by the AC'97 specification.

Table 17. Extended Audio ID Register Functions

BIT	FUNCTION
IDx	External CID pin status
AMAP	Multi-channel slot support
VRA	Variable sample rates supported

4.4.11 Extended Audio Status/Control Register (Index 2Ah)

The Extended Audio Status Control register contains one active bit to enable or disable the Variable Sampling Rate capabilities of the DACs and ADCs. If the VRA, bit D0, is 1 the variable sample rate control registers (2Ch and 32h) are active, and "on-demand" slot data required transfers are allowed. If the VRA bit is 0, the DACs and ADCs will operate at the default 48 kHz data rate.

The **STAC9744** supports "on-demand" slot request flags. These flags are passed from the codec to the AC'97 controller in every audio input frame. Each time a slot request flag is set (active low) in a given audio frame, the controller will pass the next PCM sample for the corresponding slot in the audio frame that immediately follows. The VRA enable bit must be set to 1 to enable "on-demand" data transfers. If the VRA enable bit is not set, the codec will default to 48 kHz transfers and every audio frame will include an active slot request flag and data is transferred every frame.

For variable sample rate output, the codec examines its sample rate control registers, the state of the FIFOs, and the incoming SDATA_OUT tag bits at the beginning of each audio output frame to determine which SLOTREQ bits to set active (low). SLOTREQ bits are asserted during the current audio input frame for active output slots, which will require data in the next audio output frame.

For variable sample rate input, the tag bit for each input slot indicates whether valid data is present or not. Thus, even in variable sample rate mode, the codec is always the master: for SDATA_IN (codec to controller), the codec sets the TAG bit; for SDATA_OUT (controller to codec), the codec sets the SLOTREQ bit and then checks for the TAG bit in the next frame. Whenever VRA is set to 0 the PCM rate registers (2Ch and 32h) are overwritten with BB80h (48 kHz).

4.4.12 PCM DAC Rate Registers (Index 2Ch and 32h)

The internal sample rate for the DACs and ADCs are controlled by the value in these read/write registers that contain a 16-bit unsigned value between 0 and 65535 representing the conversion rate in Hz. In VRA mode (register 2Ah bit D0 = 1), if the value written to these registers is supported that value will be echoed back when read, otherwise the closest (higher in the case of a tie) sample rate is supported and returned. As allowed by the AC'97 specification, the ADCs and the DACs jointly operate at the same specified sample rate. In VRA mode, when either register is written, both registers will be modified to reflect the new sample rate setting. Whenever VRA is set to 0 the PCM rate registers (2Ch and 32h) are overwritten with BB80h (48 kHz).

Table 18. Hardware Supported Sample Rates

Sample Rate	SR15-SR0 Value
8 kHz	1F40h
11.25 kHz	2B11h
16 kHz	3E80h
22.05 kHz	5622h
44.1 kHz	AC44h
48 kHz	BB80h

4.4.13 Revision Code Register (Index 6Ch)

The device Revision register (index 6Ch) contains a software readable revision-specific code used to identify performance, architectural, or software differences between various device revisions. Bits 7:0 of the Revision register are user readable; bits 15:8 are not used at this time and will return zeros when read. The lower order bits of the Revision Register (bits 7:0) are currently set to 00h, and will likely change if there are any **STAC9744** metal revisions. This value can be used by the audio driver, or miniport driver in the case of WIN98® WDM approaches, to adjust software functionality to match the feature-set of the **STAC9744**. This will allow the software driver to identify any required operational differences between the existing **STAC9744** and any future versions.

4.4.14 Analog Special Register (Index 6Eh)

The Analog Special Register has two read/write bits used to control two functions specific to the **STAC9744.** DAC –6dB is used to program the DAC outputs to a –6dB signal level relative to the value of gain already programmed. Similarly, ADC –6dB attenuates any signal input to the ADC by 6dB.

4.4.15 Analog Current Adjust (Index 70h and 72h)

The Analog Current Adjust register (index 72h) is a locked register and can only be properly written and read from when ABBAh has been written into register 70h. The BIASx bits allow the analog current to be adjusted with minimal reduction in performance. The –50% analog current setting is not recommended when a 5V analog supply is used. The –50% setting for 3.3V supplies is recommended to reduce power consumption for notebook computers to its lowest level.

Table 19: Analog Current Adjust

BIAS1	BIAS0	Analog Current
0	0	Normal Current
0	1	-50% Analog Current
1	0	-25% Analog Current
1	1	+25% Analog Current

4.4.16 Multi-Channel Programming Register (Index 74h)

This read/write register is used to program the various options for multi-channel configurations. Only the two LSBs are used (MC0 and MC1), and they define which AC-Link slot data is supplied to the two PCM output channels on the **STAC9744.** The purpose of using slot 10 and 11 in the final configuration is to allow for the possibility of an eight channel architecture using several **STAC9744** or STAC9708 devices in the multi-codec configuration. Also see "Multiple Codec Support" discussion for information on the use of external pins CID1 and CID0.

Table 20. Multi-Channel Programming Register

External Pins CID1, CID0	Extended Audio ID 28h ID1, ID0	Codec Designation	Multi-Channel Selection 74h MC1, MC0	PCM OUT Left	PCM OUT Right
CID1 = DVdd or floating, CID0 = DVdd or floating	0, 0	Primary, 00	0, 0	Slot 3	Slot 4
			0, 1	Slot 7	Slot 8
			1, 0	Slot 6	Slot 9
			1, 1	Slot 10	Slot 11
CID1 = DVdd or floating, CID0 = GND	0, 1	Secondary, 01	0, 0	Slot 3	Slot 4
			0, 1	Slot 7	Slot 8
			1, 0	Slot 6	Slot 9
			1, 1	Slot 10	Slot 11
CID1 = GND, CID0 = DVdd or floating	1, 0	Secondary, 10	0, 0	Slot 7	Slot 8
			0, 1	Slot 3	Slot 4
			1, 0	Slot 10	Slot 11
			1, 1	Slot 6	Slot 9
CID1 = GND, CID0 = GND	1, 1	Secondary, 11	0, 0	Slot 6	Slot 9
			0, 1	Slot 10	Slot 11
			1, 0	Slot 3	Slot 4
			1, 1	Slot 7	Slot 8

4.4.17 Clock Access (Index 76h and 78h)

The Clock Access register (index 78h) is a locked register and can only be properly written and read from when ABBAh has been written into register 76h. The **STAC9744/45** can operate as a remotely located secondary without a 24.576MHz master clock input or local crystal. The **STAC9744/45** can synchronize to the BIT_CLK after two register adjustments. The first adjustment starts the synchronization process by enabling the ALTCLK D13, CLK INV D11, and OSC PWD D1 bits of register 78h. The second adjustment turns off the oscillator detect circuit by enabling the DET DIS D10 bit. With these adjustments, the **STAC9744/45** will operate remotely without the 24.576 MHz master clock signal and without a local crystal. The XTAL_IN can either be left floating, or connected to DGND with a 10kΩ or larger resistor.

4.4.18 Vendor ID1 and ID2 (Index 7Ch and 7Eh)

These two registers contain four 8-bit ID codes. The first three codes have been assigned by Microsoft using their Plug and Play Vendor ID methodology. The fourth code is a *SigmaTel*, Inc. assigned code identifying the **STAC9744**. The ID1 register (index 7Ch) contains the value 8384h, which is the first (83h) and second (84h) characters of the Microsoft® ID code. The ID2 register (index 7Eh) contains the value 7644h, which is the third (76h) of the Microsoft® ID code, and 44h which is the **STAC9744** ID code.

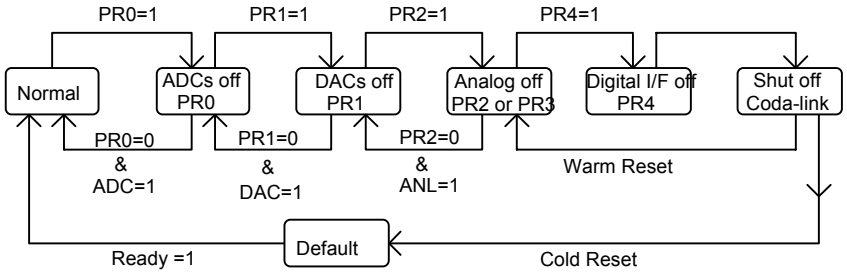
5. Low Power Modes

The **STAC9744** is capable of operating at reduced power when no activity is required. The state of power down is controlled by the Powerdown Register (26h). There are 7 separate power down commands. The power down options are listed in Table 19. The first three bits , PR0..PR2, can be used individually or in combination with each other, controling power distribution to the ADC's, DAC's and Mixer. The last analog power control bit, PR3, affects analog bias and reference voltages, and can only be used in combination with PR1, PR2, and PR3. PR3 essentially removes power from all analog sections of the codec, and is generally only asserted when the codec will not be needed for long periods. PR0 and PR1 control the PCM ADC's and DAC's only. PR2 and PR3 do not need to be "set" before a PR4, but PR0 and PR1 must be "set" before PR4.

Table 21. Low Power Modes

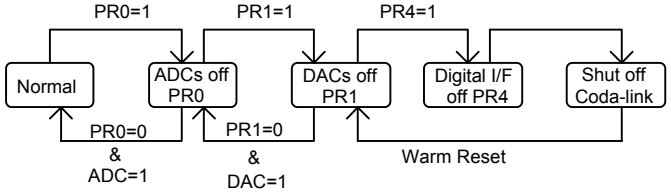
PRx Bits	Function
PR0	PCM in ADC's & Input Mux Powerdown
PR1	PCM out DACs Powerdown
PR2	Analog Mixer powerdown (Vref still on)
PR3	Analog Mixer powerdown (Vref off)
PR4	Digital Interface (AC-Link) powerdown (extnl clk off)
PR5	Internal Clk disable
PR6	LNLVL_OUT disable

Figure 12. Example of STAC9744 Powerdown/Powerup flow



The above figure illustrates one example procedure to do a complete powerdown of **STAC9744**. From normal operation, sequential writes to the Powerdown Register are performed to power down **STAC9744** a piece at a time. After everything has been shut off, a final write (of PR4) can be executed to shut down the AC-Link. The part will remain in sleep mode with all its registers holding their static values. To wake up, the AC'97 controller will send an extended pulse on the sync line, issuing a warm reset. This will restart the AC-Link (resetting PR4 to zero). The **STAC9744** can also be woken up with a cold reset. A cold reset will reset all of the registers to their default states. When a section is powered back on, the Powerdown Control/Status register (index 26h) should be read to verify that the section is ready (stable) before attempting any within that section.

Figure 13. STAC9744 Powerdown/Powerup flow with analog still alive



The above figure illustrates a state when all the mixers should work with the static volume settings that are contained in their associated registers. This configuration can be used when playing a CD (or external LINE_IN source) through **STAC9744** to the speakers, while most of the system in low power mode. The procedure for this follows the previous example except that the analog mixer is never shut down.

6. MULTIPLE CODEC SUPPORT

The **STAC9744** provides support for the multi-codec option according to the Intel AC'97, rev 2.1 specification. By definition there can be only one Primary Codec (Codec ID 00) and up to three Secondary Codecs (Codec IDs 01,10, and 11). The Codec ID functions as a chip select. Secondary devices therefore have completely orthogonal register sets; each is individually accessible and they do not share registers.

6.1 Primary/Secondary Codec Selection

In a multi-codec environment the codec ID is provided by external programming of pins 45 and 46 (CID0 and CID1). The CID pin electrical function is logically inverted from the codec ID designation. The corresponding pin state and its associated codec ID are listed in the "Codec ID Selection" table. Also see slot assignment discussion, “Multi-Channel Programming Register (Index 74)”.

Table 22. Codec ID Selection

CID1 State	CID0 State	Codec ID	Codec Status	EXTENDED AUDIO ID, 28h ID1, ID0
+5V or floating	+5V or floating	00	Primary	0, 0
+5V or floating	0V	01	Secondary	0, 1
0V	+5V or floating	10	Secondary	1, 0
0V	0V	11	Secondary	1, 1

6.1.1 Primary Codec Operation

As a Primary device the **STAC9744** is completely compatible with existing AC'97 definitions and extensions. Primary Codec registers are accessed exactly as defined in the AC'97 Component Specification and AC'97 Extensions. The **STAC9744** operates as Primary by default, and the external ID pins (45 and 46) have internal pull-ups so that these pins may be left as no-connects for primary operation.

When used as the primary codec, the **STAC9744** generates the master AC-Link BIT_CLK for both the AC'97 Digital Controller and any secondary codecs. The **STAC9744** can support up to four, 10 KΩ 50 pF loads on the BIT_CLK. This is to insure that up to 4 Codec implementations will not load down the clock output.

6.1.2 Secondary Codec Operation

When the **STAC9744** is configured as a Secondary device the BIT_CLK pin is configured as an input at power up. Using the BIT_CLK provided by the Primary Codec insures that everything on the AC-Link will be synchronous. As a Secondary device it can be defined as Codec ID 01, 10, or 11 in the two-bit field(s) of the Extended Audio and/or Extended Modem ID Register(s).

6.2 Secondary Codec Register Access Definitions

The AC'97 Digital Controller can independently access Primary and Secondary Codec registers by using a 2-bit Codec ID field (chip select) which is defined as the LSBs of Output Slot 0. For Secondary Codec access, the AC'97 Digital Controller must *invalidate* the tag bits for Slot 1 and 2 Command Address and Data (Slot 0, bits 14 and 13) and place a *non-zero* value (01, 10, or 11) into the Codec ID field (Slot 0, bits 1 and 0).

As a Secondary Codec, the **STAC9744** will disregard the Command Address and Command Data (Slot 0, bits 14 and 13) tag bits when it sees a 2-bit Codec ID value (Slot 0, bits 1 and 0) that matches its configuration. In a sense the Secondary Codec ID field functions as an alternative Valid Command Address (for Secondary reads and writes) and Command Data (for Secondary writes) tag indicator.

Secondary Codecs must monitor the Frame Valid bit, and ignore the frame (regardless of the state of the Secondary Codec ID bits) if it is not valid. AC'97 Digital Controllers should set the frame valid bit for a frame with a secondary register access, even if no other bits in the output tag slot except the Secondary Codec ID bits are set.

This method is designed to be backward compatible with existing AC'97 controllers and Codecs. There is no change to output Slot 1 or 2 definitions.

Table 23. Secondary Codec Register Access Slot 0 Bit Definitions

Output Tag Slot (16-bits)	
Bit	**Description**
15	Frame Valid
14	Slot 1 Valid Command Address bit (†Primary Codec only)
13	Slot 2 Valid Command Data bit (†Primary Codec only)
12-3	Slot 3-12 Valid bits as defined by AC'97
2	Reserved (Set to "0")
†1-0	2-bit Codec ID field (00 reserved for Primary; 01, 10, 11 indicate Secondary)
† New definitions for Secondary Codec Register Access	

7. TESTABILITY

The **STAC9744** has two test modes. One is for ATE in-circuit test and the other is restricted for ***SigmaTel's*** internal use. **STAC9744** enters the ATE in circuit test mode if SDATA_OUT is sampled high at the trailing edge of RESET#. Once in the ATE test mode, the digital AC-Link outputs (BIT_CLK and SDATA_IN) are driven to a high impedance state. This allows ATE in-circuit testing of the AC'97 controller. This case will never occur during standard operating conditions. Once either of the two test modes have been entered, the **STAC9744/45** must be issued another reset with all AC-link signals held low to return to the normal operating mode.

8. EXTENDED CODEC FUNCTIONALITY

8.1 SDATA_IN Auto Switch Function

The **STAC9744** supports automatic switching of the codec's SDATA_IN output from the typical SDATA_IN0 line of the AMR (Audio Modem Riser card) or MDC (Mobile Daughter Card) connectors, to one of the secondary connector SDATA_INx lines. Typically the SDATA_IN output of the primary codec would be routed to the connector's (and then to the audio controller's) SDATA_IN0 pin. Secondary codecs would be routed to one of the three remaining connector SDATA_INx lines. The **STAC9744** will output on the SDATA_IN0 pin in both secondary and primary modes if the PRIMARY_DN# pin is floating. If the PRIMARY_DN# pin is grounded and the codec is in secondary mode with the codec ID not equal to 00, the codec SDATA_IN output will be routed to the SDATA_IN1 pin and the SDATA_IN0 pin will be placed in a high impedance mode. If the codec is the primary with the ID equal to 00, the SDATA_IN output signal will always be routed to the SDATA_IN0 pin.

Table 24. Codec SDATA_IN Redirection in Secondary Mode

Codec ID	Codec Status	Codec PRIMARY_DN# Pin 43 floating	Codec PRIMARY_DN# Pin 43 tied to logic LOW	Recommended codec SDATA_IN0 pin 8 connection to AMR/MDC connector	Recommended codec SDATA_IN1 pin 48 connection to AMR/MDC connector
00	Primary	SDATA_IN0 pin 8 active	SDATA_IN0 pin 8 active	Connector SDATA_IN0	Don't Care
01	Secondary	SDATA_IN0 pin 8 active	SDATA_IN1 pin 48 active	Connector SDATA_IN0	Connector SDATA_IN1
10	Secondary	SDATA_IN0 pin 8 active	SDATA_IN1 pin 48 active	Connector SDATA_IN0	Connector SDATA_IN2
11	Secondary	SDATA_IN0 pin 8 active	SDATA_IN1 pin 48 active	Connector SDATA_IN0	Connector SDATA_IN3

8.2 PRIMARY_DN# Input/Output

PRIMARY_DN# Input Mode - The PRIMARY_DN# pin is always and input, and can be tied to ground to enable the automatic SDATA_IN redirection for AMR and MDC applications. When the PRIMARY_DN# pin is grounded, and the codec is operating as a secondary, the SDATA_IN0 pin will be in a high impedance state, and the SDATA_IN1 pin will be active. If the PRIMARY_DN# pin is left floating, the codec SDATA_IN data will always be output from the SDATA_IN0 pin, and the SDATA_IN1 pin will be in a high impedance state. If the codec is operating as the primary in the system, the SDATA_IN0 output will always be active.

PRIMARY_DN# Output Mode - The PRIMARY_DN# pin will be driven to logic low when the codec is placed in primary mode by allowing the CIDx pins to float, or if they are both tied to logic high. The PRIMARY_DN# pin can be connected directly to the AMR PRIMARY_DN# connector pin when the codec is installed on the motherboard. The codec will pull the AMR connector pin low when configured as the primary audio codec. If the codec is disabled by holding the ENABLE pin at logic low, the PRIMARY_DN# pin of the codec will float high. This allows the motherboard codec to be disabled, and an AMR audio codec to be assigned the primary status. If the codec is operating as a secondary codec, the PRIMARY_DN# will float high.

8.3 Enable Operation

The ENABLE pin is typically left floating. If the ENABLE pin is grounded, the codec will be disabled and all the outputs except MONO_OUT will be placed in a high impedance mode. When ENABLE is grounded, the AC-Link signals will also be placed in a high impedance mode and the codec will not respond to AC-Link commands. The ENABLE pin is typically used to disable primary motherboard codecs when an audio enabled AMR or MDC card is installed. This allows the AMR/MDC codec to operate as the primary codec. When ENABLE is grounded, the PC_BEEP signal will be routed to MONO_OUT, and can be subsequently routed to the AMR codec PC_BEEP input via the AMR connector for simplified codec selection. When ENABLE is grounded, the PRIMARY_DN# pin will float indicating that there is no active primary codec on the motherboard.

9. AC TIMING CHARACTERISTICS

($T_{ambient}$ = 25 °C, AVdd = DVdd = 5.0V or 3.3V ± 5%, AVss=DVss+0V; 50pF external load)

9.1 Cold Reset

Figure 14. Cold Reset

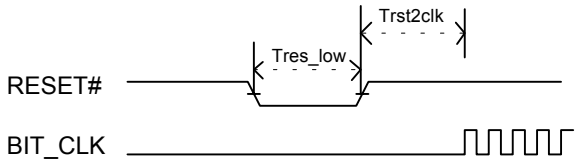


Table 25. Cold Reset

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
RESET# active low pulse width	Tres_low	1.0	-	-	us
RESET# inactive to BIT_CLK startup delay	Trst2clk	162.8	-	-	ns

# denotes active low.

9.2 Warm Reset

Figure 15. Warm Reset

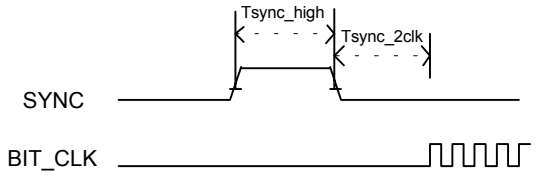


Table 26. Warm Reset

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SYNC active high pulse width	Tsync_high	1.0	1.3	-	us
SYNC inactive to BIT_CLK startup delay	Tsync2clk	162.8	-	-	ns

9.3 Clocks

Figure 16. Clocks

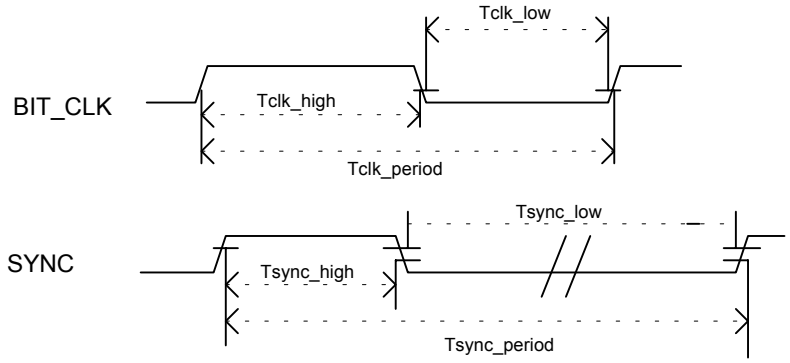


Table 27. Clocks

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
BIT_CLK frequency		-	12.288	-	MHz
BIT_CLK period	Tclk_period	-	81.4	-	ns
BIT_CLK output jitter		-	-	750	ps
BLT_CLK high pulsewidth (note 1)	Tclk_high	36	40.7	45	ns
BIT_CLK low pulse width (note 1)	Tclk_low	36	40.7	45	ns
SYNC frequency		-	48.0	-	kHz
SYNC period	Tsync_period	-	20.8	-	us
SYNC high pulse width	Tsync_high	-	1.3	-	us
SYNC low_pulse width	Tsync_low	-	19.5	-	us

Notes: 1) Worst case duty cycle restricted to 44/56.

9.4 Data Setup and Hold

(50pF external load)

Figure 17. Data Setup and Hold

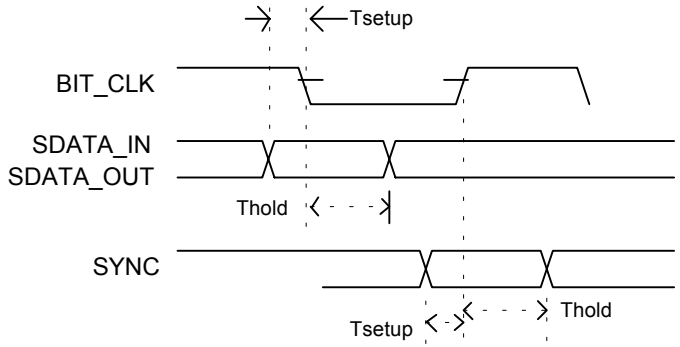


Table 28. Data Setup and Hold

Parameter	Symbol	Min	Typ	Max	Units
Setup to falling edge of BIT_CLK	Tsetup	10.0	-	-	ns
Hold from falling edge of BIT_CLK	Thold	10.0	-	-	ns

Note 1: Setup and hold time parameters for SDATA_IN are with respect to the AC'97 controller.

9.5 Signal Rise and Fall Times

(50pF external load; from 10% to 90% of Vdd)

Figure 18. Signal Rise and Fall Times

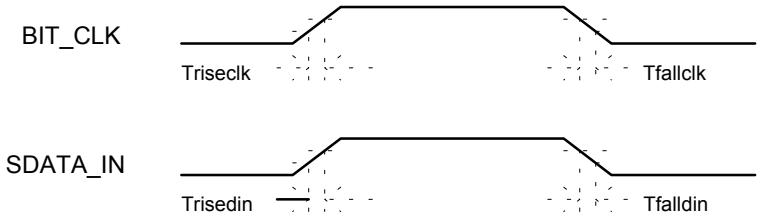


Table 29. Signal Rise and Fall Times

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
BIT_CLK rise time	Triseclk	2	-	6	ns
BIT_CLK fall time	Tfallclk	2	-	6	ns
SDATA_IN rise time	Trisedin	2	-	6	ns
SDATA_IN fall time	Tfalldin	2	-	6	ns

9.6 AC-Link Low Power Mode Timing

Figure 19. AC-Link Low Power Mode Timing

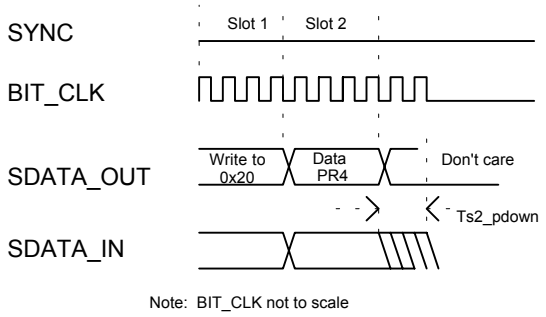


Table 30. AC-Link Low Power Mode Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
End of Slot 2 to BIT_CLK, SDATA_IN low	Ts2_pdown	-	-	1.0	us

9.7 ATE Test Mode

Figure 20. ATE Test Mode

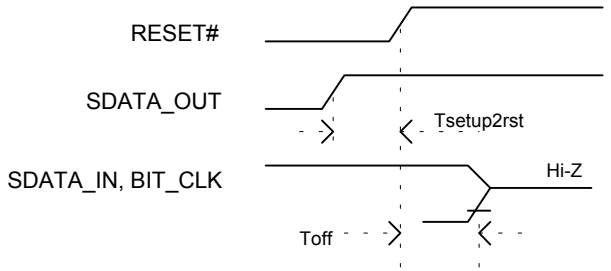


Table 31. ATE Test Mode

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Setup to trailing edge of RESET# (also applies to SYNC)	Tsetup2rst	15.0	-	-	ns
Rising edge of RESET# to Hi-Z delay	Toff	-	-	25.0	ns

Notes:

1. All AC-Link signals are normally low through the trailing edge of RESET#. Bringing SDATA_OUT high for the trailing edge of RESET# causes **STAC9744**'s AC-Link outputs to go high impedance which is suitable for ATE in circuit testing.
2. Once either of the two test modes have been entered, the **STAC9744** must be issued another RESET# with all AC-Link signals low to return to the normal operating mode.

 # denotes active low.

10. ELECTRICAL SPECIFICATIONS:

10.1 Absolute Maximum Ratings:

Voltage on any pin relative to Ground	Vss - 0.3V TO Vdd + 0.3V
Operating Temperature	0 ^{O}C TO 70 ^{O} C
Storage Temperature	-55 ^{O}C TO +125 ^{O} C
Soldering Temperature	260 ^{O}C FOR 10 SECONDS
Output Current per Pin	± 4 mA except Vrefout = ± 5mA

10.2 Recommended Operating Conditions

Table 32. Operating Conditions

PARAMETER		MIN	TYP	MAX	UNITS
Power Supplies	+ 3.3V Digital	3.135	3.3	3.465	V
	+ 5V Digital	4.75	5	5.25	V
	+ 5V Analog	4.75	5	5.25	V
	+ 3.3V Analog	3.135	3.3	3.465	V
Ambient Temperature		0	-	70	^{O}C

10.3 Power Consumption

Table 33: Power Consumption at Default Analog Current

PARAMETER	MIN	TYP	MAX	UNITS
Digital Supply Current				
+ 5V Digital: DAC and ADC Active		30		mA
+ 3.3V Digital: DAC and ADC Active		23		mA
+ 3.3V Digital: DAC and ADC Muted		7		mA
Analog Supply Current				
+ 5V Analog: PC_BEEP Muted		39		mA
+ 3.3V Analog: PC_BEEP Muted		37		mA
Power Down Status				
PR0 +5V Analog Supply Current		29		mA
PR1 +5V Analog Supply Current		39		mA
PR2 +5V Analog Supply Current		29		mA
PR3 +5V Analog Supply Current		0.6		mA
PR0,1,2,3 +5V Analog Supply Current		0.6		mA
PR4 +3.3V Digital Supply Current		0.1		mA
PR4 +5V Digital Supply Current		0.1		mA
PR5 No Effect				

Table 34: **Power Consumption at 3.3V Analog, Low Current Mode***

PARAMETER	MIN	TYP	MAX	UNITS
Digital Supply Current				
+ 3.3V Digital with DAC and ADC Active		23		mA
+ 3.3V Digital with DAC and ADC Muted		5		mA
Analog Supply Current				
+ 3.3V Analog with DAC and ADC Muted		21		mA
Power Down Status				
PR0 +3.3V Analog Supply Current		16		mA
PR1 +3.3V Analog Supply Current		21		mA
PR2 +3.3V Analog Supply Current		16		mA
PR3 +3.3V Analog Supply Current		0.4		mA
PR0,1,2,3 +3.3V Analog Supply Current		0.4		mA
PR4 +3.3V Digital Supply Current		0.1		mA
PR5 No Effect				

* -50% Analog Current Setting (Recommended for 3.3V Analog only): Register 70h=ABBAh, 72h=0002h

Table 35: Reduced Analog Power Settings Typical Supply Current

Condition	3.3V Analog	5V Analog
Default Analog Current		
Reset	36	38
All Un-Muted	77	84
ADC, LINE Thru, PC_BEEP active	57	63
DAC, LINE Thru, PC_BEEP active	52	56
All but DAC and ADC	43	45
-25% Analog Current		
Reset	29	31
All Un-Muted	62	70
ADC, LINE Thru, PC_BEEP active	46	52
DAC, LINE Thru, PC_BEEP active	42	45
All but DAC and ADC	34	36
-50% Analog Current		
Reset	20	This Setting Not
All Un-Muted	45	Recommended
ADC, LINE Thru, PC_BEEP active	33	
DAC, LINE Thru, PC_BEEP active	29	
All but DAC and ADC	24	
+25% Analog Current		
Reset	42	45
All Un-Muted	89	96
ADC, LINE Thru, PC_BEEP active	66	72
DAC, LINE Thru, PC_BEEP active	61	65
All but DAC and ADC	50	53

10.4 AC-Link Static Digital Specifications

($T_{ambient}$ = 25 ^{O}C, DVdd = 5.0V or 3.3V ± 5%, AVss=DVss=0V; 50pF external load)

Table 36. AC-Link Static Specifications

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input Voltage Range	Vin	-0.30		DVdd + 0.30	V
Low level input range	Vil	-	-	0.35xDVdd	V
High level input voltage	Vih	0.65xDVdd	-	-	V
High level output voltage	Voh	0.90xDVdd	-	-	V
Low level output voltage	Vol	-	-	0.1xDVdd	V
Input Leakage Current (AC-Link inputs)	-	-10	-	10	uA
Output Leakage Current (Hi-Z'd AC-Link outputs)	-	-10	-	10	uA
Output buffer drive current	-	-	5		mA

10.5STAC9744 +5V Analog Performance Characteristics

($T_{ambient}$ = 25 ^{O}C, AVdd = 5.0V ± 5%, DVdd = 3.3V ± 5%, AVss=DVss=0V; 1 kHz input sine wave; Sample Frequency = 48 kHz; 0 dB = 1 Vrms, 10KΩ/50pF load, Testbench Characterization BW: 20 Hz – 20 kHz, 0 dB settings on all gain stages)

Table 37. Analog Performance Characteristics

PARAMETER	MIN	TYP	MAX	UNITS
Full Scale Input Voltage:				
Line Inputs	-	1.0	-	Vrms
Mic Inputs[1]	-	0.1	-	Vrms
Full Scale Output Voltage:				
Line Output 5V	-	1.0	-	Vrms
Analog S/N:				
CD to LINE_OUT 5V	90	102	-	dB
Other to LINE_OUT 5V	-	102	-	dB
Analog Frequency Response[2]	20	-	20,000	Hz
Digital S/N[3]				
D/A 5V	85	96	-	dB
A/D 5V	75	86	-	dB
Total Harmonic Distortion:				
Line Output[4]	-	-	0.02	%
D/A & A/D Frequency Response[5]	20	-	19,200	Hz
Transition Band	19,200	-	28,800	Hz
Stop Band	28,800	-	∞	Hz
Stop Band Rejection[6]	+85	-	–	dB
Out-of-Band Rejection[7]	-	+40	–	dB
Group Delay	-	-	1	ms
Power Supply Rejection Ratio (1kHz)	-	+40	–	dB
Crosstalk between Input channels	-	-	-70	dB
Spurious Tone Rejection	-	+100	–	dB
Attenuation, Gain Step Size	-	1.5	–	dB
Input Impedance	10	-	–	KΩ
Input Capacitance	-	15	–	pF

Vrefout	-	0.5 x AVdd	–	V
Interchannel Gain Mismatch ADC			0.5	dB
Interchannel Gain Mismatch DAC		-	0.5	dB
Gain Drift		100		ppm/deg. C
DAC Offset Voltage		10	50	mV
Deviation from Linear Phase			1	degree
External Load Impedance	10			K ohm
Mute Attenuation (Vrms input)	90	96		dB

Notes:

1. With +20 dB Boost on, 1.0Vrms with Boost off
2. ± 1 dB limits
3. The ratio of the rms output level with 1 kHz full scale input to the rms output level with all zeros into the digital input. Measured "A weighted" over a 20 Hz to a 20 kHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
4. 0 dB gain, 20 kHz BW, 48 kHz Sample Frequency
5. ± 0.25dB limits
6. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
7. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 kHz, with respect to a 1 Vrms DAC output.

10.6 STAC9745 +3.3V Analog Performance Characteristics

($T_{ambient}$ = 25 ^{O}C, AVdd = DVdd = 3.3V ± 5%, AVss=DVss=0V; 1 kHz input sine wave; Sample Frequency = 48 kHz; 0 dB = 1 Vrms, 10KΩ/50pF load, Testbench Characterization BW: 20 Hz – 20 kHz, 0 dB settings on all gain stages)

Table 38. Analog Performance Characteristics

PARAMETER	MIN	TYP	MAX	UNITS
Full Scale Output Voltage:				
Line Inputs to line output 3.3V	-	0.7	-	Vrms
Line Inputs to LINE_OUT 3.3V @ Line In = 1 Vrms and @ Gain setting of -6 dB		0.7		Vrms
Line Inputs to LINE_OUT 3.3V @ Line In = 0.5 Vrms and @ gain setting of 0dB		0.7		Vrms
PCM to LINE_OUT 3.3V @ full scale PCM input @PCM gain setting of 0dB		0.7		Vrms
PCM to Line Output 3.3V				
MIC Inputs to LINE_OUT 3.3V @ MIC In = 1 Vrms and @ gain setting of 0dB		0.7		Vrms
Analog S/N:				
CD to LINE_OUT 3.3V	-	101	-	dB
Other to LINE_OUT 3.3V		101		dB
Analog Frequency Response[2]	20	-	20,000	Hz
Digital S/N[3]				
D/A 3.3V	85	95	-	dB
A/D 3.3V	75	85	-	dB
Total Harmonic Distortion:				
Line Output[4]	-	-	0.02	%
D/A & A/D Frequency Response[5]	20	-	19,200	Hz
Transition Band	19,200	-	28,800	Hz
Stop Band	28,800	-	∞	Hz
Stop Band Rejection[6]	+85	-	–	dB
Out-of-Band Rejection[7]	-	+40	–	dB
Group Delay	-	-	1	ms
Power Supply Rejection Ratio (1kHz)	-	+40	–	dB
Crosstalk between Input channels	-	-	-70	dB
Spurious Tone Rejection	-	+100	–	dB

Attenuation, Gain Step Size	-	1.5	–	dB
Input Impedance	10	-	–	KΩ
Input Capacitance	-	15	–	pF
Vrefout	-	0.5 x AVdd	–	V
Interchannel Gain Mismatch ADC			0.5	dB
Interchannel Gain Mismatch DAC		-	0.5	dB
Gain Drift		100		ppm/ ^{O}C
DAC Offset Voltage		10	50	mV
Deviation from Linear Phase			1	degree
External Load Impedance	10			KΩ
Mute Attenuation (0 dB)	90	96		dB

Notes:

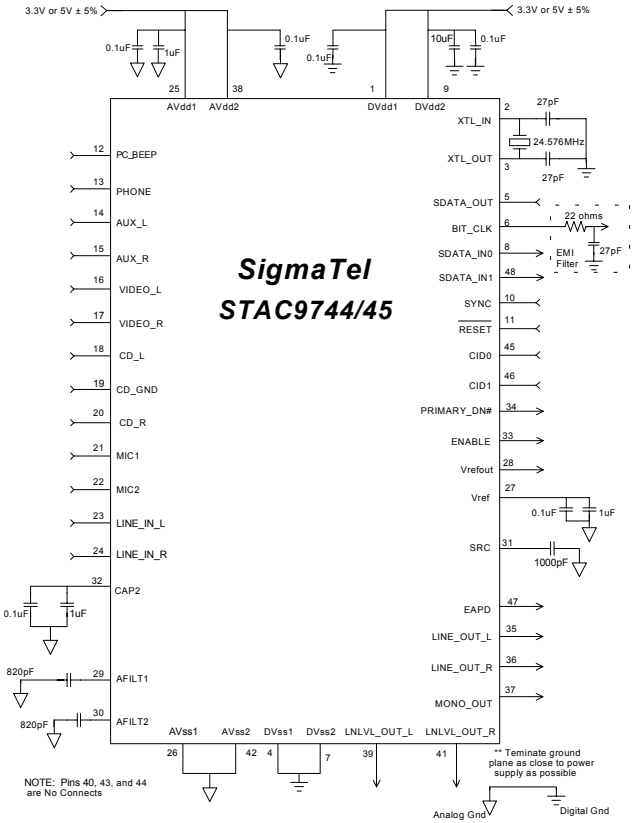
1. With +20 dB Boost on, 1.0Vrms with Boost off
2. ± 1 dB limits
3. The ratio of the rms output level with 1 kHz full scale input to the rms output level with all zeros into the digital input. Measured "A weighted" over a 20 Hz to a 20 kHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
4. 0 dB gain, 20 kHz BW, 48 kHz Sample Frequency
5. ± 0.25dB limits
6. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
   The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 kHz, with respect to a 1 Vrms DAC output.

Appendix A

SPLIT INDEPENDENT POWER SUPPLY OPERATION

In PC applications, one power supply input to the **STAC9744** may be derived from a supply regulator (as shown in Figure 3) and the other directly from the PCI power supply bus. When power is applied to the PC, the regulated supply input to the IC will be applied some time delay after the PCI power supply. Without proper on-chip partitioning of the analog and digital circuitry, some manufacturer's codecs would be subject to on-chip SCR type latch-up.

SigmaTel's **STAC9744** specifically allows power-up sequencing delays between the analog (AVddx) and digital (VDddx) supply pins. These two power supplies can power-up independently and at different rates with no adverse effects to the codec. The IC is designed with independent analog and digital circuitry that prevents on-chip SCR type latch-up.



Appendix B

+5.0V/+3.3V POWER SUPPLY OPERATION NOTES

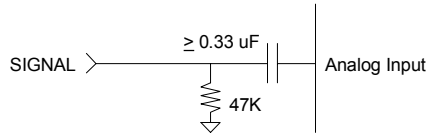
The **STAC9744** is capable of operating from a single 5V supply connected to both DVdd and Avdd. When operating with a +5V digital supply, all digital AC-Link interface signals should be at a 5V level. If digital interface signals below 5V are used with a +5V digital supply, then appropriate level shifting circuitry may be needed to ensure adequate digital noise immunity.

The **STAC9744** can also operate from a +3.3V digital supply connected to DVdd while maintaining a 5V analog supply on AVdd. On-chip level shifters ensure accurate logic transfers between the analog and digital portions of the **STAC9744**. If digital interface signals above +3.3V are used (i.e. a +5V AC-Link interface), appropriate level shifting circuitry must be provided to prevent on-chip ESD protection diodes from turning on. (See Appendixes A concerning SPLIT INDEPENDENT POWER SUPPLY OPERATION).

The **STAC9745** must be run from a +3.3V supply connected to both DVdd and AVdd. If digital interface signals above +3.3V are used (i.e. a +5V AC-Link interface), then appropriate level shifting circuitry must be provided to prevent on-chip ESD protection diodes from turning on.

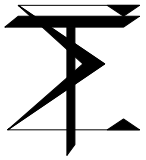
***Always operate the STAC97xx digital supply from the same supply voltage as the digital controller supply.**

***All the analog inputs must be ac-coupled with a capacitor of 0.33 uF or greater. It is recommended that a resistor of about 47KΩ be connected from the signal side of the capacitor to analog GND as shown below.**



***All the analog outputs must be ac-coupled. If an external amplifier is used, make sure that the input impedance of the amplifier is at least 10KΩ and use an ac-coupling capacitor of +2 uF or greater to maintain the minimum PC99 20 Hz low-frequency bandwidth.**

For more information, please contact:



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