STAP1011-180

RF power transistor the LdmoST family, N-channel enhancement-mode lateral MOSFETs

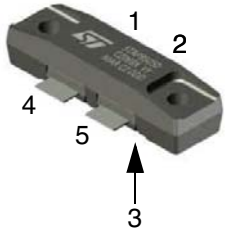
Features

- Excellent thermal stability
- Common source configuration push-pull
- P_{OUT} = 180W with 10 dB gain @ 1030 MHz 36 V/100 µsec - 10%
- Plastic package
- In compliance with the 2002/95/EC european directive

Description

The STAP1011-180 is a common source N-channel enhancement-mode lateral field-effect RF power transistor. It is designed for 1030-1090 MHz avionics applications.
STAP1011-180 is mounted in STAP ST advanced PowerSO-10RF package.
The STAP package was designed to offer high reliability and power capability. It has been specially optimized for RF needs and offers excellent RF performances and ease of assembly.

Figure 1. Pin connection



1, 2 Drain

3 Source

4, 5 Gate

Table 1. Device summary

Order code	Package	Packaging
STAP1011-180	STAP2	Tube

1 Electrical data

1.1 Maximum ratings

T_{CASE} = 25 °C

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain-source voltage	65	V
V_{GS}	Gate-source voltage	±20	V
P_{DISS}	Power dissipation (@ Tc = 70 °C)	800	W
T_J	Max. operating junction temperature	165	°C
T_{STG}	Storage temperature	-65 to + 150	°C

1.2 Thermal data

Table 3. Thermal data (CW)

Symbol	Parameter	Value	Unit
R_{thJC}	Junction - case thermal resistance	0.10	°C/W

2 Electrical characteristics

T_{CASE} = +25 °C

2.1 Static

Table 4. Static (per side)

Symbol	Test conditions			Min	Typ	Max	Unit
$V_{(BR)DSS}$	V_{GS} = 0 V	I_{DS} = 1 mA		65			V
I_{DSS}	V_{GS} = 0 V	V_{DS} = 28 V				1	µA
I_{GSS}	V_{GS} = 20 V	V_{DS} = 0 V				1	µA
$V_{GS(Q)}$	V_{DS} = 28 V	I_D = 100 mA		2.0		4.0	V
$V_{DS(ON)}$	V_{GS} = 10 V	I_D = 3 A			0.7	0.9	V
G_{FS}	V_{DS} = 10 V	I_D = 3 A			3		S
ΔV_{TH} (1)	I_D = 100 mA					100	mV
C_{ISS}	V_{GS} = 0 V	V_{DS} = 28 V	f = 1 MHz		83		pF
C_{OSS}	V_{GS} = 0 V	V_{DS} = 28 V	f = 1 MHz		58		pF
C_{RSS}	V_{GS} = 0 V	V_{DS} = 28 V	f = 1 MHz		3.0		pF

1. Absolute VGS difference between side 1 and side 2 of the device

2.2 Dynamic

Table 5. Dynamic

Symbol	Test conditions	Min	Typ	Max	Unit
P_{OUT}	V_{DD} = 36 V I_{DQ} = 300 mA f = 1030 MHz	180	195	-	W
G_{PS}	V_{DD} = 36 V I_{DQ} = 300 mA P_{OUT} = 180 W f = 1030 MHz	10		-	dB
h_D	V_{DD} = 36 V I_{DQ} = 300 mA P_{OUT} = 180 W f = 1030 MHz	45	50	-	%
Load mismatch	V_{DD} = 36 V I_{DQ} = 300 mA P_{OUT} = 180 W f = 1030 MHz All phase angles	10:1		-	VSWR
Rise time	V_{DD} = 36 V I_{DQ} = 300 mA P_{OUT} = 180 W f = 1030 MHz		40	100	nsec
Fall time	V_{DD} = 36 V I_{DQ} = 300 mA P_{OUT} = 180 W f = 1030 MHz		25	100	nsec
Power drop	V_{DD} = 36 V I_{DQ} = 300 mA P_{OUT} = 180 W f = 1030 MHz		0.3	0.5	dB

3 Impedance

Figure 2. Current conventions

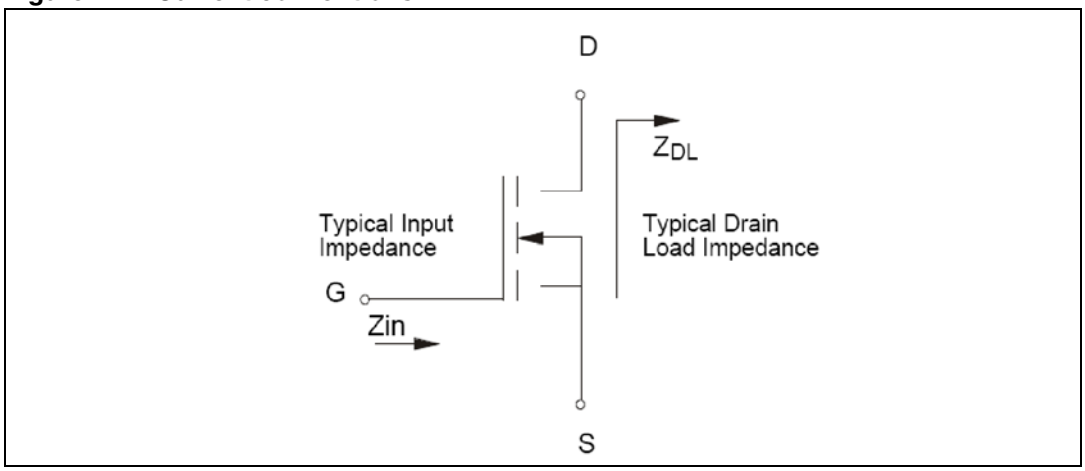


Table 6. Impedance data

Freq. (MHz)	Z_{IN} (Ω)	Z_{DL}(Ω)
1030 MHz	TBD	TBD

Note: Measured gate to gate and drain to drain respectively.

4 Typical performance

Figure 3. Output power & efficiency vs input power

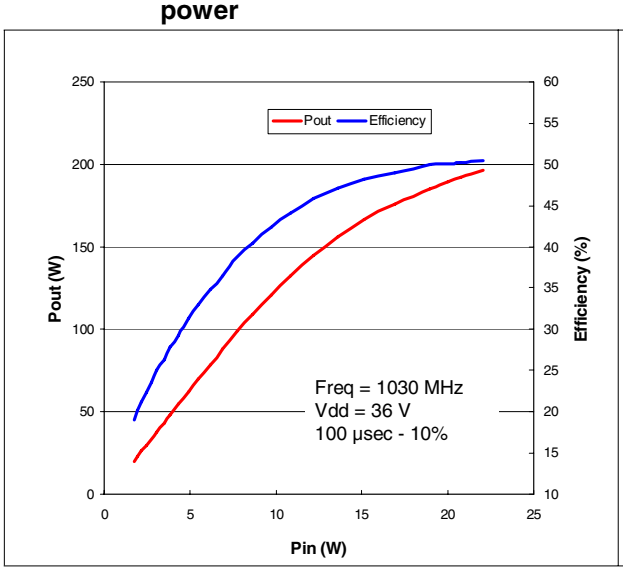


Figure 4. Gain vs output power & bias current

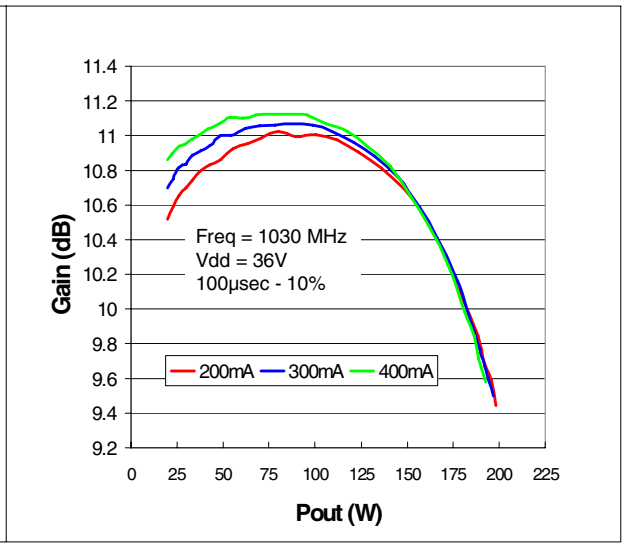
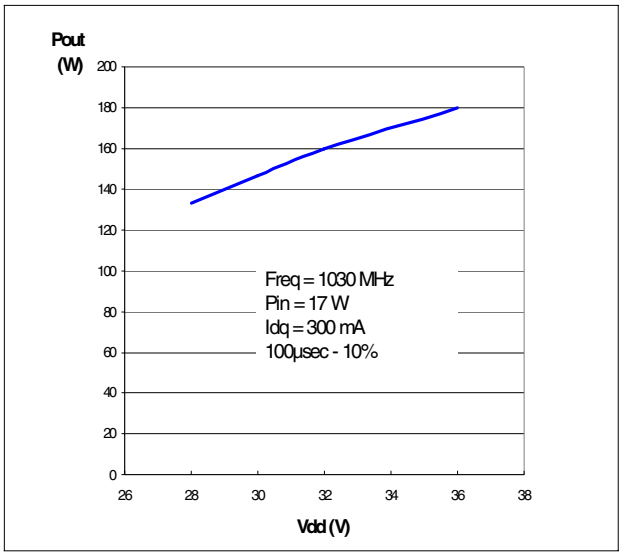


Figure 5. Output power vs drain voltage



5 Package mechanical data

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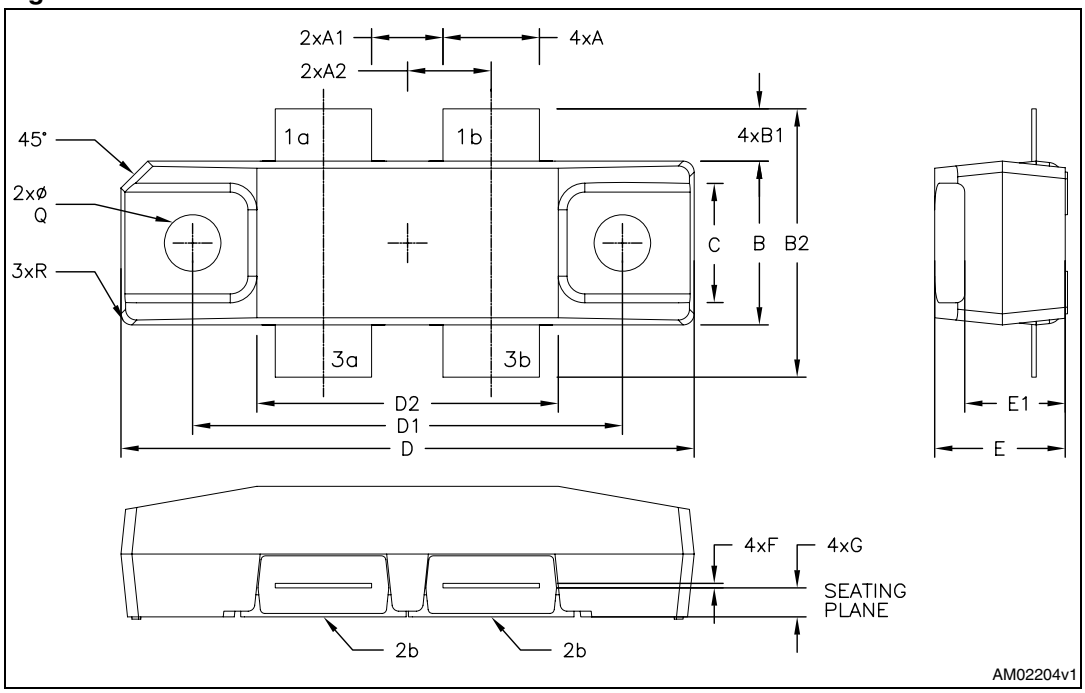
Table 7. STAP2 mechanical data

Dim	mm			inch		
	Min	Typ	Max	Min	Typ	Max
A	5.40		5.65	0.212		0.222
A1	3.89		4.29	0.153		0.169
A2	4.70		4.90	0.185		0.193
B	9.27		9.53	0.365		0.375
B1	2.90		3.10	0.114		0.122
B2	15.10		15.65	0.594		0.616
C	6.60		6.99	0.260		0.275
D	32.74		33.05	1.289		1.301
D1	24.51		24.82	0.965		0.977
D2	17.15		17.45	0.675		0.687
E	7.42		7.57	0.292		0.298
E1	5.69		5.84	0.224		0.230
F	0.21		0.31	0.008		0.012
G	1.62		1.68	0.064		0.068
Q	3.15		3.30	0.124		0.130
R	0.64			0.025		

Figure 6. STAP2 mechanical data



6 Revision history

Table 8. Document revision history

Date	Revision	Changes
07-May-2009	1	Initial release

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