

N-channel 800 V, 0.55 Ω typ., 8 A MDmesh™ K5 Power MOSFET in a D²PAK package

Datasheet - production data

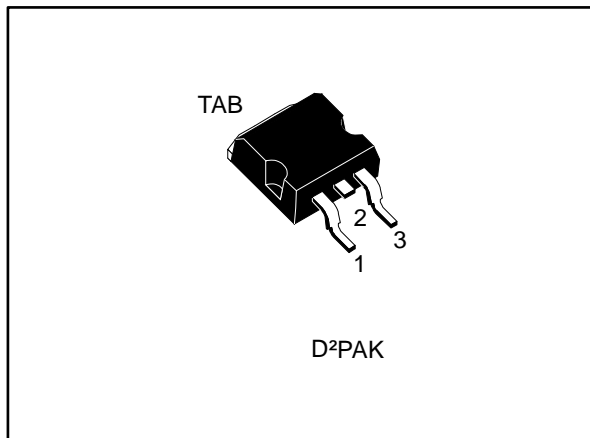


Figure 1: Internal schematic diagram

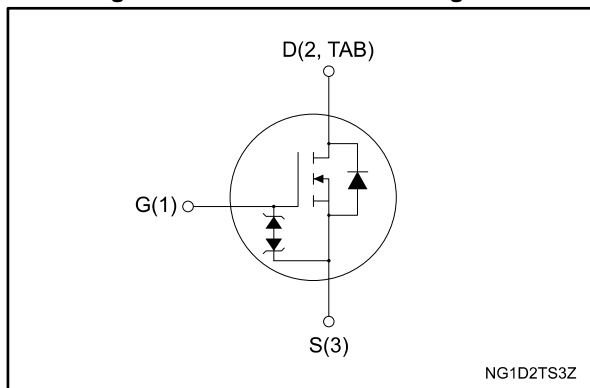


Table 1: Device summary

| Order code | Marking | Package | Packing |
|-------------|----------|--------------------|---------------|
| STB10LN80K5 | 10LN80K5 | D ² PAK | Tape and reel |

Features

| Order code | V _{DS} | R _{DS(on)} max. | I _D |
|-------------|-----------------|--------------------------|----------------|
| STB10LN80K5 | 800 V | 0.63 Ω | 8 A |

- Industry's lowest R_{DS(on)} x area
- Industry's best figure of merit (FoM)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

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1 Electrical ratings

Table 2: Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|---------------|---|-------------|------------------|
| V_{GS} | Gate-source voltage | ± 30 | V |
| I_D | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$ | 8 | A |
| I_D | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$ | 5 | A |
| $I_D^{(1)}$ | Drain current (pulsed) | 32 | A |
| P_{TOT} | Total dissipation at $T_C = 25\text{ }^\circ\text{C}$ | 110 | W |
| $dv/dt^{(2)}$ | Peak diode recovery voltage slope | 4.5 | V/ns |
| $dv/dt^{(3)}$ | MOSFET dv/dt ruggedness | 50 | |
| T_j | Operating junction temperature range | - 55 to 150 | $^\circ\text{C}$ |
| T_{stg} | Storage temperature range | | |

Notes:

⁽¹⁾Pulse width limited by safe operating area.

⁽²⁾ $I_{SD} \leq 8\text{ A}$, $di/dt \leq 100\text{ A}/\mu\text{s}$; $V_{DS\text{ peak}} < V_{(BR)DSS}$

⁽³⁾ $V_{DS} \leq 640\text{ V}$

Table 3: Thermal data

| Symbol | Parameter | Value | Unit |
|---------------------|----------------------------------|-------|---------------------------|
| $R_{thj-case}$ | Thermal resistance junction-case | 1.14 | $^\circ\text{C}/\text{W}$ |
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-pcb | 35 | $^\circ\text{C}/\text{W}$ |

Notes:

⁽¹⁾When mounted on FR-4 board of 1 inch², 2 oz Cu

Table 4: Avalanche characteristics

| Symbol | Parameter | Value | Unit |
|----------|--|-------|------|
| I_{AR} | Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax}) | 2.7 | A |
| E_{AS} | Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$) | 240 | mJ |

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified

Table 5: On/off-state

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|-----------------------------------|--|------|------|----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$ | 800 | | | V |
| I_{DSS} | Zero gate voltage drain current | $V_{GS} = 0\text{ V}$, $V_{DS} = 800\text{ V}$ | | | 1 | μA |
| | | $V_{GS} = 0\text{ V}$, $V_{DS} = 800\text{ V}$ $T_C = 125\text{ °C}$ | | | 50 | μA |
| I_{GSS} | Gate body leakage current | $V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$ | | | ± 10 | μA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = V_{GS}$, $I_D = 100\text{ }\mu\text{A}$ | 3 | 4 | 5 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$, $I_D = 4\text{ A}$ | | 0.55 | 0.63 | Ω |

Table 6: Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-------------------|---------------------------------------|--|------|------|------|----------|
| C_{iss} | Input capacitance | $V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$ | - | 427 | - | pF |
| C_{oss} | Output capacitance | | - | 43 | - | pF |
| C_{rss} | Reverse transfer capacitance | | - | 0.25 | - | pF |
| $C_{o(tr)}^{(1)}$ | Equivalent capacitance time related | $V_{DS} = 0\text{ to }640\text{ V}$, $V_{GS} = 0\text{ V}$ | - | 72 | - | pF |
| $C_{o(er)}^{(2)}$ | Equivalent capacitance energy related | | | | 27 | - |
| R_g | Intrinsic gate resistance | $f = 1\text{ MHz}$, $I_D = 0\text{ A}$ | - | 7 | - | Ω |
| Q_g | Total gate charge | $V_{DD} = 640\text{ V}$, $I_D = 8\text{ A}$ $V_{GS} = 10\text{ V}$ See Figure 16: "Test circuit for gate charge behavior" | - | 15 | - | nC |
| Q_{gs} | Gate-source charge | | - | 4.2 | - | nC |
| Q_{gd} | Gate-drain charge | | - | 9 | - | nC |

Notes:

⁽¹⁾Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

⁽²⁾Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7: Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------|---------------------|---|------|------|------|------|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD} = 400\text{ V}$, $I_D = 4\text{ A}$, $R_G = 4.7\text{ }\Omega$ $V_{GS} = 10\text{ V}$ See Figure 15: "Test circuit for resistive load switching times" and Figure 20: "Switching time waveform" | - | 11.8 | - | ns |
| t_r | Rise time | | - | 10 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 28 | - | ns |
| t_f | Fall time | | - | 13 | - | ns |

Table 8: Source-drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|--|------|------|------|---------------|
| I_{SD} | Source-drain current | | - | | 8 | A |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | - | | 32 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $I_{SD} = 8 \text{ A}$, $V_{GS} = 0 \text{ V}$ | - | | 1.5 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = 8 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 60 \text{ V}$ See <i>Figure 17: "Test circuit for inductive load switching and diode recovery times"</i> | - | 350 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 3.9 | | μC |
| I_{RRM} | Reverse recovery current | | - | 22.5 | | A |
| t_{rr} | Reverse recovery time | $I_{SD} = 8 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 60 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$ See <i>Figure 17: "Test circuit for inductive load switching and diode recovery times"</i> | - | 505 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 5 | | μC |
| I_{RRM} | Reverse recovery current | | - | 20 | | A |

Notes:

⁽¹⁾Pulse width limited by safe operating area

⁽²⁾Pulsed: pulse duration = 300 $\mu\text{ s}$, duty cycle 1.5%

Table 9: Gate-source Zener diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|-------------------------------|---|------|------|------|------|
| $V_{(BR)GSO}$ | Gate-source breakdown voltage | $I_{GS} = \pm 1 \text{ mA}$, $I_D = 0 \text{ A}$ | 30 | - | - | V |

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.2 Electrical characteristics (curves)

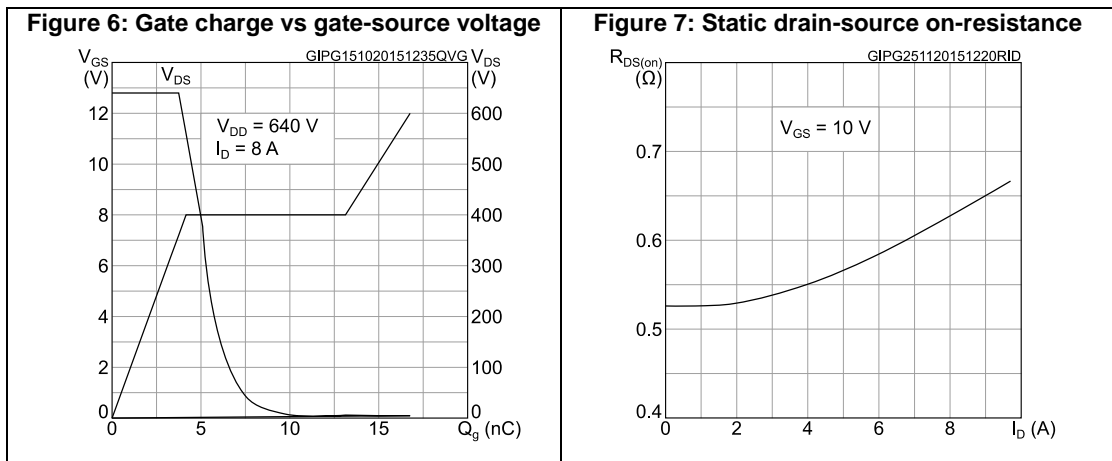
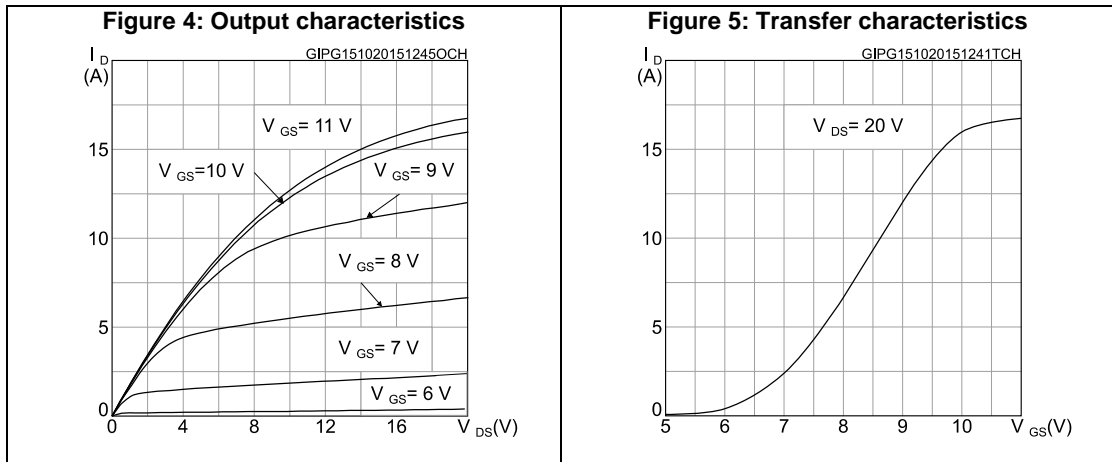
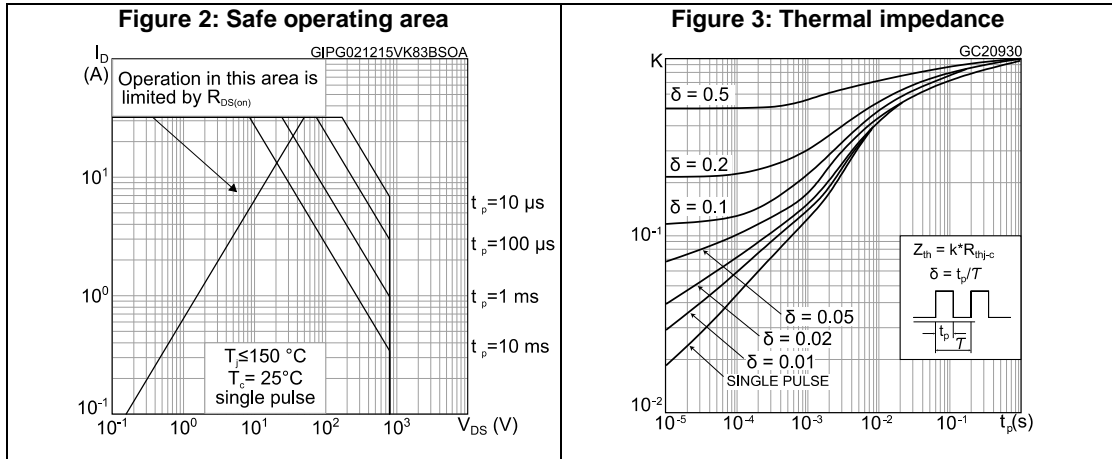


Figure 8: Capacitance variations

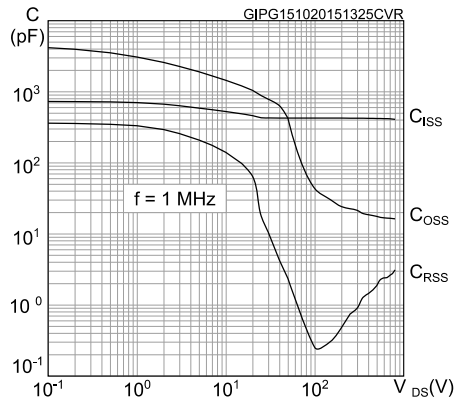


Figure 9: Normalized gate threshold voltage vs temperature

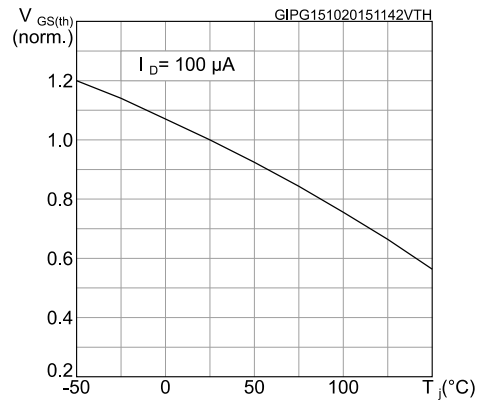


Figure 10: Normalized on-resistance vs temperature

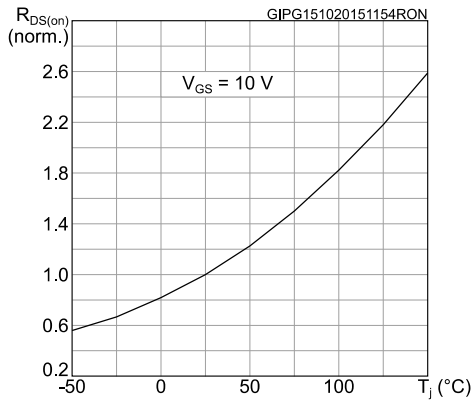


Figure 11: Normalized $V_{(BR)DSS}$ vs temperature

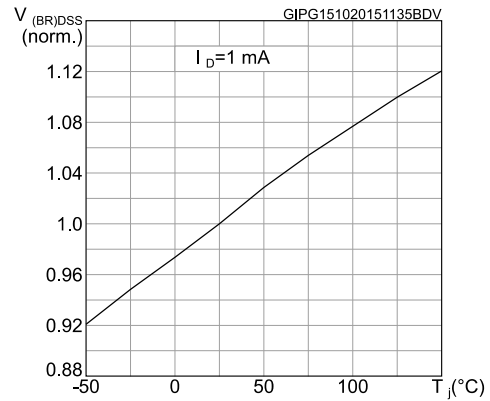


Figure 12: Output capacitance stored energy

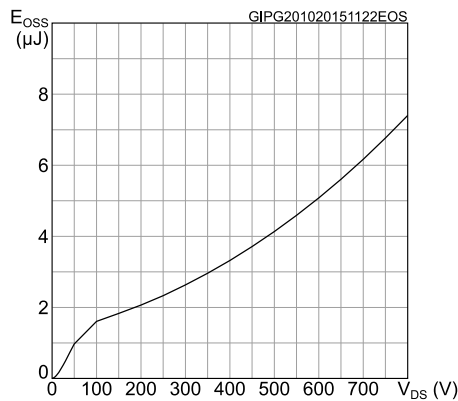


Figure 13: Source-drain diode forward characteristics

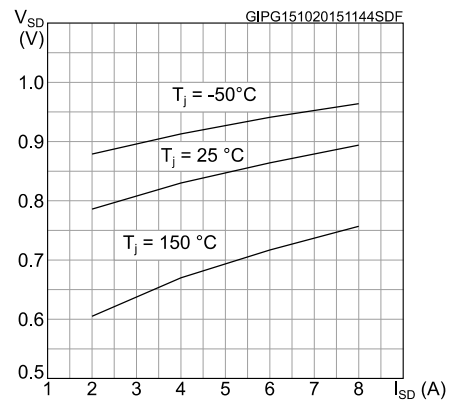
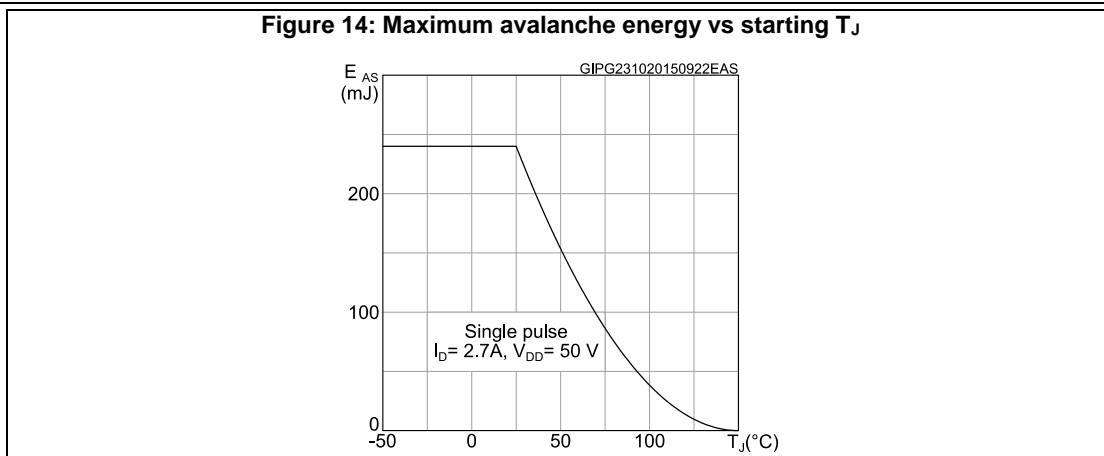


Figure 14: Maximum avalanche energy vs starting T_J



3 Test circuits

Figure 15: Test circuit for resistive load switching times



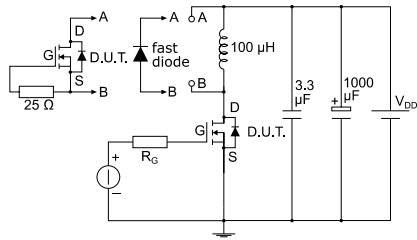
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Figure 16: Test circuit for gate charge behavior



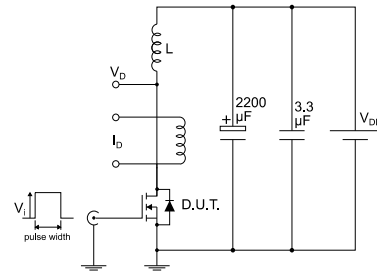
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Figure 17: Test circuit for inductive load switching and diode recovery times



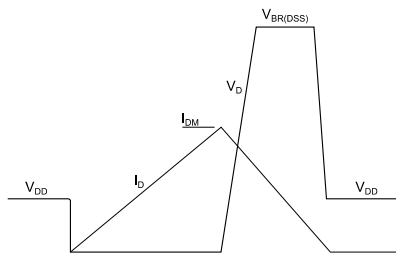
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Figure 18: Unclamped inductive load test circuit



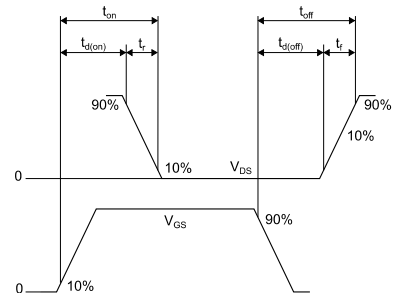
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Figure 19: Unclamped inductive waveform



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Figure 20: Switching time waveform



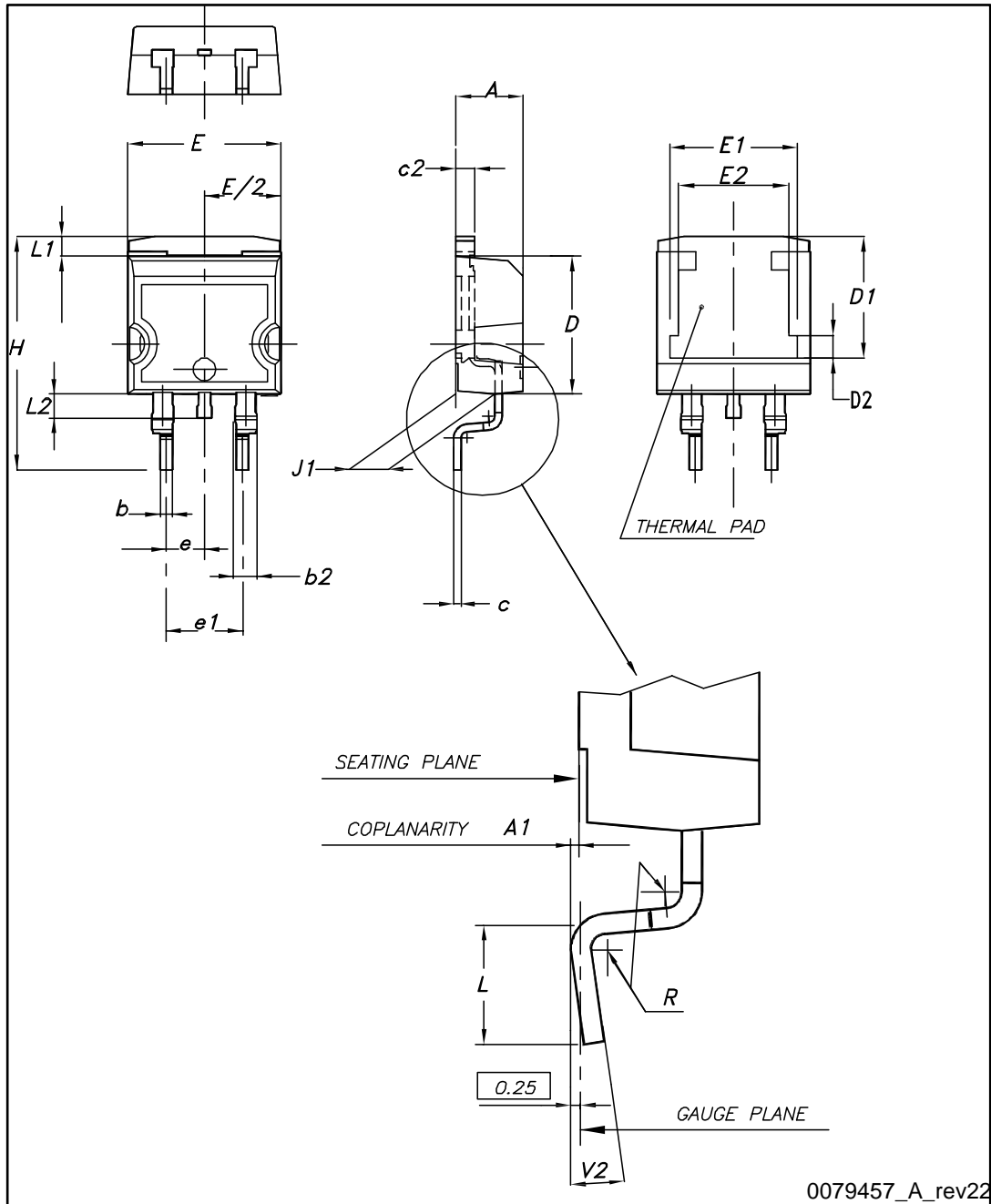
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 D²PAK package information

Figure 21: D²PAK (TO-263) type A package outline

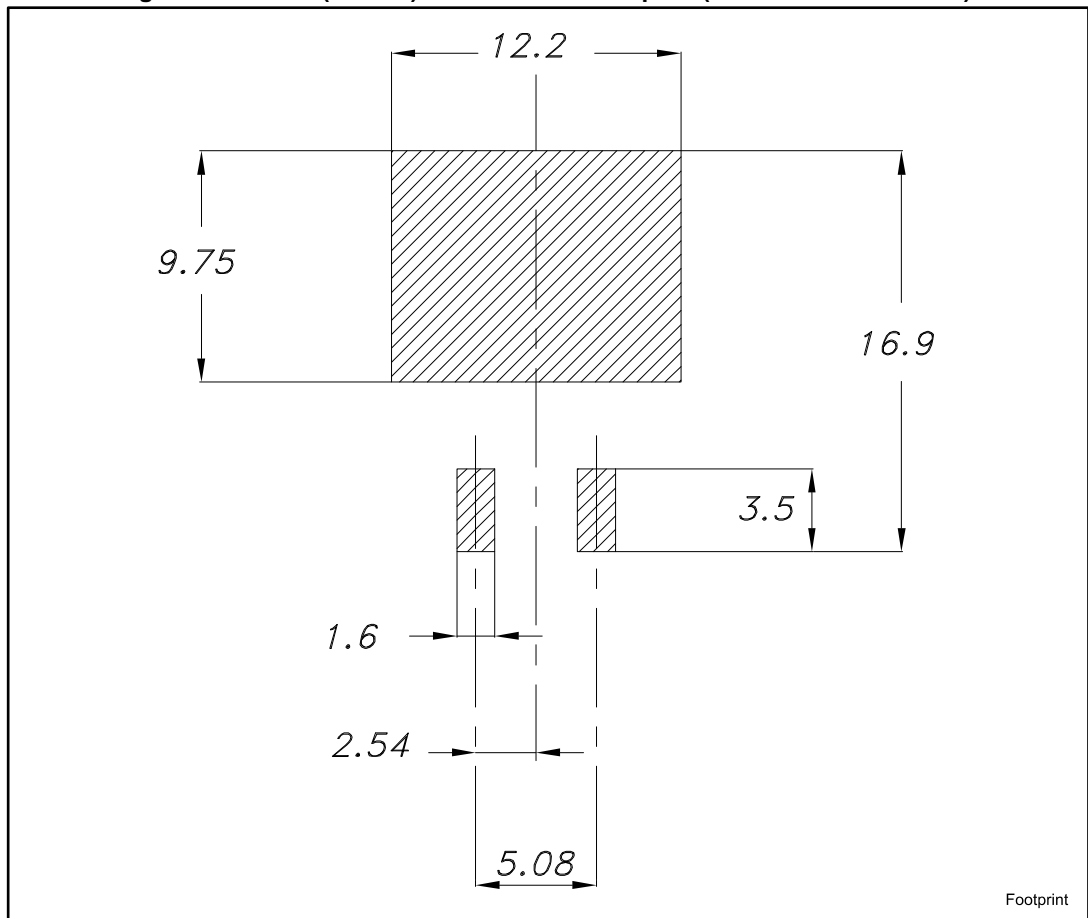


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Table 10: D²PAK (TO-263) type A package mechanical data

| Dim. | mm | | |
|------|------|------|-------|
| | Min. | Typ. | Max. |
| A | 4.40 | | 4.60 |
| A1 | 0.03 | | 0.23 |
| b | 0.70 | | 0.93 |
| b2 | 1.14 | | 1.70 |
| c | 0.45 | | 0.60 |
| c2 | 1.23 | | 1.36 |
| D | 8.95 | | 9.35 |
| D1 | 7.50 | 7.75 | 8.00 |
| D2 | 1.10 | 1.30 | 1.50 |
| E | 10 | | 10.40 |
| E1 | 8.50 | 8.70 | 8.90 |
| E2 | 6.85 | 7.05 | 7.25 |
| e | | 2.54 | |
| e1 | 4.88 | | 5.28 |
| H | 15 | | 15.85 |
| J1 | 2.49 | | 2.69 |
| L | 2.29 | | 2.79 |
| L1 | 1.27 | | 1.40 |
| L2 | 1.30 | | 1.75 |
| R | | 0.4 | |
| V2 | 0° | | 8° |

Figure 22: D²PAK (TO-263) recommended footprint (dimensions are in mm)



4.2 Packing information

Figure 23: Tape outline

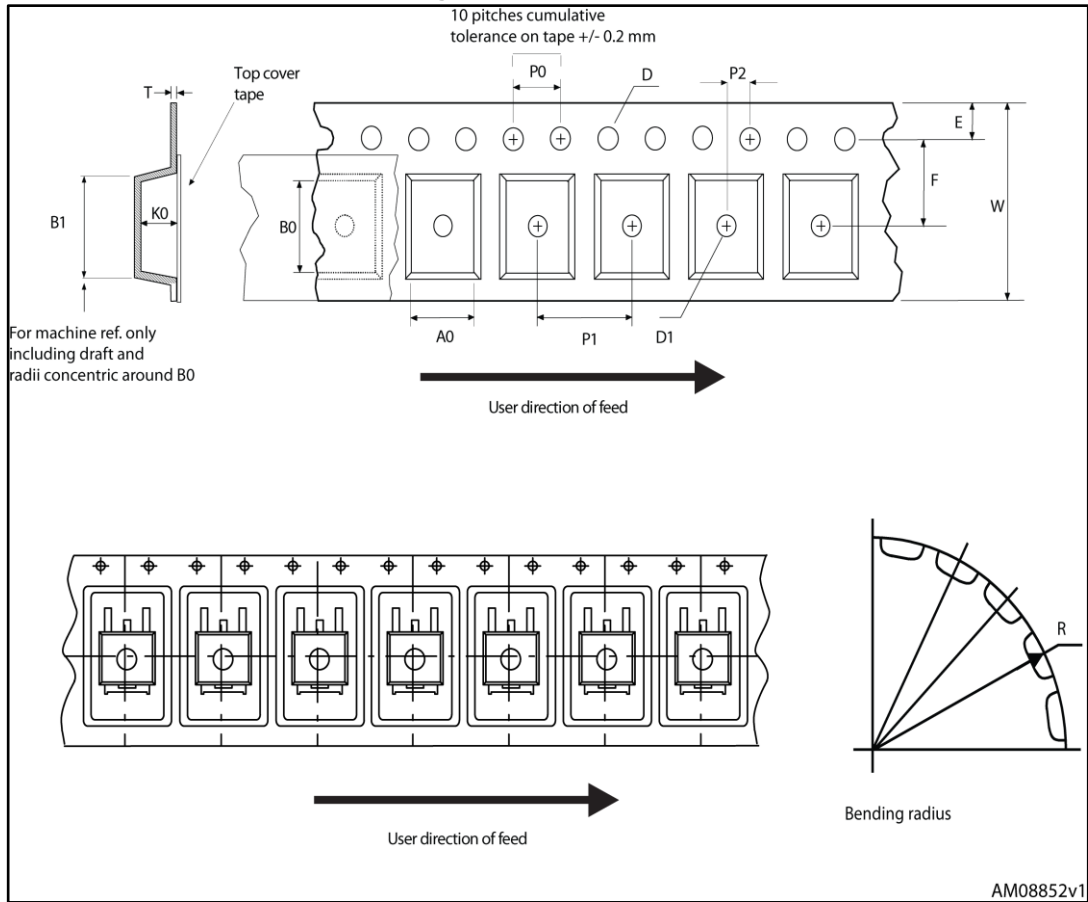


Figure 24: Reel outline

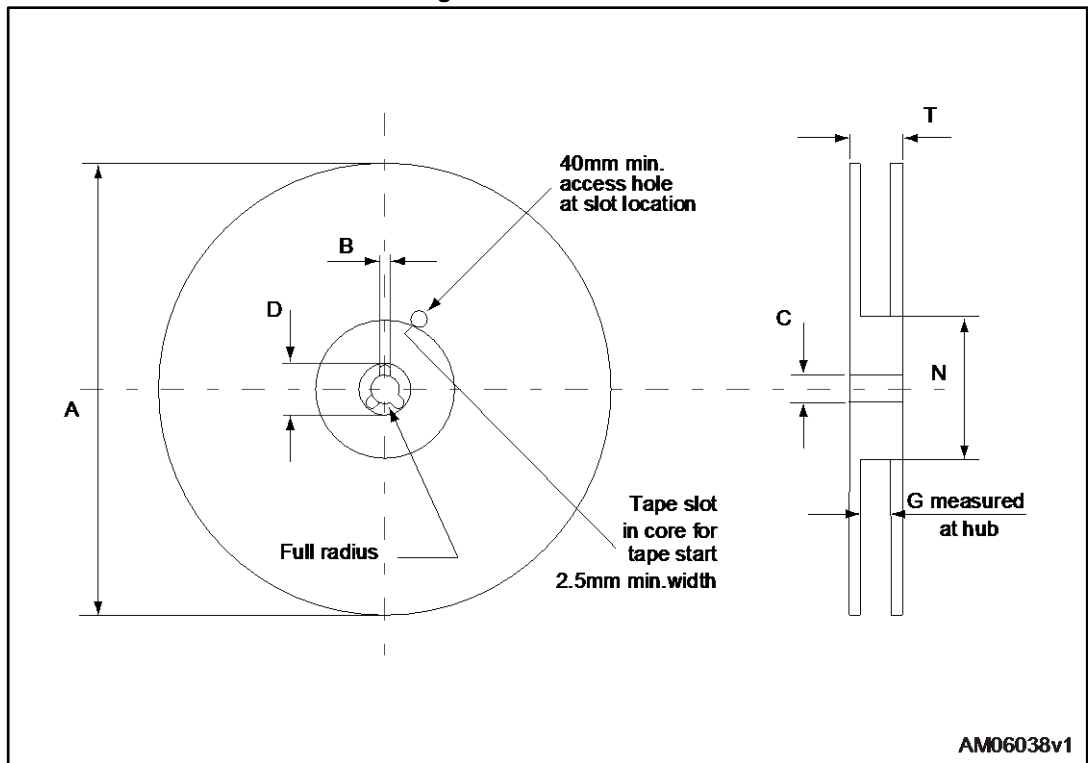


Table 11: D²PAK tape and reel mechanical data

| Tape | | | Reel | | |
|------|------|------|---------------|------|------|
| Dim. | mm | | Dim. | mm | |
| | Min. | Max. | | Min. | Max. |
| A0 | 10.5 | 10.7 | A | | 330 |
| B0 | 15.7 | 15.9 | B | 1.5 | |
| D | 1.5 | 1.6 | C | 12.8 | 13.2 |
| D1 | 1.59 | 1.61 | D | 20.2 | |
| E | 1.65 | 1.85 | G | 24.4 | 26.4 |
| F | 11.4 | 11.6 | N | 100 | |
| K0 | 4.8 | 5.0 | T | | 30.4 |
| P0 | 3.9 | 4.1 | | | |
| P1 | 11.9 | 12.1 | Base quantity | | 1000 |
| P2 | 1.9 | 2.1 | Bulk quantity | | 1000 |
| R | 50 | | | | |
| T | 0.25 | 0.35 | | | |
| W | 23.7 | 24.3 | | | |

5 Revision history

Table 12: Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 04-May-2015 | 1 | First release. |
| 08-Feb-2016 | 2 | Modified: <i>Table 2: "Absolute maximum ratings"</i> , <i>Table 3: "Thermal data"</i> , <i>Table 4: "Avalanche characteristics"</i> , <i>Table 5: "On/off-state"</i> , <i>Table 7: "Switching times"</i> and <i>Table 8: "Source-drain diode"</i> Added: <i>Section 3.1: "Electrical characteristics (curves)"</i> Datasheet promoted from preliminary data to production data Minor text changes |

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