STB16PF06L

P-CHANNEL 60V - 0.11Ω - 16A D2PAK
STripFET™ MOSFET

Table 1: General Features

TYPE	V_{DSS}	$R_{DS(on)}$	I_D	Pw
STB16PF06L	60 V	< 0.125 Ω	16 A	70 W

- TYPICAL R_{DS}(on) = 0.11 Ω
- LOW THRESHOLD DEVICE
- LOW GATE CHARGE

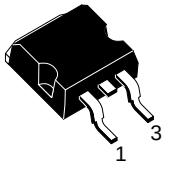
DESCRIPTION

This MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalance characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- MOTOR CONTROL
- DC-DC CONVERTERS

Figure 1: Package



D^2PAK
TO-263

Figure 2: Internal Schematic Diagram

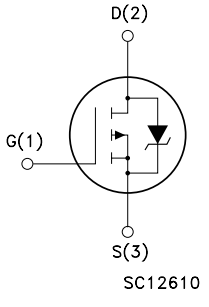


Table 2: Order Codes

PART NUMBER	MARKING	PACKAGE	PACKAGING
STB16PF06LT4	B16PF06L	D^2PAK	TAPE & REEL

Rev. 1

Table 3: Absolute Maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	60	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	60	V
V_{GS}	Gate-source Voltage	± 16	V
I_D	Drain Current (continuous) at T_C = 25°C	16	A
I_D	Drain Current (continuous) at T_C = 100°C	11.4	A
I_{DM} (•)	Drain Current (pulsed)	64	A
P_{TOT}	Total Dissipation at T_C = 25°C	70	W
	Derating Factor	0.4	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	20	V/ns
E_{AS} (2)	Single Pulse Avalanche Energy	250	mJ
T_j T_{stg}	Operating Junction Temperature Storage Temperature	- 55 to 175	°C

(•) Pulse width limited by safe operating area
(1) $I_{SD} \leq 16A$, di/dt ≤100A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.
(2) Starting T_j = 25°C , I_D = 8 A , V_{DD} = 30 V
Note:For the P-CHANNEL MOSFET actual polarity of voltages and current has to be reverse

Table 4: Thermal Data

Rthj-case	Thermal Resistance Junction-case Max	2.14	°C/W
Rthj-PCB(#)	Thermal Resistance Junction-PCB Max	34	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose (1.6 mm frrom case, for 10sec)	300	°C

(#) When Mounted on 1 inch^2 FR-4 board, 2 oz of Cu

ELECTRICAL CHARACTERISTICS (T_{CASE} =25°C UNLESS OTHERWISE SPECIFIED)

Table 5: On/Off

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D = 250µA, V_{GS} = 0	60			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating V_{DS} = Max Rating, T_C = 125 °C			1 10	µA µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 16V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 100µA	1.5			V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 8 A V_{GS} = 5V, I_D = 8 A		0.11 0.130	0.125 0.165	Ω Ω

ELECTRICAL CHARACTERISTICS (CONTINUED)

Table 6: Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs}	Forward Transconductance	V_{DS} = 10 V, I_D = 3 A		7.2		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		630 121 49		pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	V_{DD} = 30 V, I_D = 8 A, R_G = 4.7Ω V_{GS} = 4.5 V (Resistive Load , Figure 1)		129 90 25.5 19.5		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD} = 48 V, I_D = 16 A, V_{GS} = 4.5V (See test circuit, Figure 2)		11.4 5.2 4.7	15.5	nC nC nC

Table 7: Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (2)	Source-drain Current Source-drain Current (pulsed)				16 64	A A
V_{SD} (1)	Forward On Voltage	I_{SD} = 8 A, V_{GS} = 0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD} = 16 A, di/dt = 100A/µs V_{DD} = 20V, T_j = 150°C (see test circuit, Figure 3)		48.5 87.3 3.6		ns nC A

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

Figure 3: Safe Operating Area

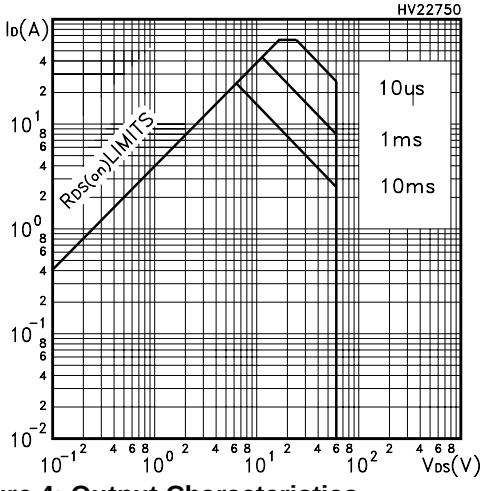


Figure 4: Output Characteristics

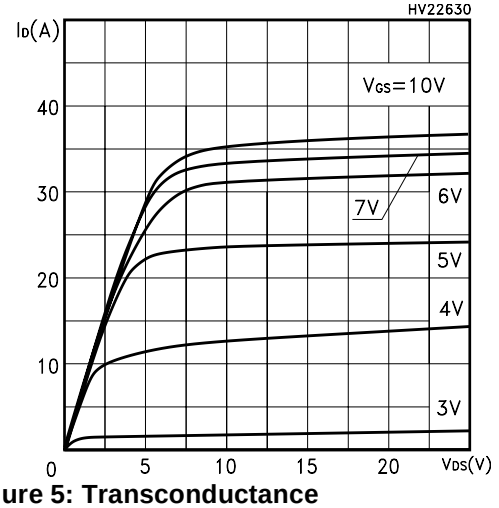


Figure 5: Transconductance

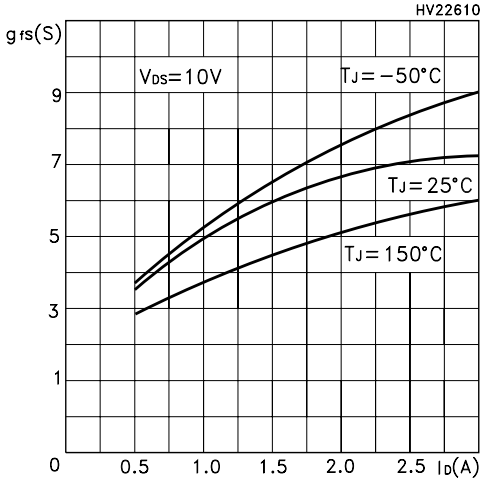


Figure 6: Thermal Impedance

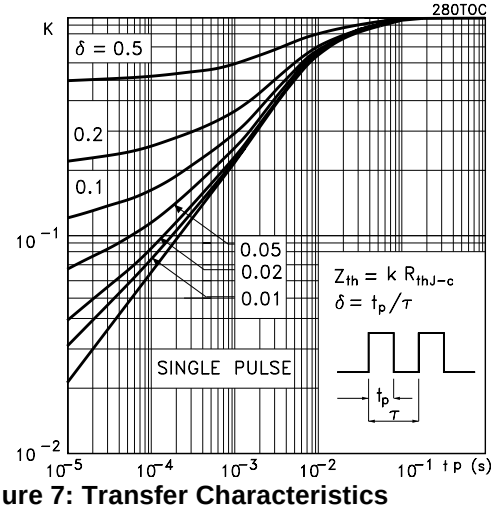


Figure 7: Transfer Characteristics

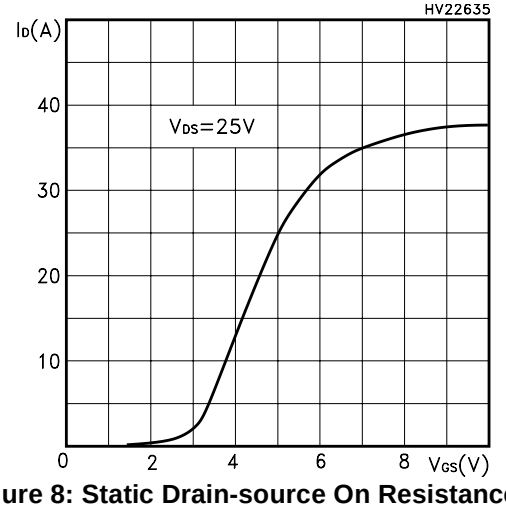


Figure 8: Static Drain-source On Resistance

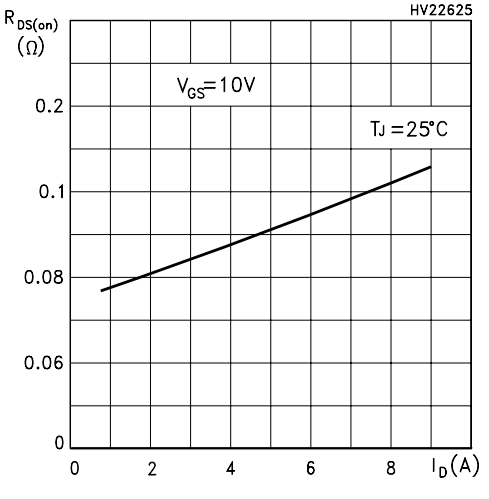


Figure 9: Gate Charge vs Gate-source Voltage

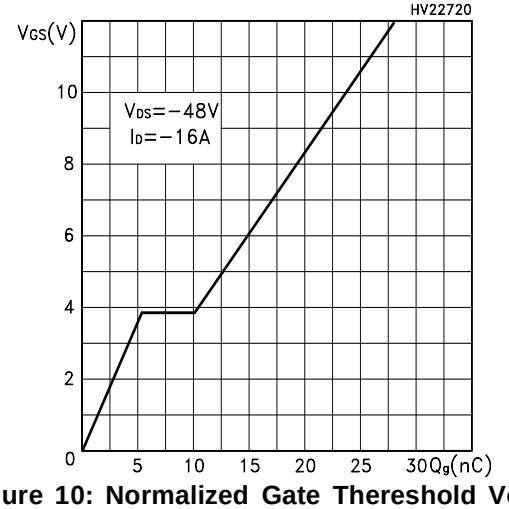


Figure 10: Normalized Gate Thereshold Voltage vs Temperature

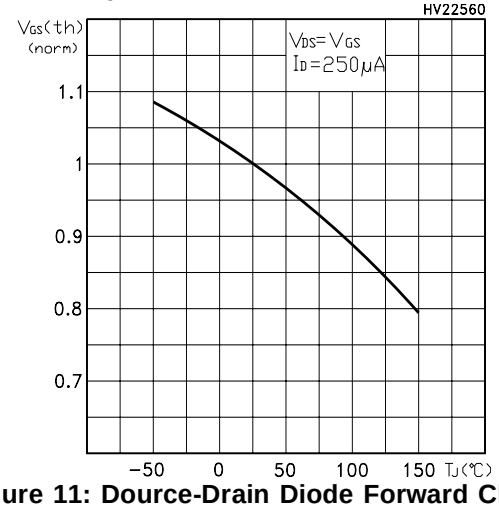


Figure 11: Dource-Drain Diode Forward Characteristics

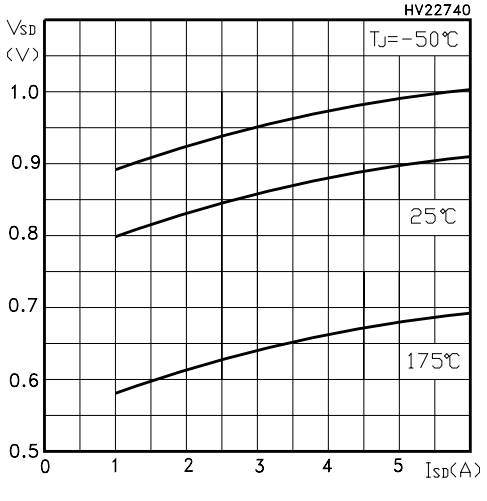


Figure 12: Capacitance Variations

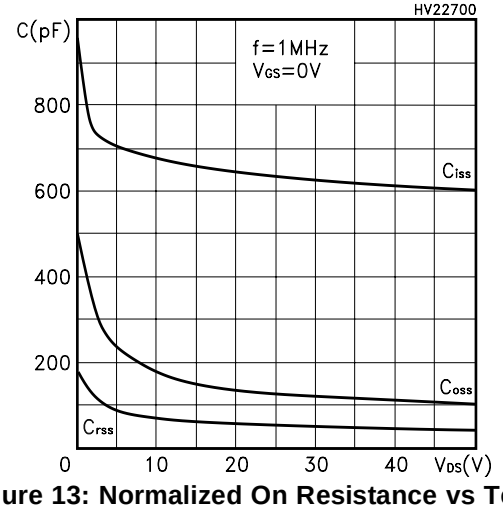


Figure 13: Normalized On Resistance vs Temperature

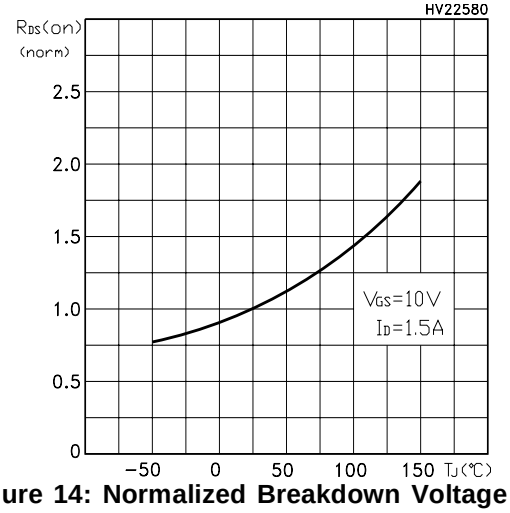


Figure 14: Normalized Breakdown Voltage vs Temperature

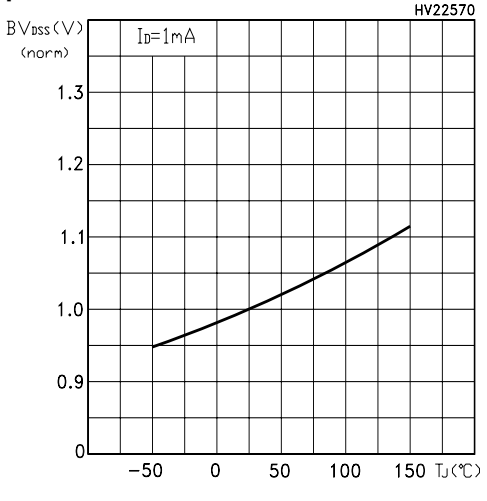


Figure 15: Unclamped Inductive Load Test Circuit

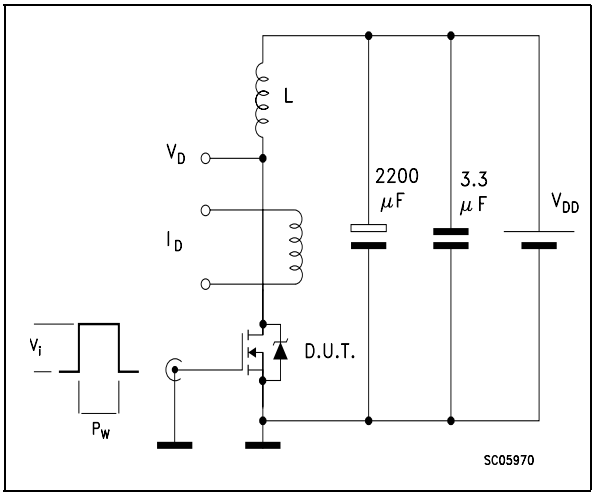


Figure 16: Switching Times Test Circuit For Resistive Load

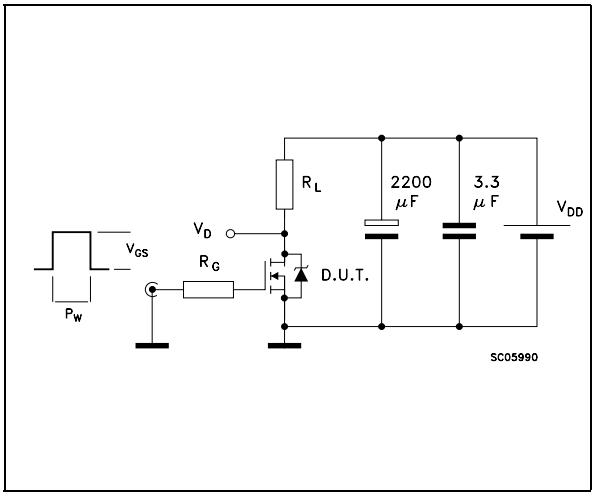


Figure 17: Test Circuit For Inductive Load Switching and Diode Recovery Times

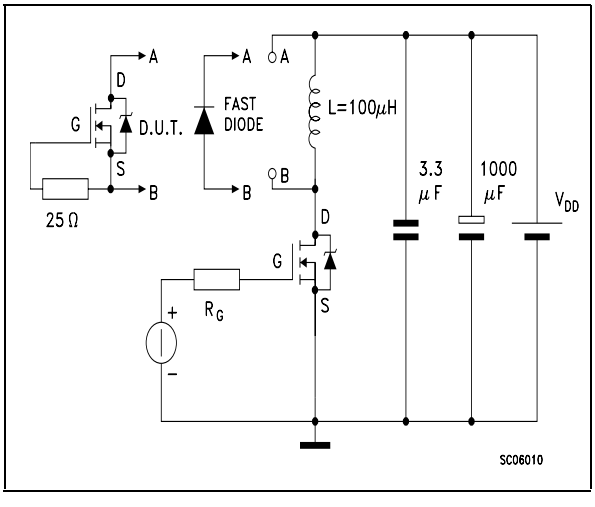


Figure 18: Unclamped Inductive Wafeform

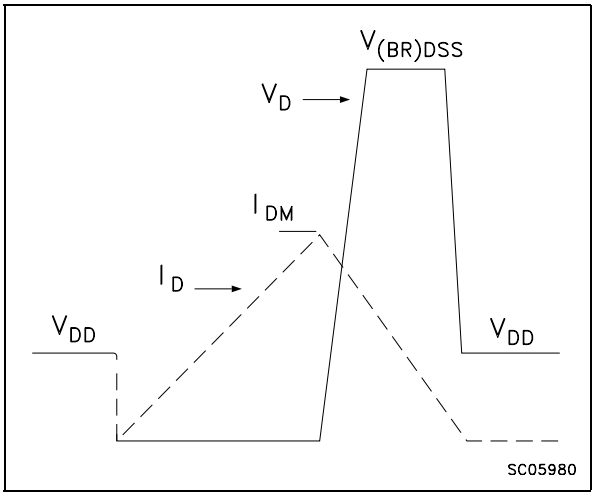
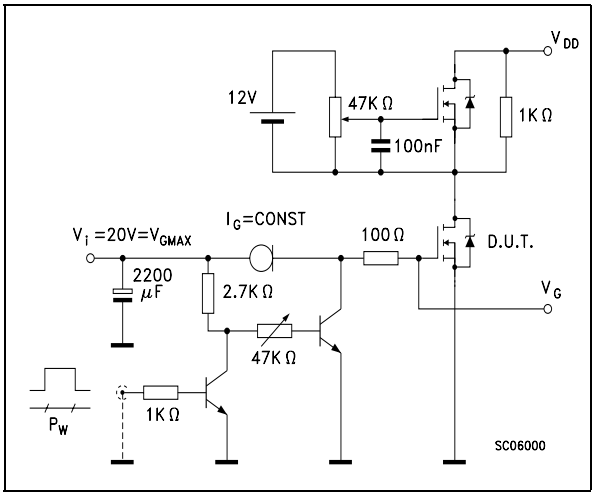
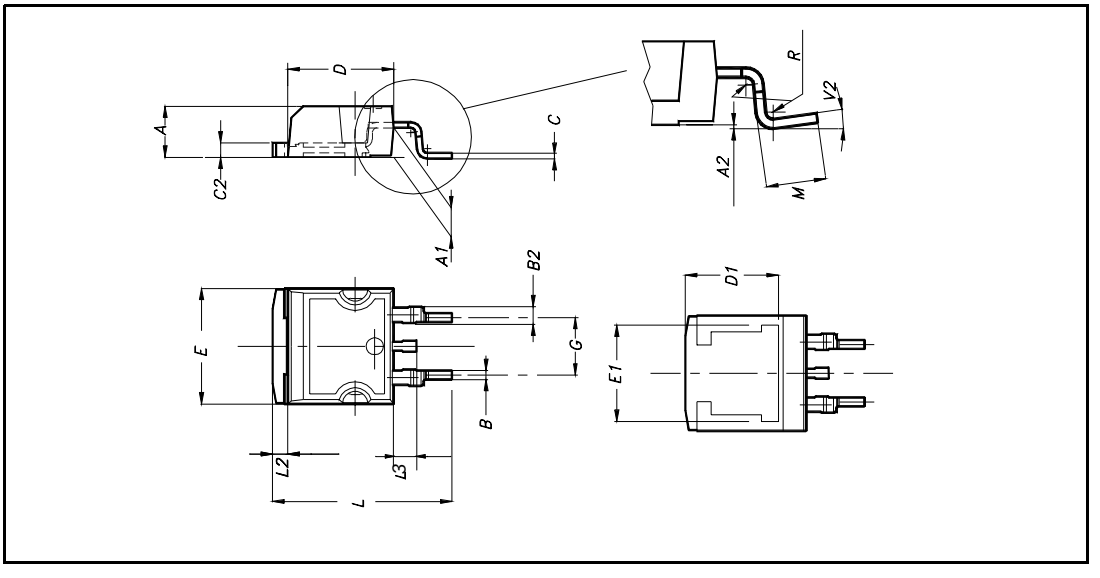


Figure 19: Gate Charge Test Circuit

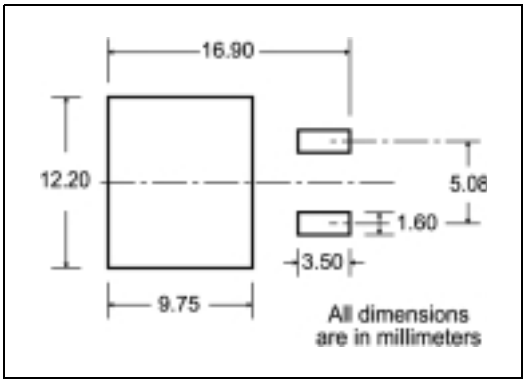


D^2PAK MECHANICAL DATA

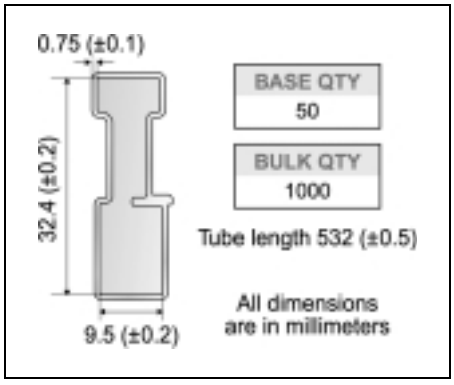
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0º		4º			



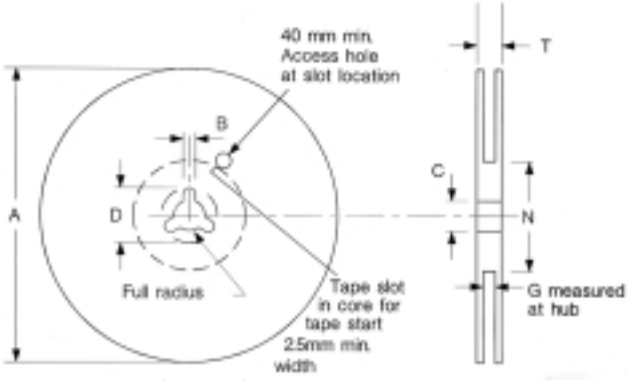
D²PAK FOOTPRINT



TUBE SHIPMENT (no suffix)*



TAPE AND REEL SHIPMENT (suffix "T4")*



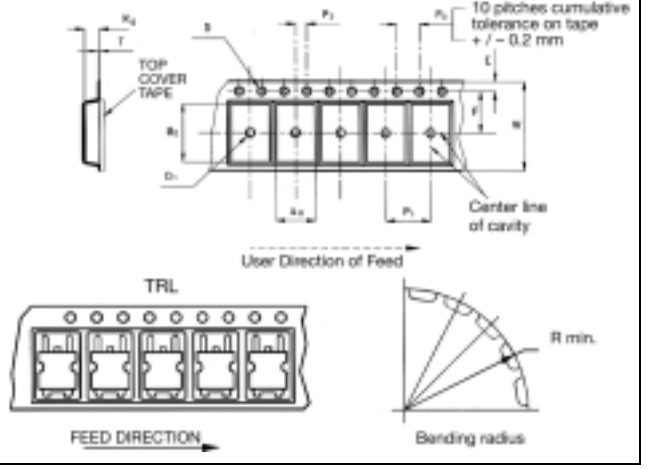
REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

BASE QTY	BULK QTY
1000	1000

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956



* on sales type

Table 8: Revision History

Date	Revision	Description of Changes
13/Sep/2004	1	First Release.