



STB180N55 STP180N55

N-CHANNEL 55V - 2.9mΩ - 120A - D²PAK - TO-220
MDmesh™ Low Voltage Power MOSFET

TARGET SPECIFICATION

General features

Type	V _{DSS}	R _{DS(on)}	I _D
STB180N55	55V	3.5mΩ	120A (Note 1)
STP180N55	55V	3.8mΩ	120A (Note 1)

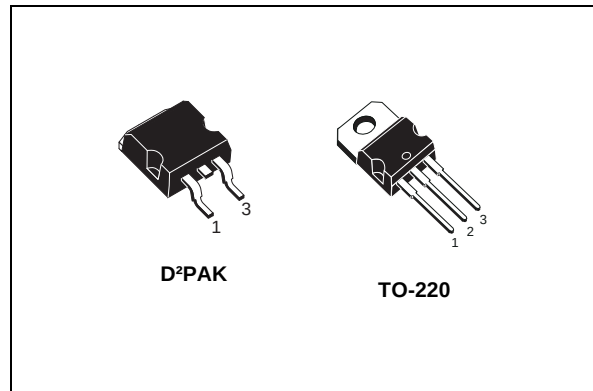
- ULTRA LOW ON-RESISTANCE
- 100% AVALANCHE TESTED

Description

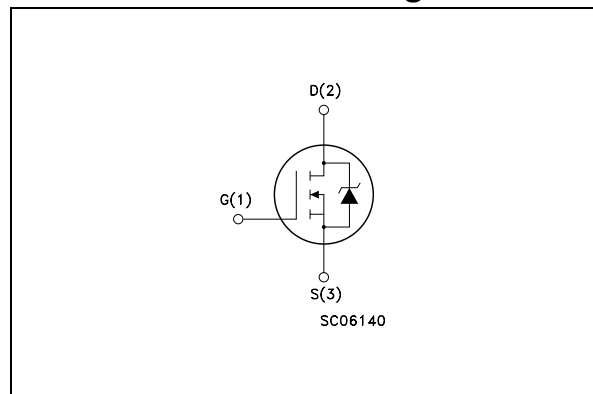
This N-Channel enhancement mode MOSFET is the latest refinement of STMicroelectronic unique "Single Feature Size™" strip-based process with less critical alignment steps and therefore a remarkable manufacturing reproducibility. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and low gate charge.

Applications

- HIGH CURRENT SWITCHING APPLICATION



Internal schematic diagram



Order codes

Sales Type	Marking	Package	Packaging
STB180N55	B180N55	D ² PAK	TAPE & REEL
STP180N55	P180N55	TO-220	TUBE

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage ($V_{GS}=0$)	55	V
V_{GS}	Gate-Source Voltage	± 20	V
I_D Note 1	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	120	A
I_D Note 1	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	120	A
I_{DM} Note 2	Drain Current (pulsed)	480	A
P_{TOT}	Total Dissipation at $T_C = 25^\circ\text{C}$	315	W
	Derating Factor	2.1	W/ $^\circ\text{C}$
dv/dt	Peak Diode Recovery voltage slope	TBD	V/ns
E_{AS} Note 4	Single Pulse Avalanche Energy	TBD	mJ
T_j T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 175	$^\circ\text{C}$

Table 2. Thermal data

		TO-220	D ² PAK	Unit
$R_{thj-case}$	Thermal Resistance Junction-case	0.48		$^\circ\text{C/W}$
R_{thj-a}	Thermal Resistance Junction-ambient Max	62.5	--	$^\circ\text{C/W}$
$R_{thj-pcb}$ Note 5	Thermal Resistance Junction-ambient Max	--	35	$^\circ\text{C/W}$
T_l	Maximum Lead Temperature For Soldering Purpose	300	--	$^\circ\text{C}$

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-Source Breakdown Voltage	I _D = 250μA, V _{GS} = 0	55			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating, V _{DS} = Max Rating, T _c = 125°C			10 100	μA μA
I _{GSS}	Gate Body Leakage Current (V _{DS} = 0)	V _{GS} = ±20V			±200	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	2		4	V
R _{DS(on)}	Static Drain-Source On Resistance	V _{GS} = 10V, I _D = 60A D²PAK TO-220			3.5 3.8	mΩ mΩ

Table 4. Dynamic

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} <i>Note 3</i>	Forward Transconductance	V _{DS} = 15V, I _D = 60A		TBD		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		6200 1800 100		pF pF pF
Q _g Q _{gs} Q _{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V _{DD} = 44V, I _D = 120A V _{GS} = 10V (see Figure 2)		110 TBD TBD	TBD	nC nC nC

Table 5. Switching times

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD}=27V$, $I_D=60A$, $R_G=4.7\Omega$, $V_{GS}=10V$ (see Figure 3)		TBD TBD		ns ns
$t_{d(off)}$ t_f	Off voltage Rise Time FallTime	$V_{DD}=27V$, $I_D=60A$, $R_G=4.7\Omega$, $V_{GS}=10V$ (see Figure 3)		TBD TBD		ns ns

Table 6. Source drain diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} Note 2	Source-drain Current Source-drain Current (pulsed)				120 480	A A
V_{SD} Note 3	Forward on Voltage	$I_{SD}=120A$, $V_{GS}=0$			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD}=120A$, $di/dt = 100A/\mu s$, $V_{DD}=30V$, $T_j=150^\circ C$		TBD TBD TBD		ns nC A

(1) Current limited by package

(2) Pulse width limited by safe operating area

(3) Pulsed: pulse duration = 300 μs , duty cycle 1.5%(4) Starting $T_j=25^\circ C$, $I_D=60A$, $V_{DD}=40V$ (5) When mounted on 1 inch² FR4 2oz Cu

3 Test circuits

Figure 1. Switching Times Test Circuit For Resistive Load

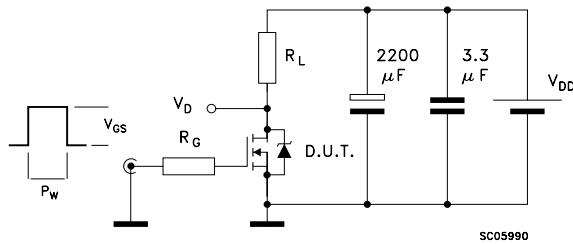


Figure 2. Gate Charge Test Circuit

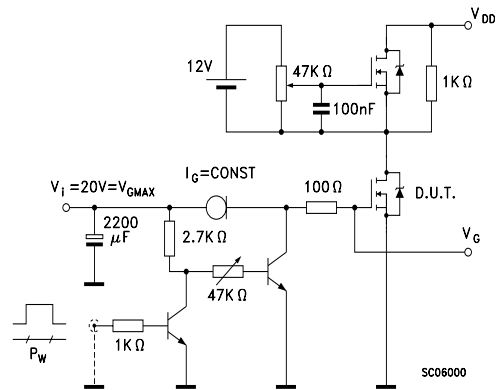


Figure 3. Test Circuit For Inductive Load Switching and Diode Recovery Times

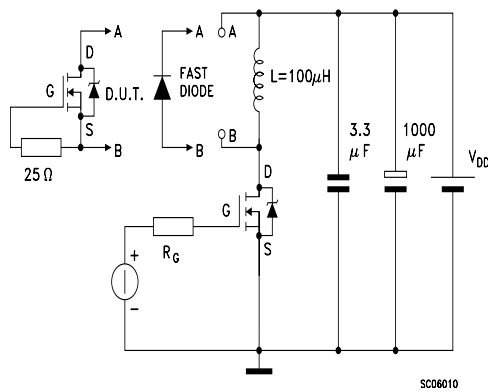


Figure 5. Unclamped Inductive Load Test Circuit

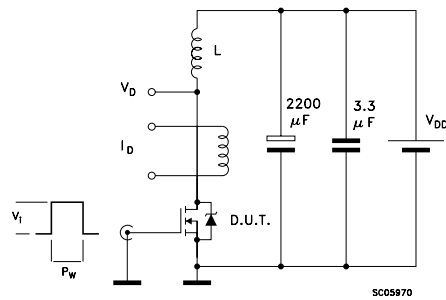


Figure 4. Unclamped Inductive Waveform

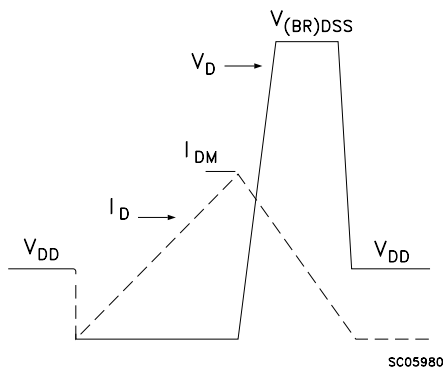
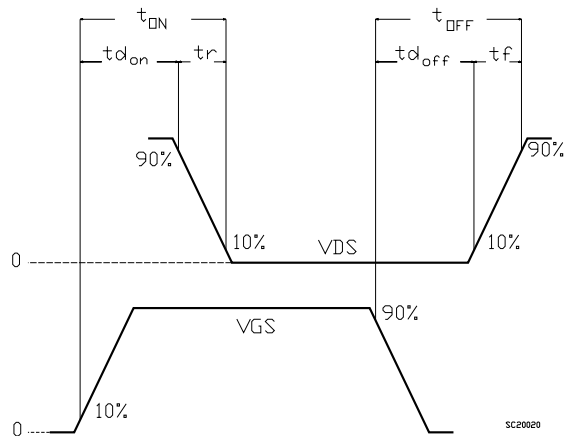


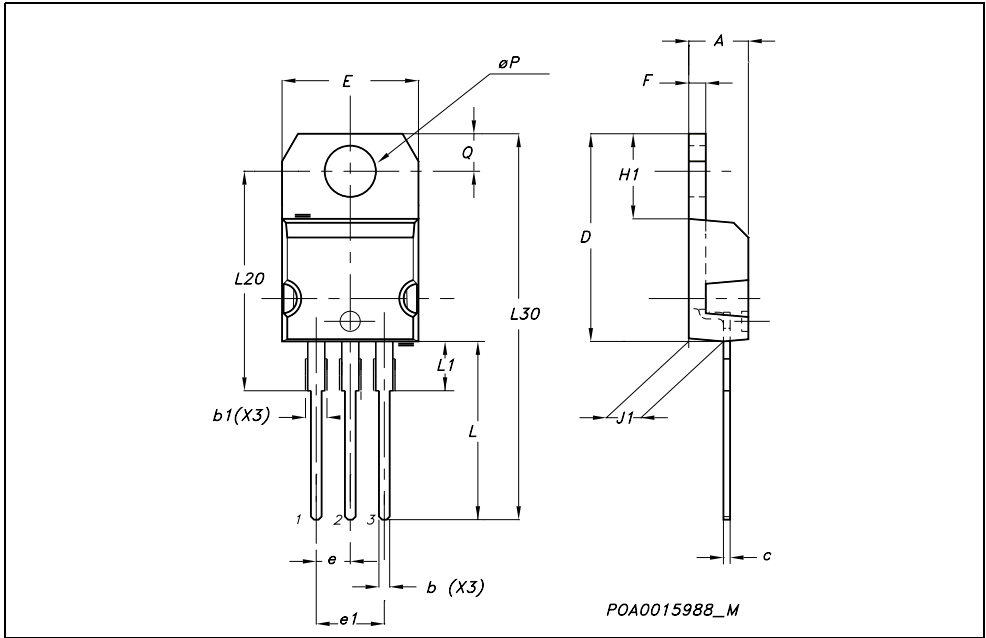
Figure 6. Switching Time Waveform



4 Package mechanical data

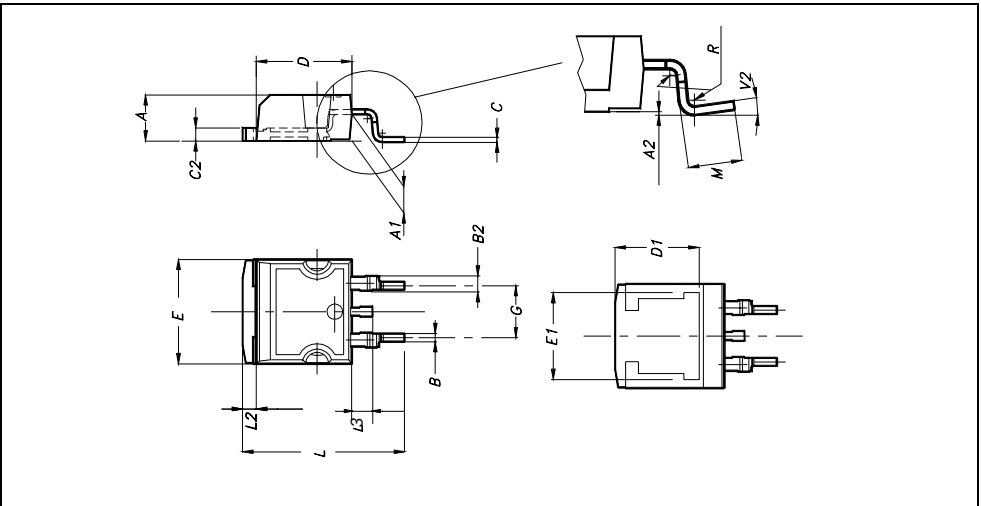
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TO-220 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



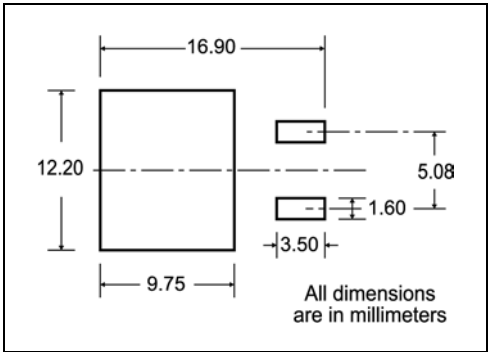
D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			

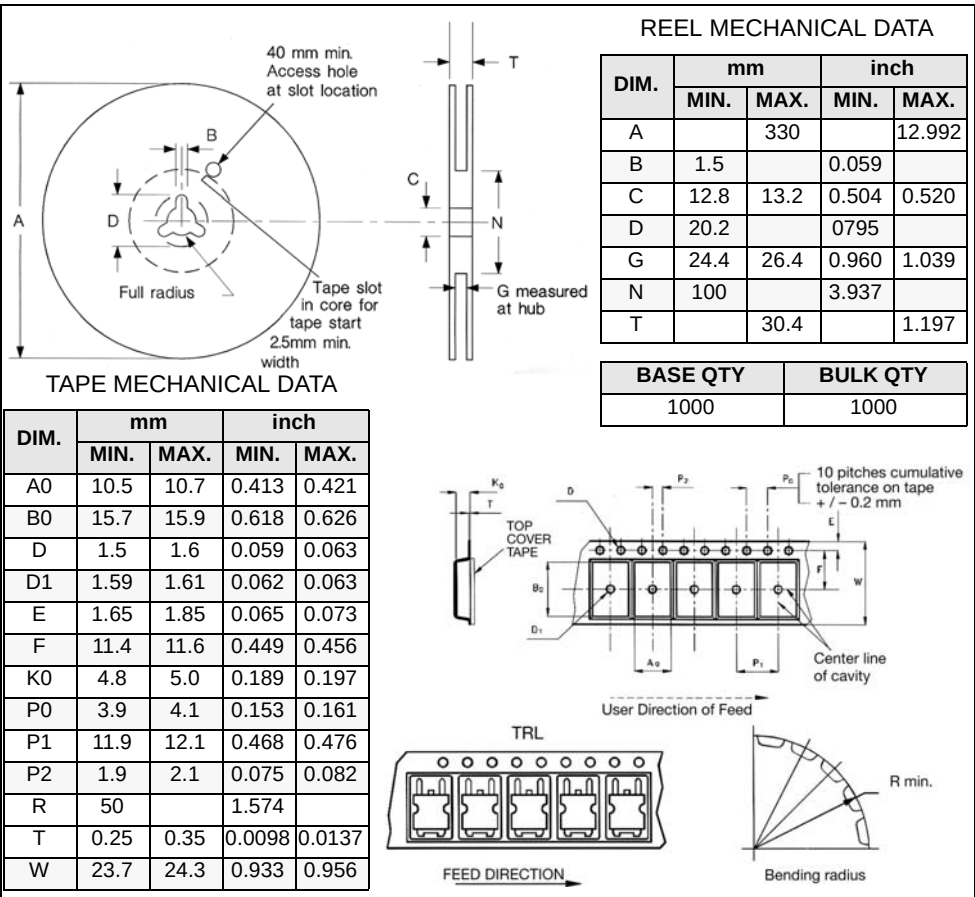


5 Packing mechanical data

D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT



* on sales type

6 Revision History

Date	Revision	Changes
03-Jan-2006	1	First release

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