STB28N60DM2, STP28N60DM2, STW28N60DM2

N-channel 600 V, 0.13 Ω typ., 21 A MDmesh™ DM2 Power MOSFETs in D²PAK, TO-220 and TO-247 packages

Datasheet - production data

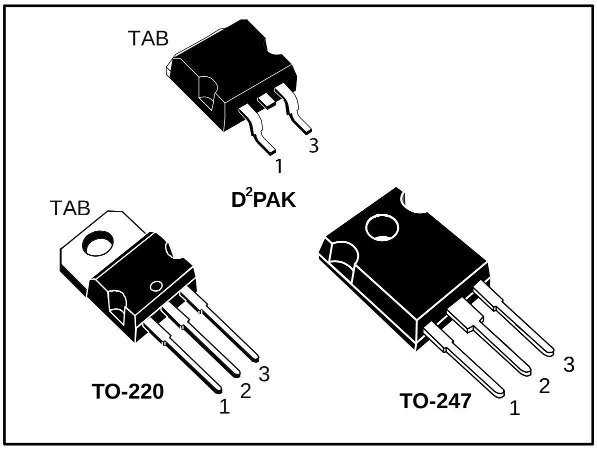
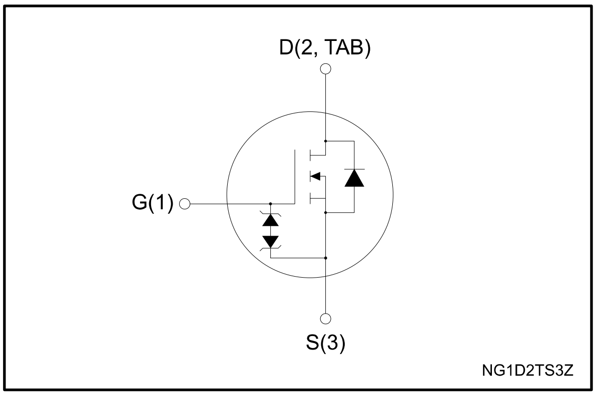


Figure 1: Internal schematic diagram



Features

Order code	V_{DS} @ $T_{Jmax.}$	$R_{DS(on)}$ max.	I_D	P_{TOT}
STB28N60DM2	650 V	0.16 Ω	21 A	170 W
STP28N60DM2				
STW28N60DM2				

- Fast-recovery body diode
- Extremely low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- Extremely high dv/dt ruggedness
- Zener-protected

Applications

- Switching applications

Description

These high voltage N-channel Power MOSFETs are part of the MDmesh™ DM2 fast recovery diode series. They offer very low recovery charge (Q_{rr}) and time (t_{rr}) combined with low $R_{DS(on)}$, rendering them suitable for the most demanding high efficiency converters and ideal for bridge topologies and ZVS phase-shift converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STB28N60DM2	28N60DM2	D²PAK	Tape and reel
STP28N60DM2		TO-220	Tube
STW28N60DM2		TO-247	Tube

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_{case} = 25 °C	21	A
	Drain current (continuous) at T_{case} = 100 °C	14	
I_{DM}(1)	Drain current (pulsed)	84	A
P_{TOT}	Total dissipation at T_{case} = 25 °C	170	W
dv/dt(2)	Peak diode recovery voltage slope	50	V/ns
dv/dt(3)	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

Notes:

(1) Pulse width is limited by safe operating area.

(2) I_{SD} ≤ 21 A, di/dt=900 A/μs; V_{DS} peak < $V_{(BR)DSS}$,V_{DD} = 400 V

(3) V_{DS} ≤ 480 V.

Table 3: Thermal data

Symbol	Parameter	Value			Unit
		D²PAK	TO-220	TO-247	
$R_{thj-case}$	Thermal resistance junction-case	0.74			°C/W
$R_{thj-pcb}$(1)	Thermal resistance junction-pcb	30			
$R_{thj-amb}$	Thermal resistance junction-ambient		62.5	50	

Notes:

(1) When mounted on a 1-inch² FR-4, 2 Oz copper board.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}(1)	Avalanche current, repetitive or not repetitive	4	A
E_{AS}(2)	Single pulse avalanche energy	350	mJ

Notes:

(1) pulse width limited by T_{jmax}

(2) starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V.

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 5: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_{case} = 125 °C(1)			100	
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 10.5 A		0.13	0.16	Ω

Notes:

(1)Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	1500	-	pF
C_{oss}	Output capacitance		-	70	-	
C_{rss}	Reverse transfer capacitance		-	1.6	-	
$C_{oss\ eq.}$(1)	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	134	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	4.6	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 21 A, V_{GS} = 0 to 10 V (see *Figure 19: "Test circuit for gate charge behavior"*)	-	34	-	nC
Q_{gs}	Gate-source charge		-	8	-	
Q_{gd}	Gate-drain charge		-	18.5	-	

Notes:

(1) $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 10.5 A R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 18: "Test circuit for resistive load switching times"* and *Figure 23: "Switching time waveform"*)	-	16	-	ns
t_r	Rise time		-	7.3	-	
$t_{d(off)}$	Turn-off delay time		-	53	-	
t_f	Fall time		-	9.3	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}(1)	Source-drain current		-		21	A
I_{SDM}(2)	Source-drain current (pulsed)		-		84	A
V_{SD}(3)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 21 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 21 A, di/dt = 100 A/µs, V_{DD} = 60 V (see *Figure 20: "Test circuit for inductive load switching and diode recovery times"*)	-	140		ns
Q_{rr}	Reverse recovery charge		-	0.5		µC
I_{RRM}	Reverse recovery current		-	7.4		A
t_{rr}	Reverse recovery time	I_{SD} = 21 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see *Figure 20: "Test circuit for inductive load switching and diode recovery times"*)	-	309		ns
Q_{rr}	Reverse recovery charge		-	2.6		µC
I_{RRM}	Reverse recovery current		-	16.8		A

Notes:

(1) Limited by maximum junction temperature.

(2) Pulse width is limited by safe operating area.

(3) Pulse test: pulse duration = 300 µs, duty cycle 1.5%.

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS} = ±250 µA, I_D = 0 A	±25	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area for D²PAK

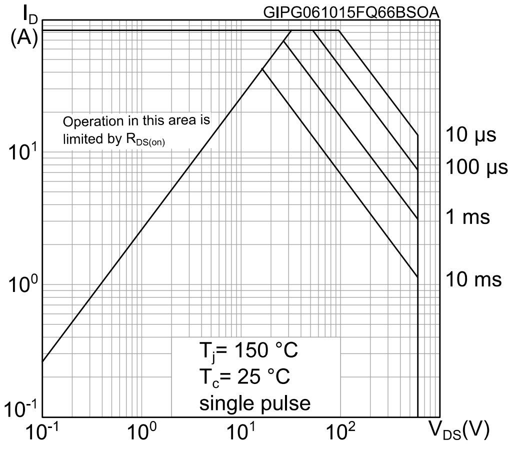


Figure 3: Thermal impedance for D²PAK

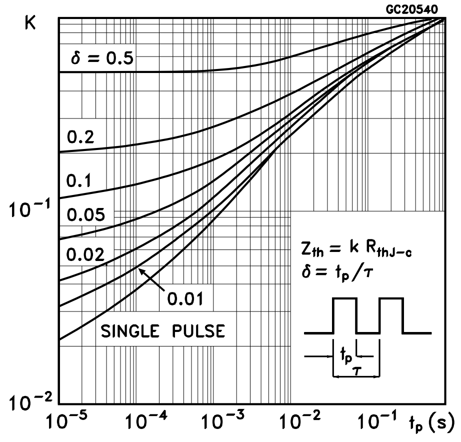


Figure 4: Safe operating area for TO-220

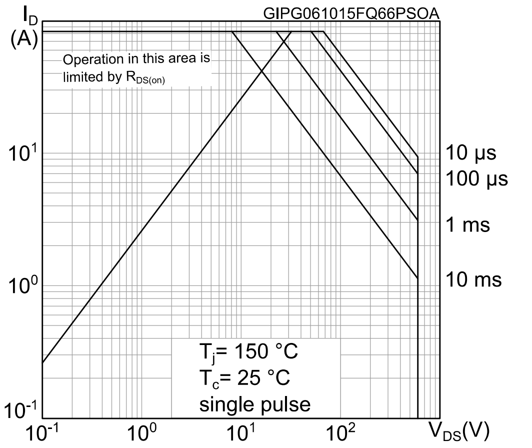


Figure 5: Thermal impedance for TO-220

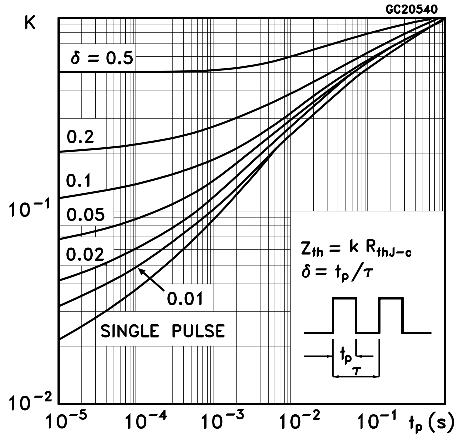


Figure 6: Safe operating area for TO-247

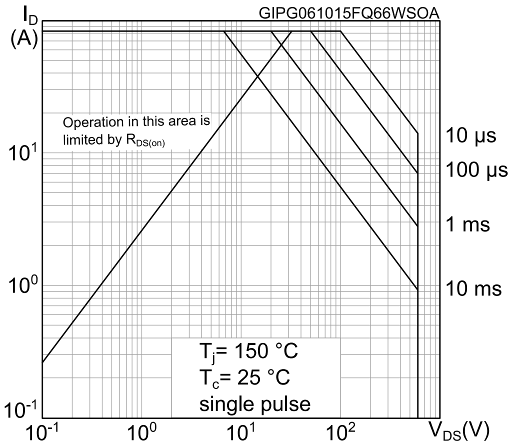


Figure 7: Thermal impedance for TO-247

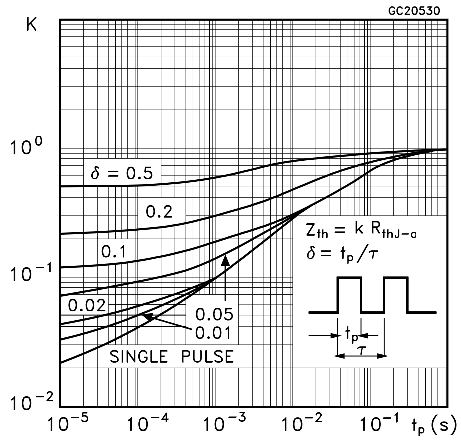


Figure 8: Output characteristics

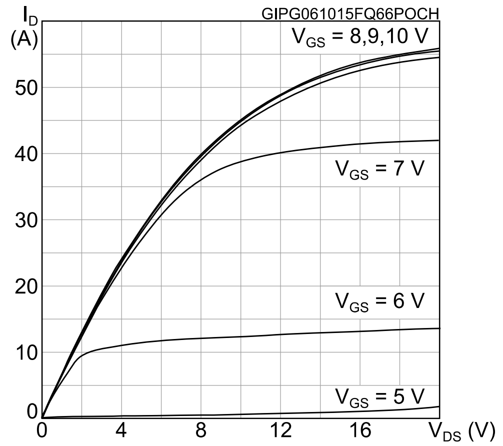


Figure 9: Transfer characteristics

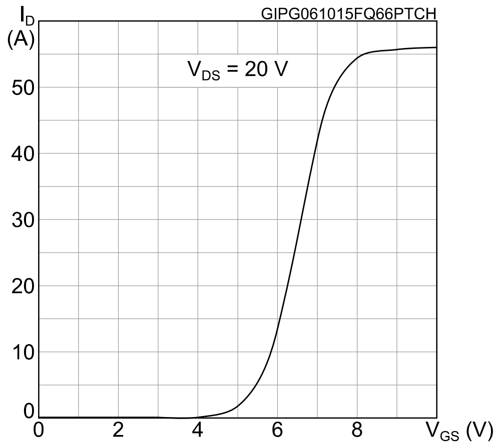


Figure 10: Gate charge vs gate-source voltage

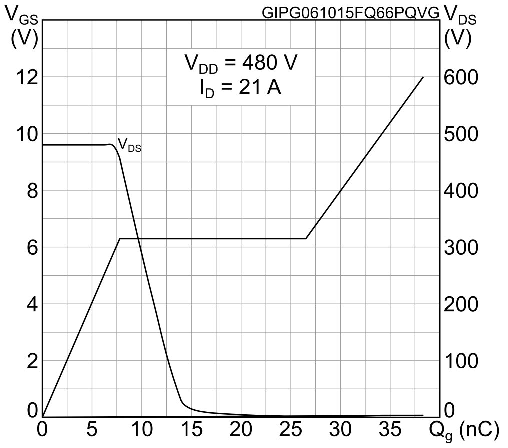


Figure 11: Static drain-source on-resistance

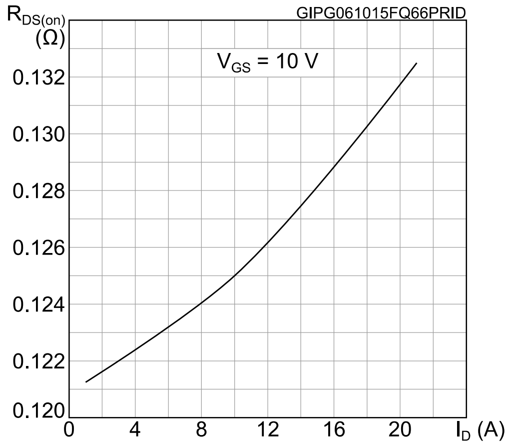


Figure 12: Capacitance variations

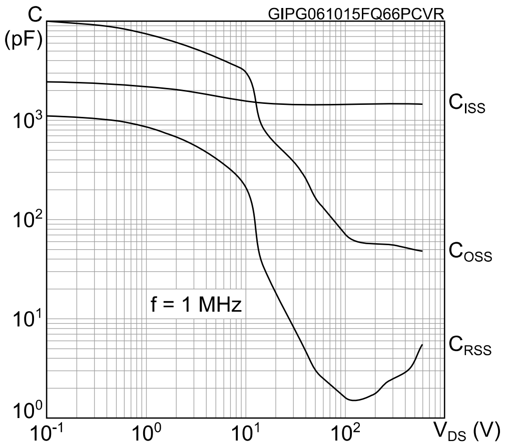


Figure 13: Normalized gate threshold voltage vs temperature

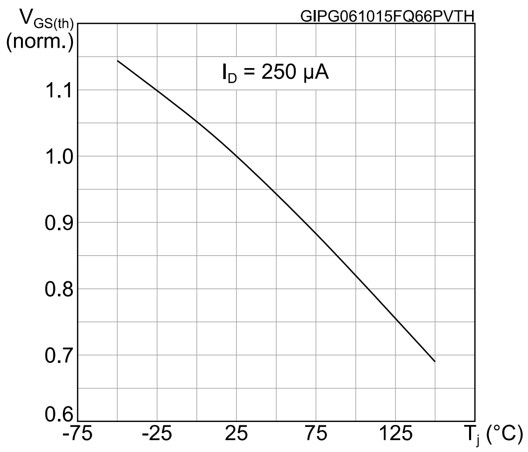


Figure 14: Normalized on-resistance vs temperature

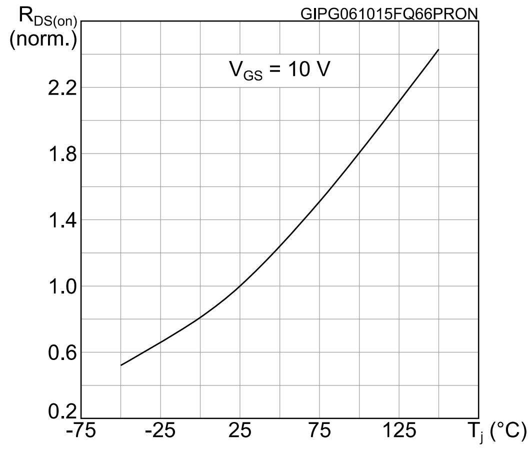


Figure 15: Normalized V(BR)DSS vs temperature

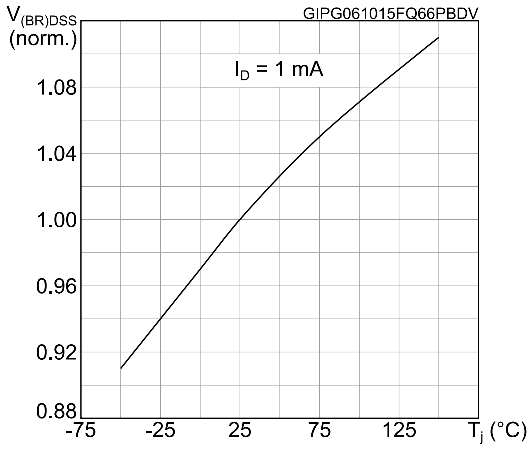


Figure 16: Output capacitance stored energy

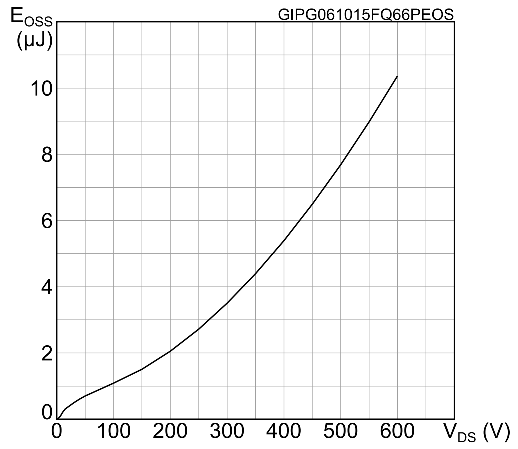
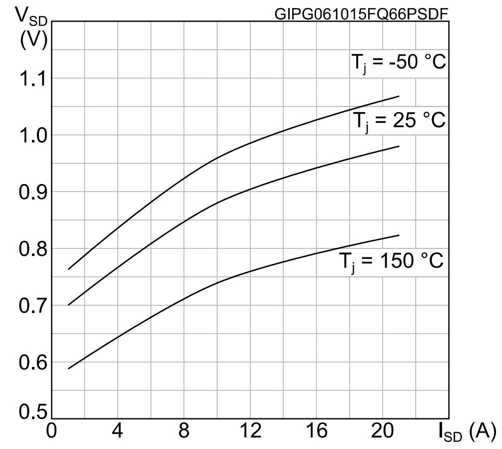


Figure 17: Source-drain diode forward characteristics



3 Test circuits

Figure 18: Test circuit for resistive load switching times

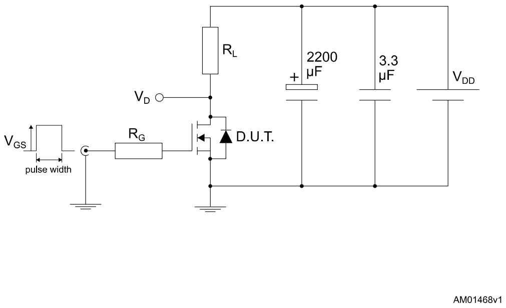


Figure 19: Test circuit for gate charge behavior

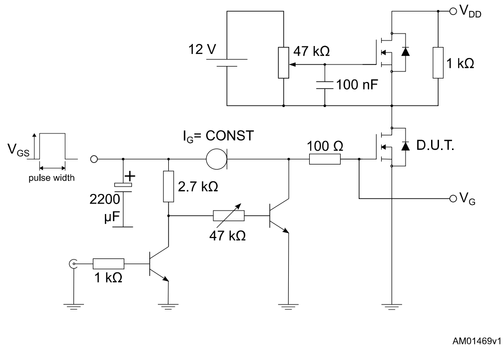


Figure 20: Test circuit for inductive load switching and diode recovery times

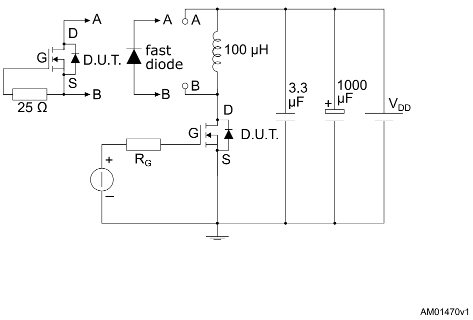


Figure 21: Unclamped inductive load test circuit

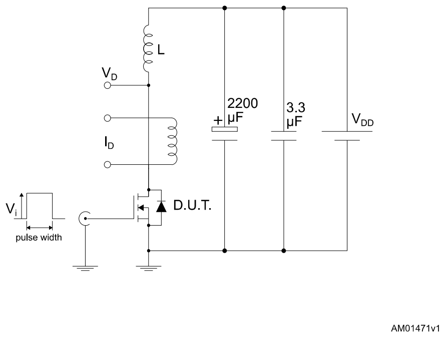


Figure 22: Unclamped inductive waveform

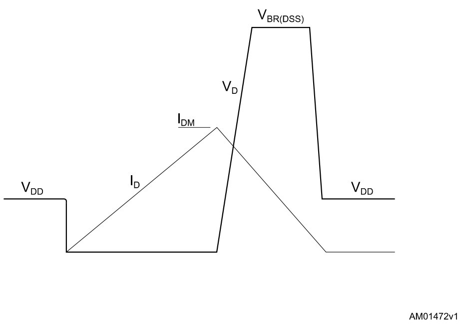
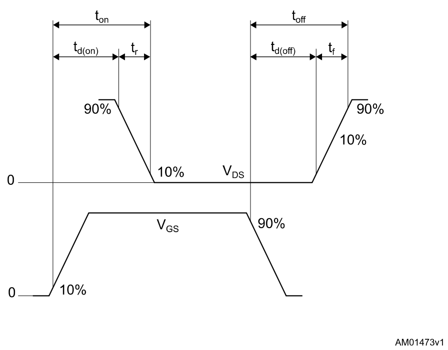


Figure 23: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 D²PAK (TO-263) type A package information

Figure 24: D²PAK (TO-263) type A package outline

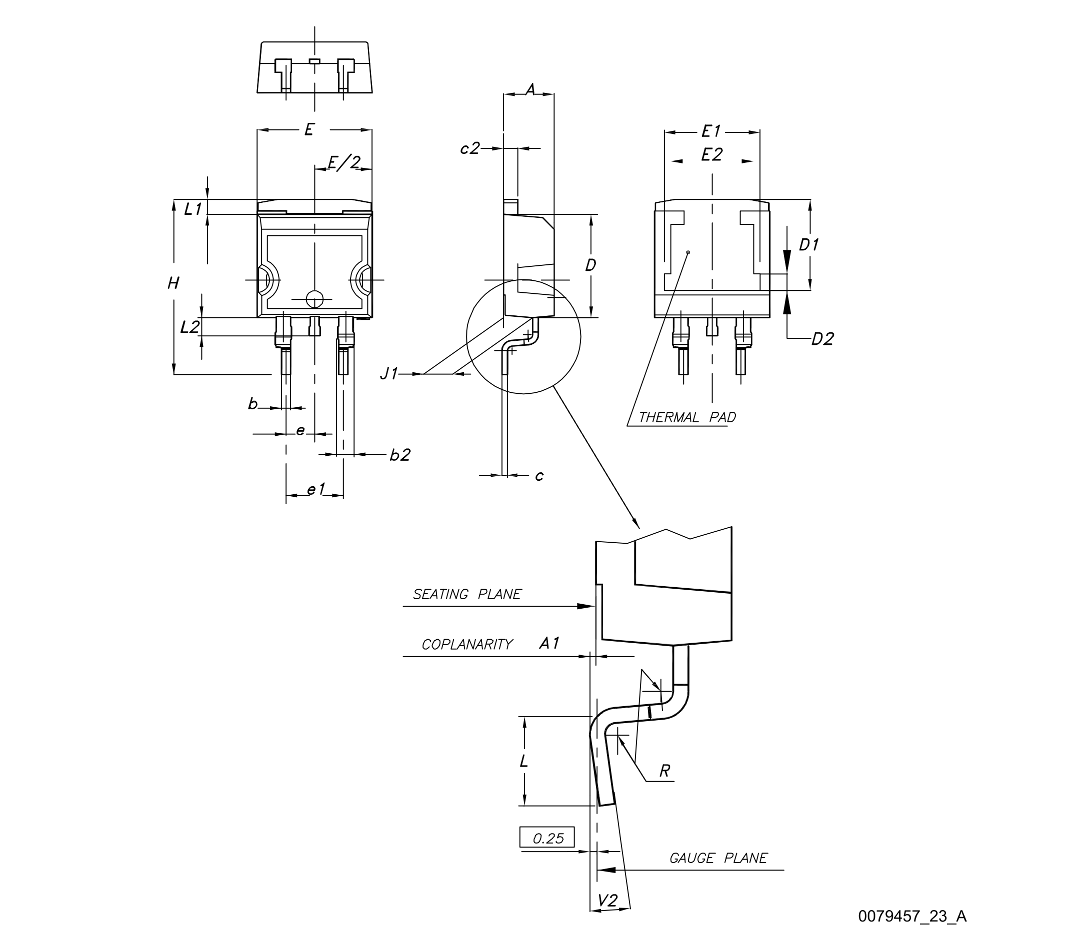
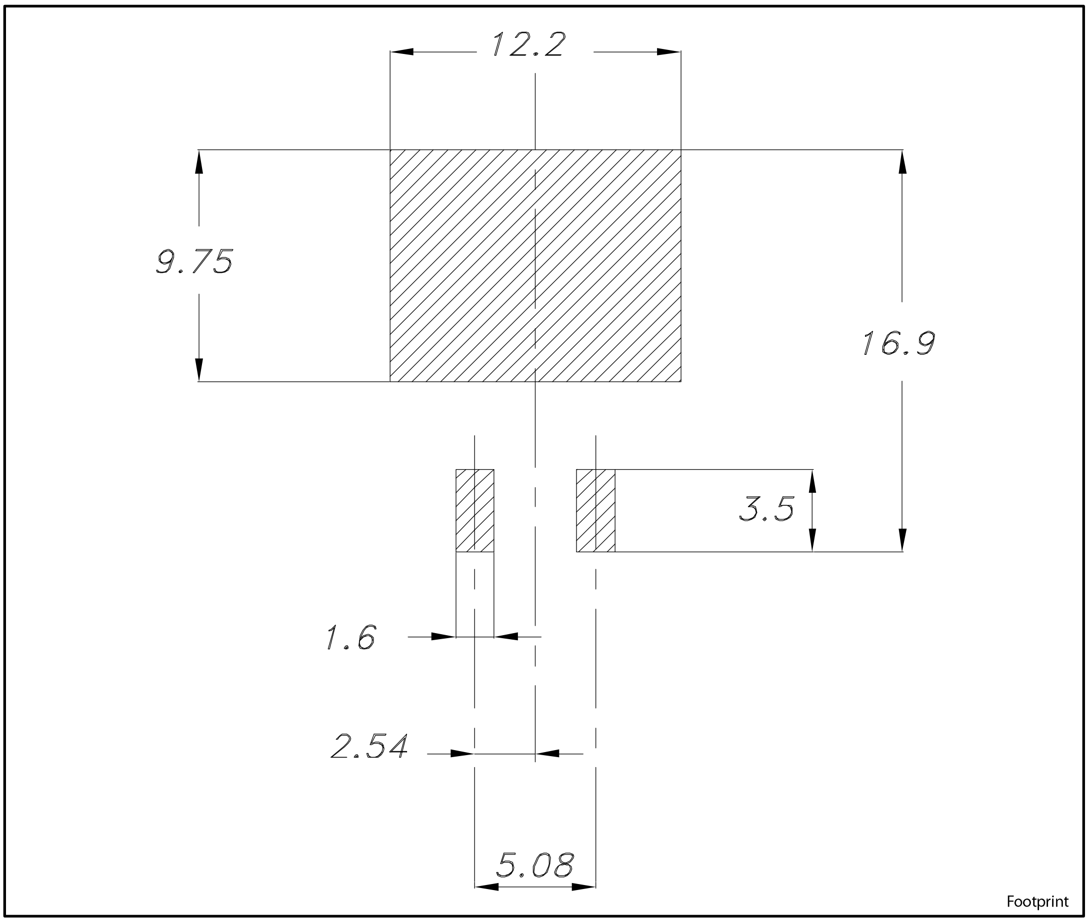


Table 10: D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

Figure 25: D²PAK (TO-263) type A recommended footprint (dimensions are in mm)



4.2 TO-220 type A package information

Figure 26: TO-220 type A package outline

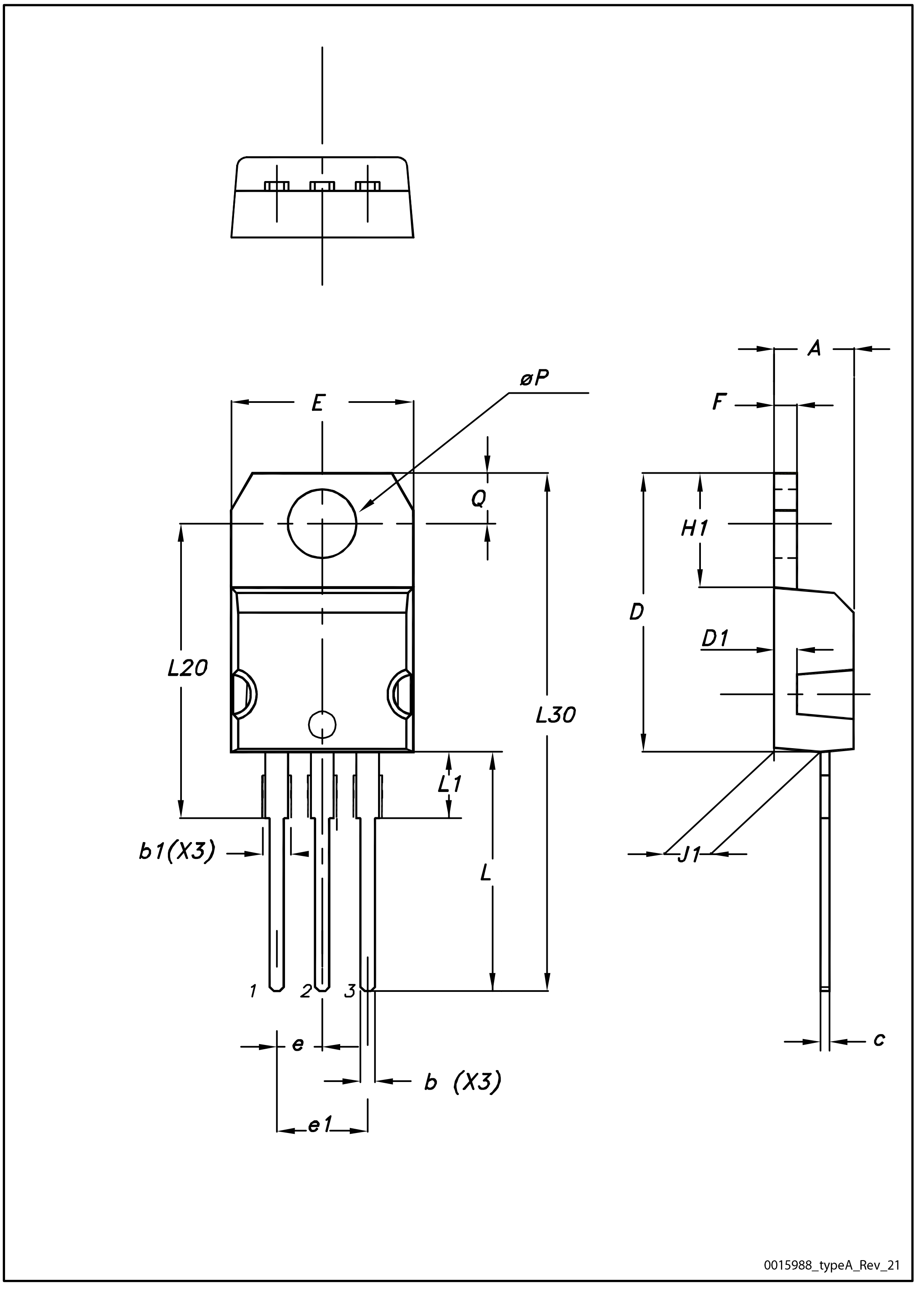


Table 11: TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

4.3 TO-247 package information

Figure 27: TO-247 package outline

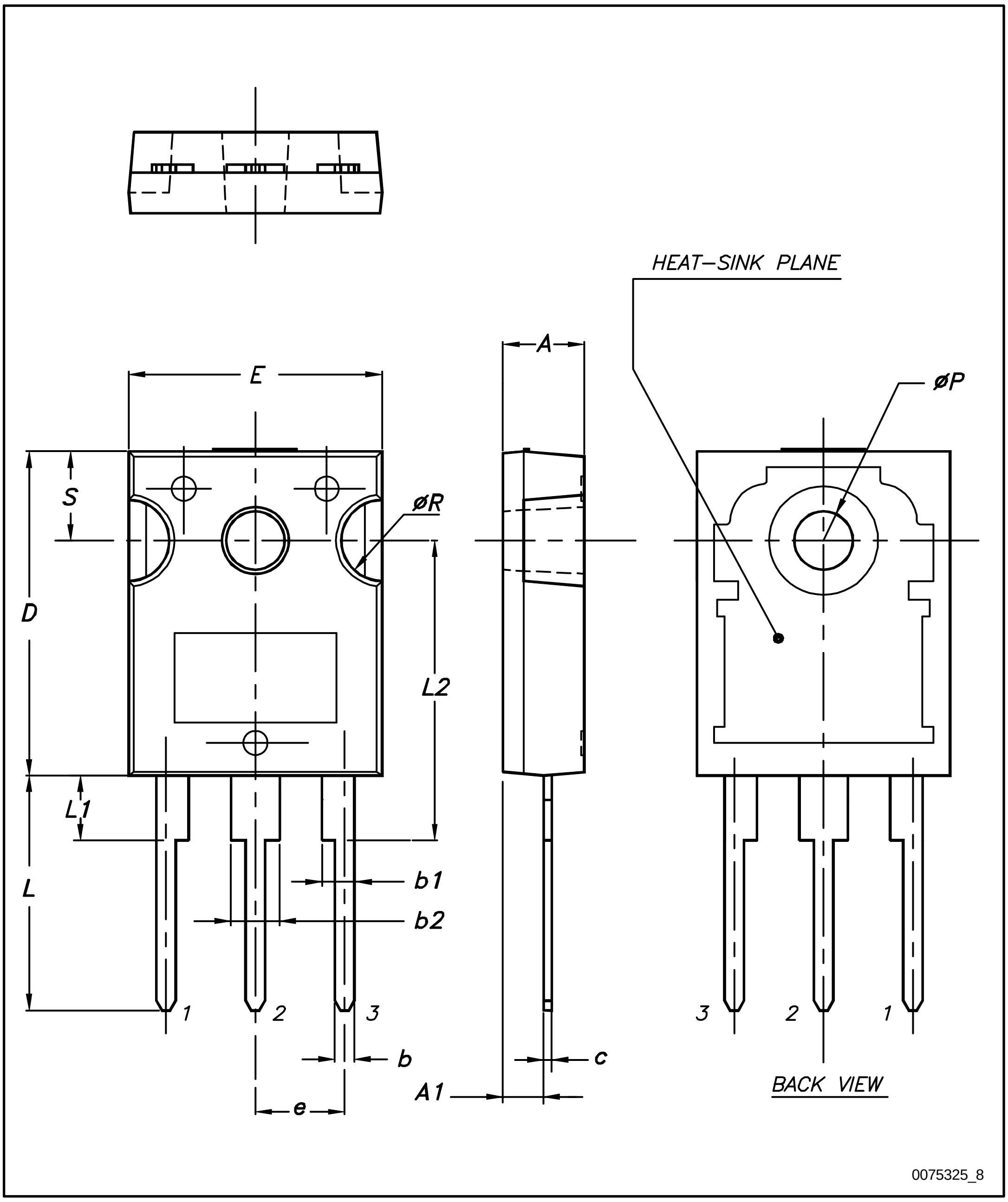


Table 12: TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

5 Packing information

5.1 D²PAK type A packing information

Figure 28: D2PAK type A tape outline

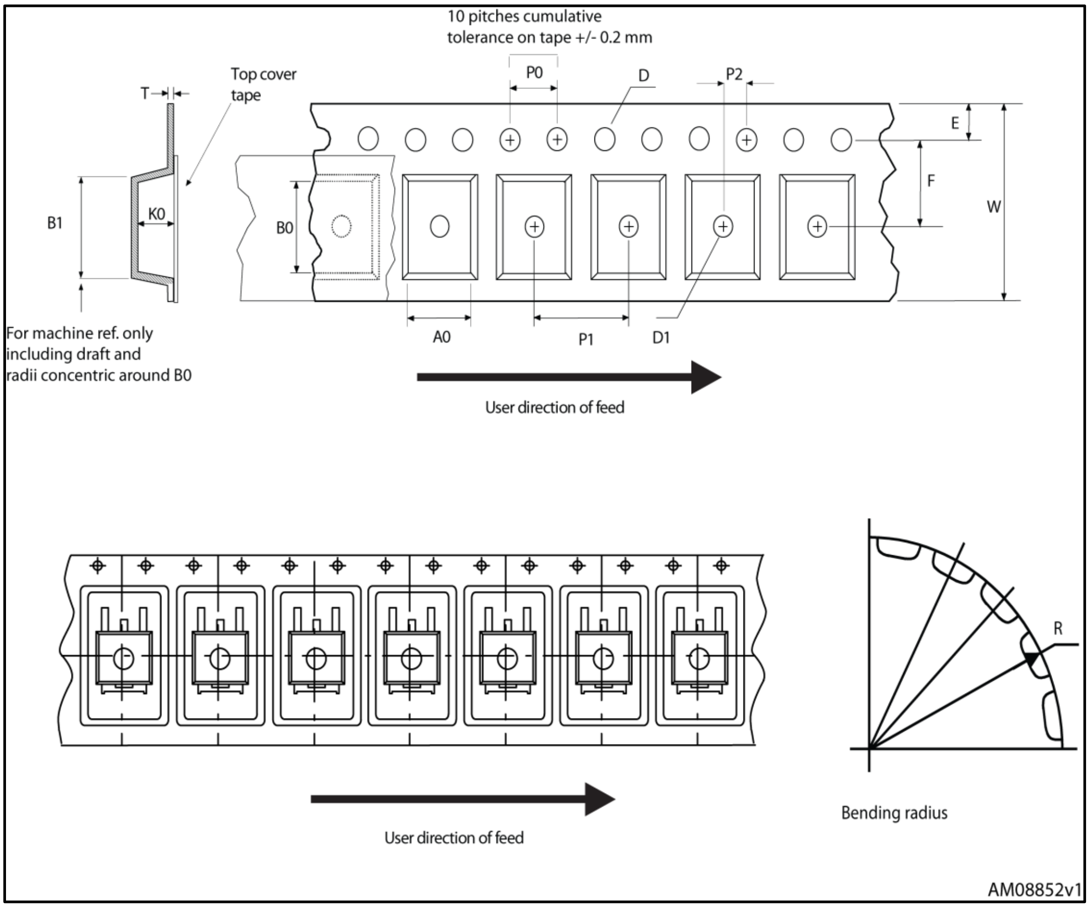


Figure 29: D2PAK type A reel outline

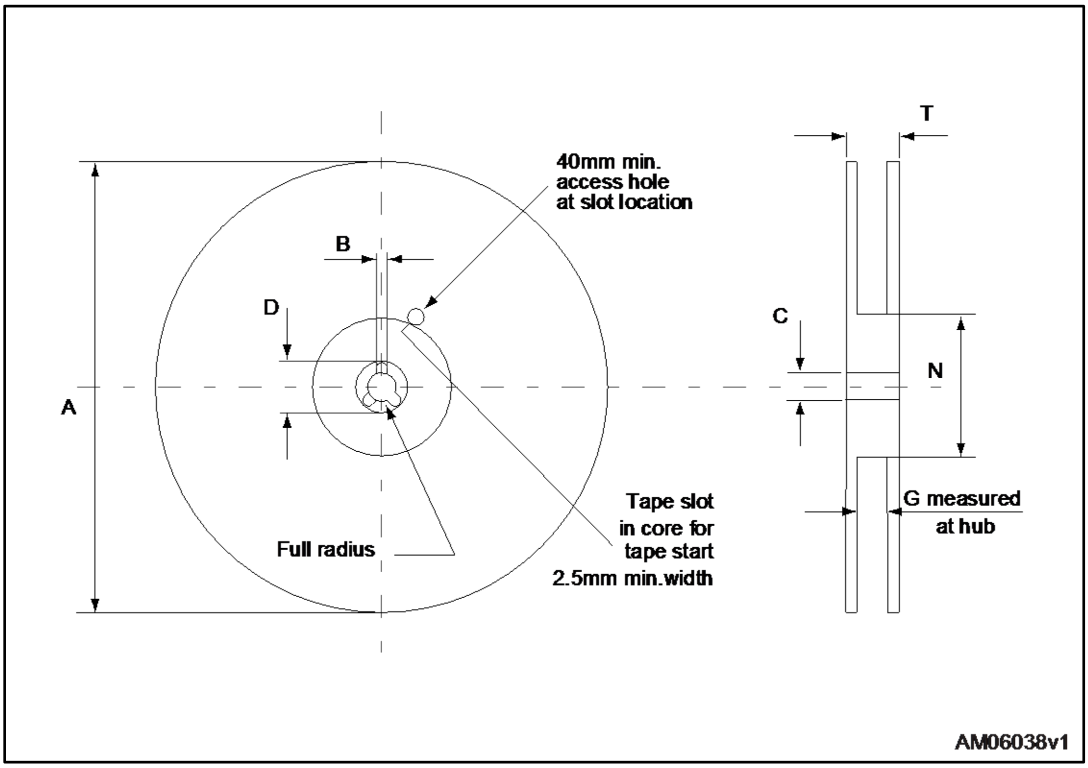


Table 13: D²PAK type A tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

6 Revision history

Table 14: Document revision history

Date	Revision	Changes
21-Oct-2014	1	First release.
05-Oct-2015	2	Text and formatting changes throughout document On cover page: - upated title and Features table In section Electrical ratings: - updated all table data In section Electrical characteristics: - updated all table data - renamed table Static (was On /off states) - added table Gate-source Zener diode Added section Electrical characteristics (curves) Updated and renamed section Package mechanical data (was Package information) Datasheet promoted from preliminary to production data
30-Oct-2015	3	Minor text changes in *Section 2.1: "Electrical characteristics (curves)*".
09-Dec-2015	4	Updated features and *Table 1: "Device summary"*.
24-Apr-2017	5	Updated features in cover page. Updated *Section 4: "Package information"* Minor text changes.