

N-channel 800 V, 0.15 Ω typ., 24 A, MDmesh™ K5 Power MOSFET in a D²PAK package

Datasheet - production data

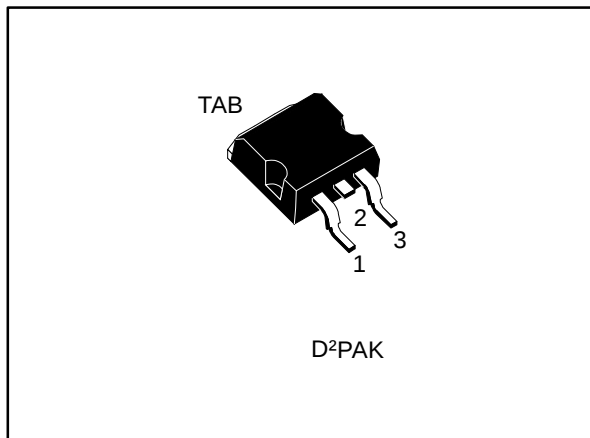
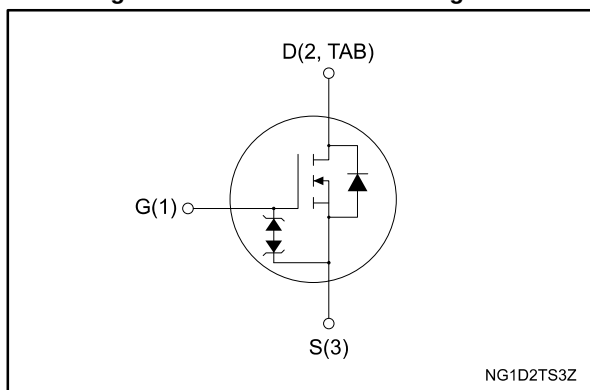


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STB30N80K5	800 V	0.18 Ω	24 A

- Industry's lowest R_{DS(on)} X area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

This very high voltage N-channel Power MOSFET is designed using MDmesh™ K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.

Table 1: Device summary

Order code	Marking	Package	Packaging
STB30N80K5	30N80K5	D ² PAK	Tape and reel

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	800	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	24	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	15	A
$I_{DM}^{(1)}$	Drain current (pulsed)	96	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	250	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature range	- 55 to 150	$^{\circ}\text{C}$
T_j	Operating junction temperature range		

Notes:

⁽¹⁾Pulse width limited by safe operating area.

⁽²⁾ $I_{SD} < 24\text{ A}$, $di/dt < 100\text{ A}/\mu\text{s}$, $V_{DSpeak} < V_{(BR)DSS}$, $V_{DD} = 80\% V_{(BR)DSS}$

⁽³⁾ $V_{DS} = 640\text{ V}$

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.5	$^{\circ}\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	30	$^{\circ}\text{C}/\text{W}$

Notes:

⁽¹⁾When mounted on FR-4 board of 1 inch², 2 oz Cu

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax} .)	8	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	440	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0 V	800			V
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 800 V			1	μA
		V _{GS} = 0 V, V _{DS} = 800 V, T _C = 125 °C ⁽¹⁾			50	μA
I _{GSS}	Gate source leakage current	V _{DS} = 0 V, V _{GS} = ± 20 V			±10	μA
V _{GS(th)}	Gate threshold voltage	V _{DD} = V _{GS} , I _D = 100 μA	3	4	5	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 12 A		0.15	0.18	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 100 V, f = 1 MHz, V _{GS} = 0 V	-	1530	-	pF
C _{oss}	Output capacitance		-	145	-	pF
C _{rss}	Reverse transfer capacitance		-	1.2	-	pF
C _{o(er)} ⁽¹⁾	Equivalent capacitance energy related	V _{GS} = 0 V, V _{DS} = 0 to 640 V	-	91	-	pF
C _{o(tr)} ⁽²⁾	Equivalent capacitance time related		-	244	-	pF
Q _g	Total gate charge	V _{DD} = 640 V, I _D = 24 A, V _{GS} = 10 V (see Figure 16: "Test circuit for gate charge behavior")	-	43	-	nC
Q _{gs}	Gate-source charge		-	12.8	-	nC
Q _{gd}	Gate-drain charge		-	24.2	-	nC
R _g	Gate input resistance	f = 1 MHz, I _D = 0 A	-	3.5	-	Ω

Notes:

⁽¹⁾Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

⁽²⁾Time related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DS} = 400\text{ V}$, $I_D = 12\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 15: "Test circuit for resistive load switching times")	-	21	-	ns
t_r	Rise time		-	15	-	ns
$t_{d(off)}$	Turn-off delay time		-	100	-	ns
t_f	Fall time		-	13.5	-	ns

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		24	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		96	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 24\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 24\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 17: "Test circuit for inductive load switching and diode recovery times")	-	555		ns
Q_{rr}	Reverse recovery charge		-	9.95		μC
I_{RRM}	Reverse recovery current		-	36		A
t_{rr}	Reverse recovery time	$I_{SD} = 24\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 17: "Test circuit for inductive load switching and diode recovery times")	-	765		ns
Q_{rr}	Reverse recovery charge		-	13.2		μC
I_{RRM}	Reverse recovery current		-	34.5		A

Notes:

⁽¹⁾Pulse width limited by safe operating area.

⁽²⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

Table 9: Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$, $I_D = 0\text{ A}$	30	-	-	V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

2.2 Electrical characteristics (curves)

Figure 2: Safe operating area

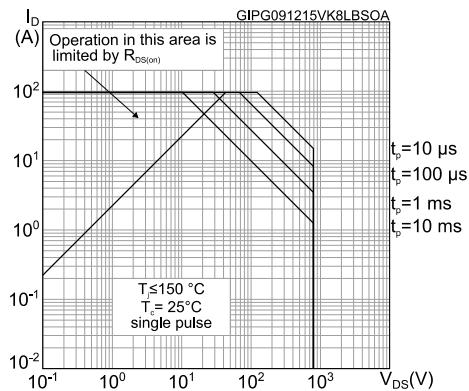


Figure 3: Thermal impedance

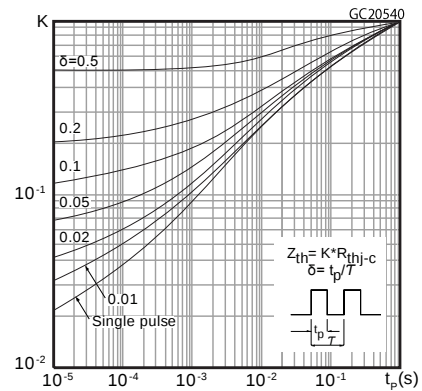


Figure 4: Output characteristics

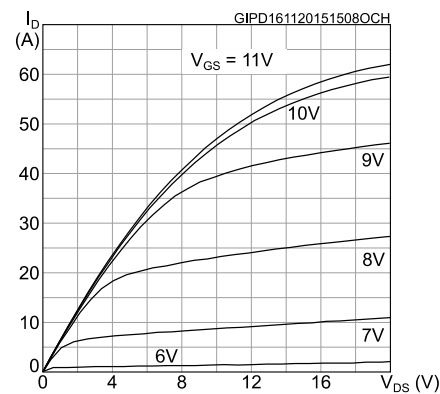


Figure 5: Transfer characteristics

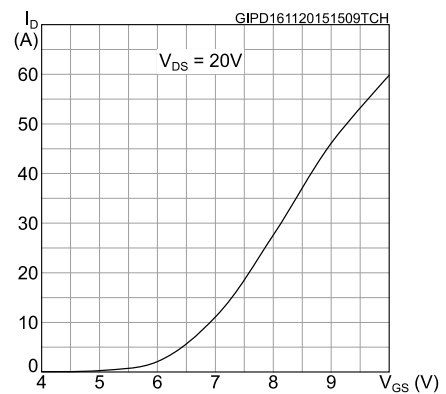


Figure 6: Gate charge vs gate-source voltage

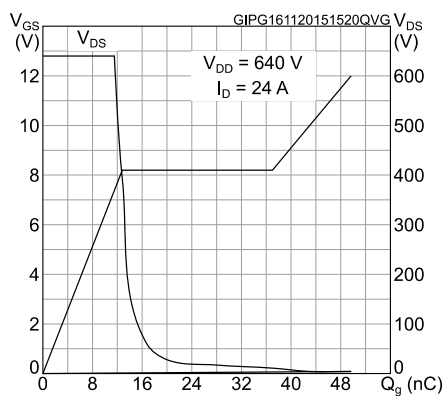


Figure 7: Static drain-source on-resistance

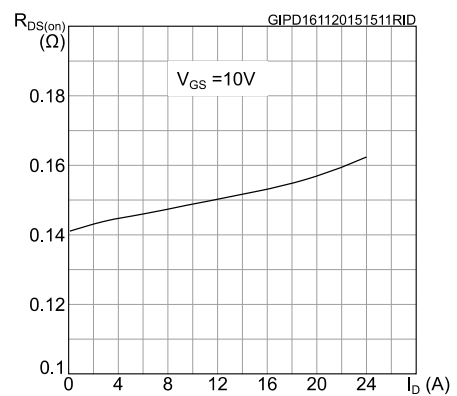


Figure 8: Capacitance variations

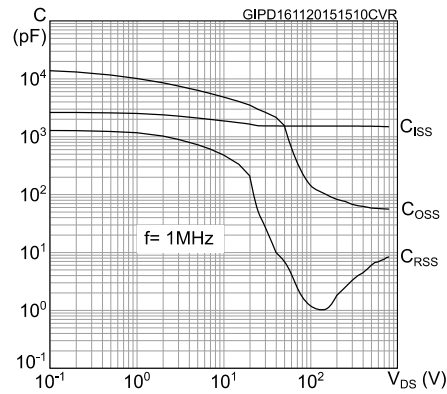


Figure 9: Normalized gate threshold voltage vs temperature

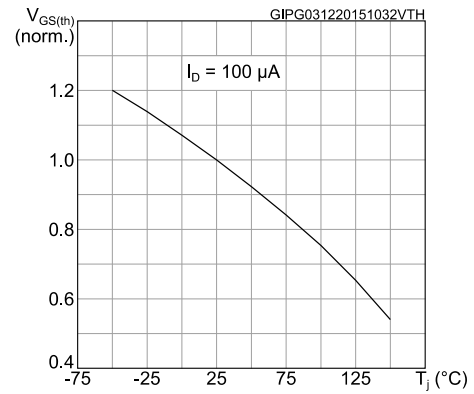


Figure 10: Normalized on-resistance vs temperature

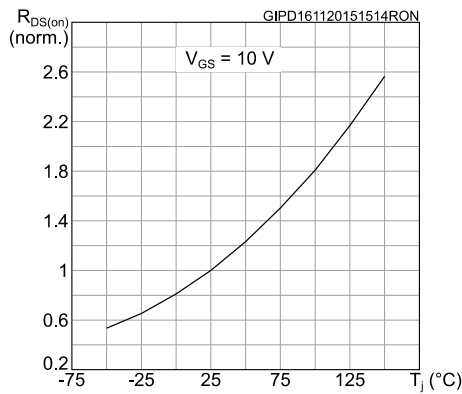
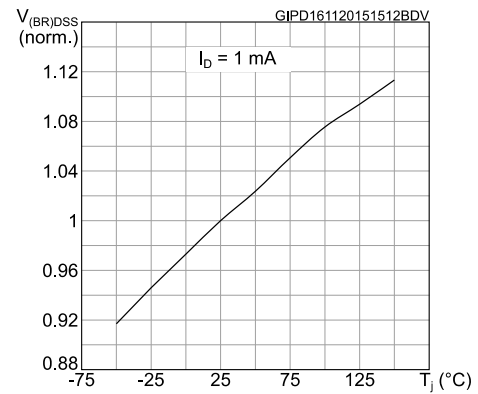
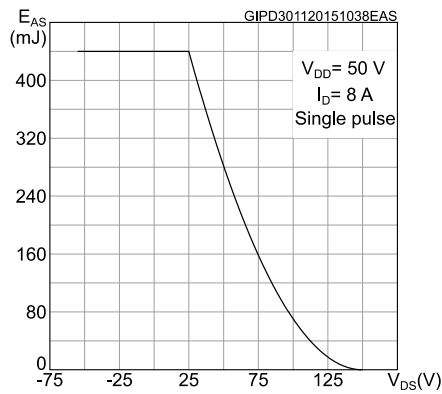
Figure 11: Normalized $V_{(BR)DSS}$ vs temperatureFigure 12: Maximum avalanche energy vs starting T_J 

Figure 13: Source-drain diode forward characteristics

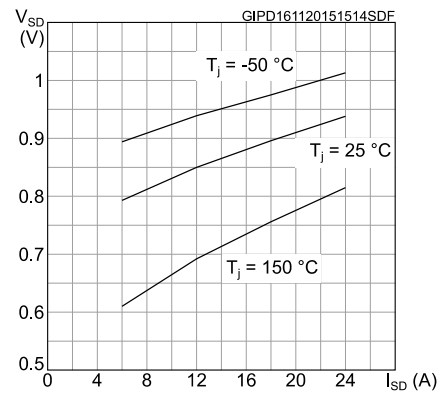
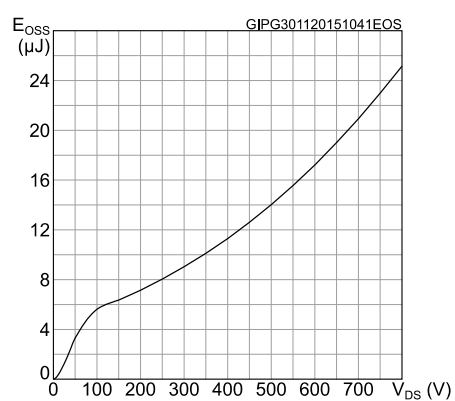
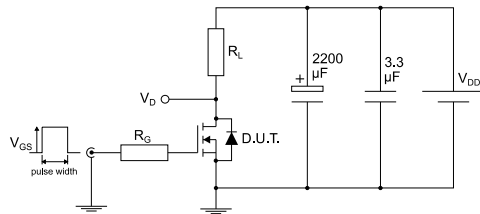


Figure 14: Output capacitance stored energy



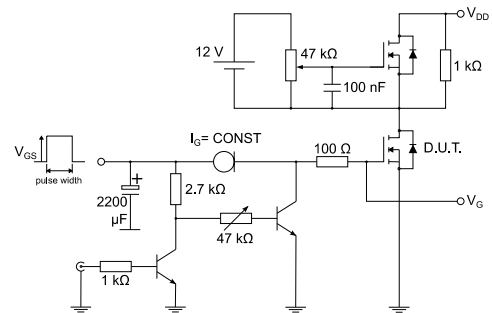
3 Test circuits

Figure 15: Test circuit for resistive load switching times



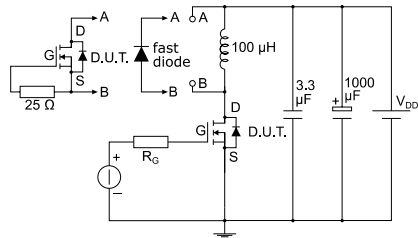
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Figure 16: Test circuit for gate charge behavior



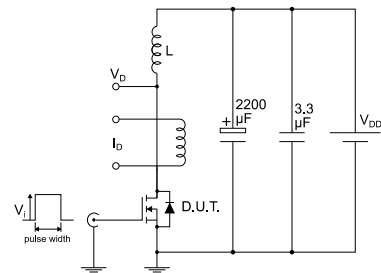
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Figure 17: Test circuit for inductive load switching and diode recovery times



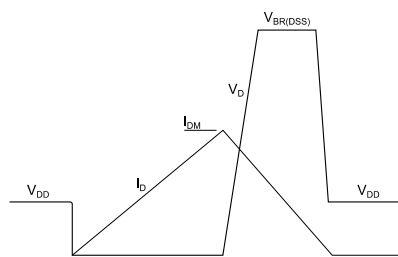
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Figure 18: Unclamped inductive load test circuit



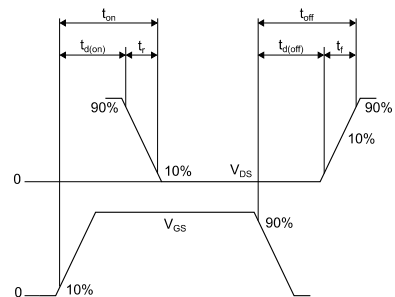
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Figure 19: Unclamped inductive waveform



AM01472v1

Figure 20: Switching time waveform



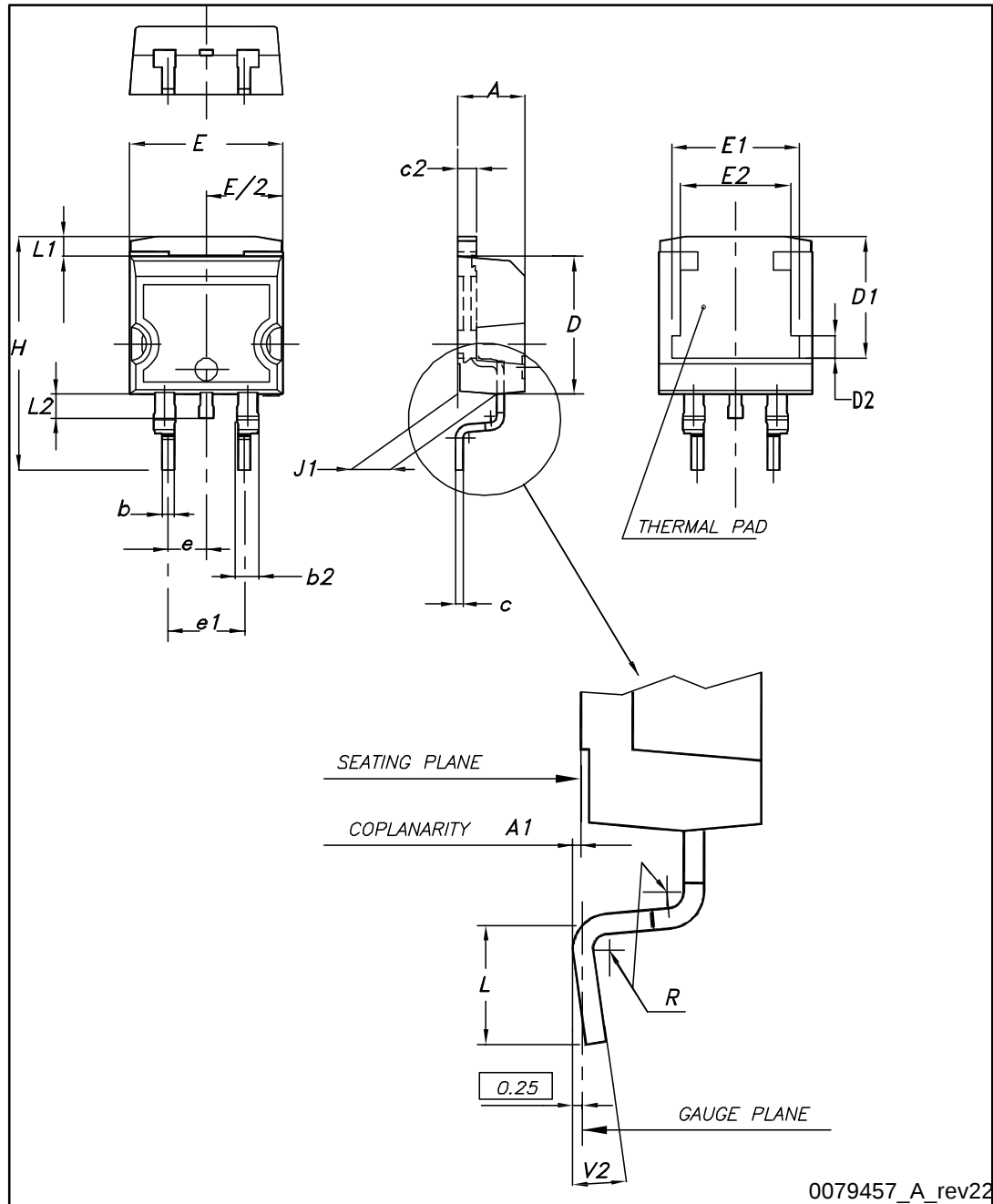
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 D²PAK package information

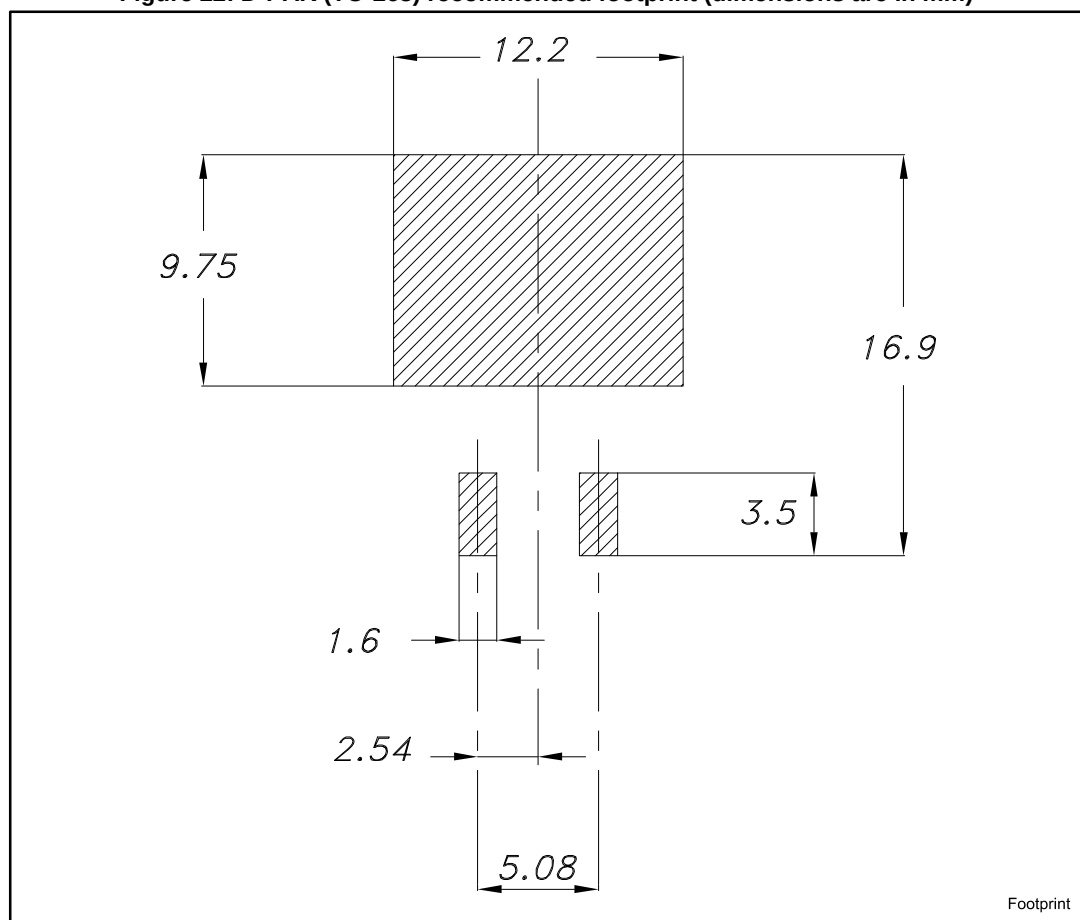
Figure 21: D²PAK (TO-263) type A package outline



0079457_A_rev22

Table 10: D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 22: D²PAK (TO-263) recommended footprint (dimensions are in mm)

4.2 D²PAK packaging information

Figure 23: Tape outline

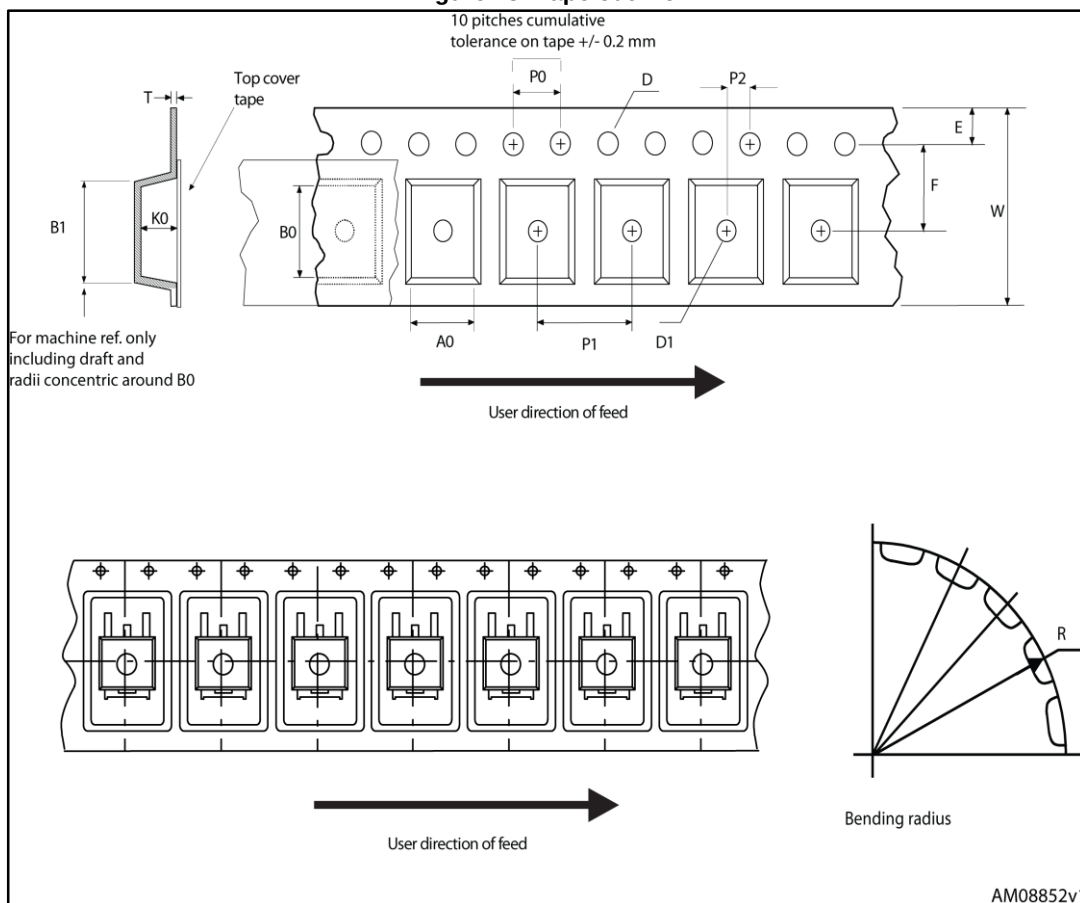
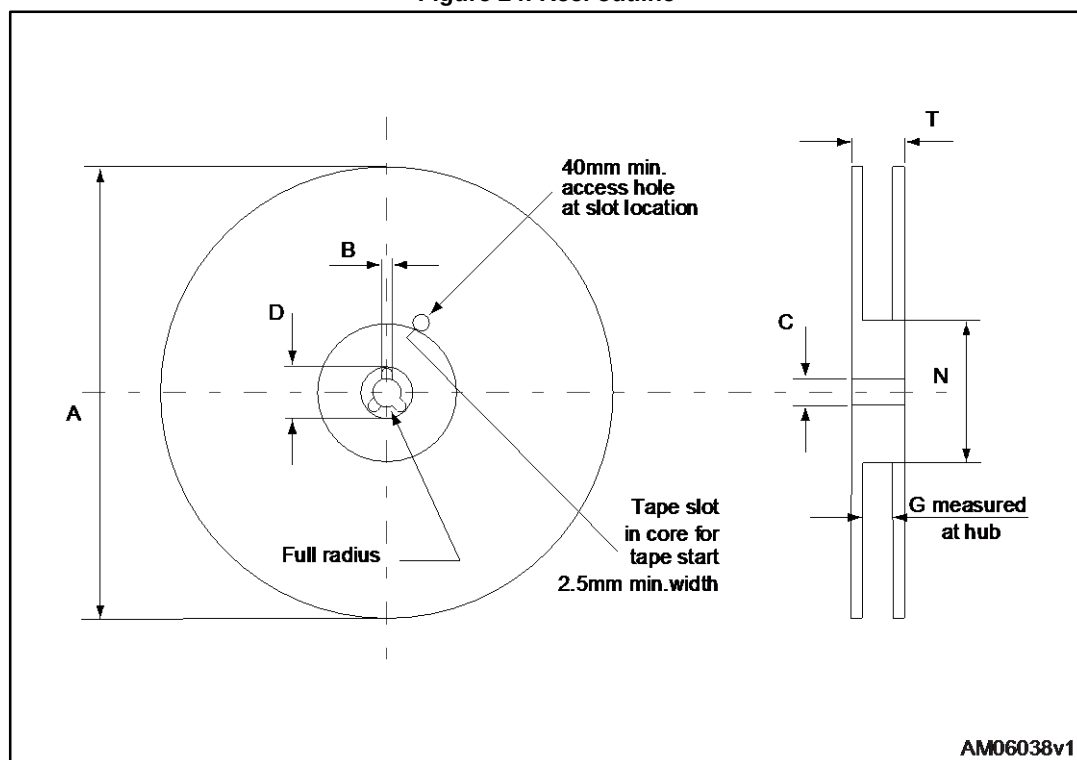


Figure 24: Reel outline

Table 11: D²PAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

5 Revision history

Table 12: Document revision history

Date	Revision	Changes
14-Dec-2015	1	First release.
06-Jul-2016	2	Modified: features in cover page. Added: note in Table 5: "On/off states" . Modified: Figure 3: "Thermal impedance" . Minor text changes.

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