

STB40NF10L

N-channel 100V - 0.028Ω - 40A - D²PAK Low gate charge STripFET™ II Power MOSFET

General features

Туре	V _{DSS}	R _{DS(on)}	Ι _D
STB40NF10L	100V	<0.033Ω	40A

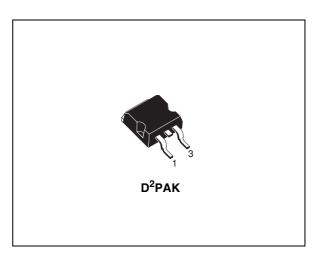
- Exceptional dv/dt capability
- 100% avalanche tested
- Application oriented characterization

Description

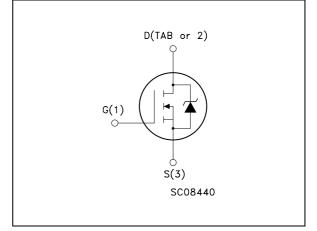
This Power MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced highefficiency isolated DC-DC converters for Telecom and Computer application. It is also intended for any application with low gate charge drive requirements.

Applications

Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STB40NF10L	B40NF10L	D ² PAK	Tape & reel

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Electrical ratings

Table 1.	Absolute max	imum ratings
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Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage ($V_{GS} = 0$)	100	V
V _{DGR}	Drain-gate voltage ($R_{GS} = 20 \text{ k}\Omega$)	100	V
V _{GS}	Gate- source voltage	± 15	V
I _D	Drain current (continuous) at $T_C = 25^{\circ}C$	40	А
۱ _D	Drain current (continuous) at $T_C = 100^{\circ}C$	25	А
I _{DM} ⁽¹⁾	Drain current (pulsed)	160	А
P _{tot}	Total dissipation at $T_C = 25^{\circ}C$	150	W
	Derating Factor	1	W/°C
E _{AS} ⁽²⁾	Single pulse avalanche energy	430	mJ
T _{stg}	Storage temperature	-65 to 175	°C
Тj	Max. operating junction temperature	-05 10 175	U

1. Pulse width limited by safe operating area.

2. Starting $T_j = 25 \text{ °C}$, $I_D = 20A$, $V_{DD} = 40V$

Table 2. Thermal data

Rthj-case	Thermal resistance junction-case max	1	°C/W
Rthj-amb	Thermal resistance junction-ambient max	62.5	°C/W
TJ	Maximum lead temperature for soldering purpose	300	°C

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 250µA, V _{GS} =0	100			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, T_{C} = 125°C			1 10	μΑ μΑ
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	$V_{GS} = \pm 20V$			±100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1	1.7	2.5	V
R _{DS(on)}	Static drain-source on resistance	$V_{GS} = 10V$, $I_D = 20A$ $V_{GS} = 5V$, $I_D = 20A$		0.028 0.030	0.033 0.036	Ω Ω

Table 3. On/off states

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
g _{fs} ⁽¹⁾	Forward transconductance	V _{DS} = 15V _, I _D = 20A		25		S
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V _{DS} = 25V, f = 1MHz, V _{GS} = 0		2300 290 125		pF pF pF
t _{d(on)} t _r t _{d(off)} t _f	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 50V, I_D = 20A$ $R_G = 4.7\Omega V_{GS} = 4.5V$ (see <i>Figure 13</i>)		25 82 64 24		ns ns ns ns
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 80V, I_D = 40A,$ $V_{GS} = 4.5V, R_G = 4.7\Omega$ (see <i>Figure 14</i>)		46 12 22	64	nC nC nC

1. Pulsed: Pulse duration = 300 μ s, duty cycle 1.5 %.

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD} I _{SDM} ⁽¹⁾	Source-drain current Source-drain current (pulsed)				40 160	A A
V _{SD} ⁽²⁾	Forward on voltage	I _{SD} = 40A, V _{GS} = 0			1.3	V
t _{rr} Q _{rr} I _{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 40A, di/dt = 100A/\mu s,$ $V_{DD} = 30V, T_j = 150^{\circ}C$ (see <i>Figure 15</i>)		110 467 8		ns nC A

Table 5.Source drain diode

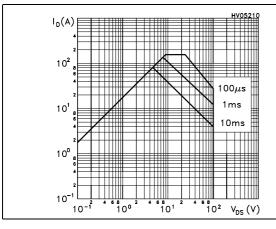
1. Pulse width limited by safe operating area.

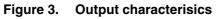
2. Pulsed: Pulse duration = 300 μ s, duty cycle 1.5 %

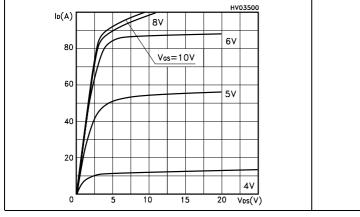


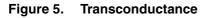
2.1 Electrical characteristics (curves)

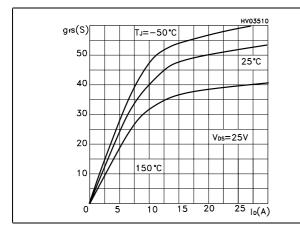
Figure 1. Safe operating area



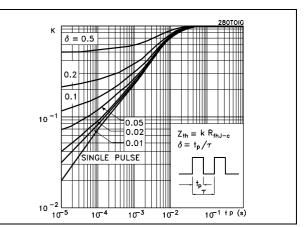














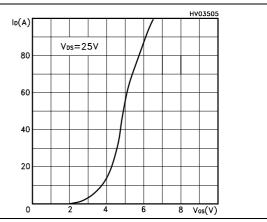
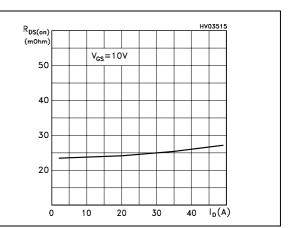
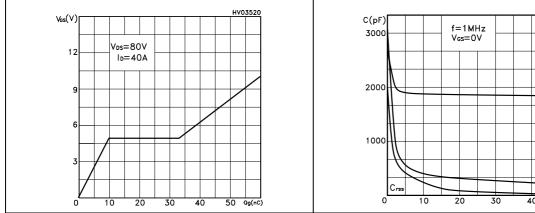


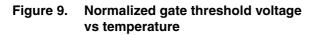
Figure 6. Static drain-source on resistance



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Gate charge vs gate-source voltage Figure 8. Capacitance variations Figure 7.



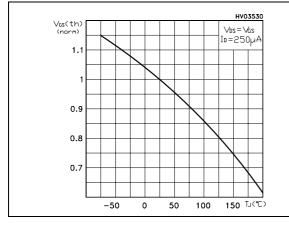


Figure 11. Source-drain diode forward characteristics

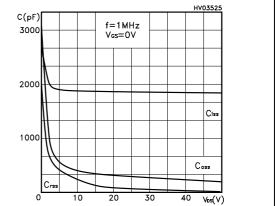


Figure 10. Normalized on resistance vs temperature

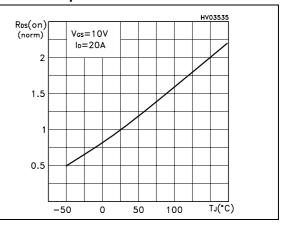
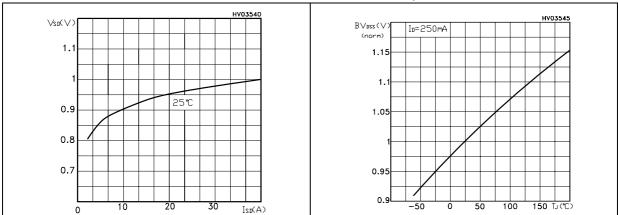


Figure 12. Normalized breakdown voltage vs temperature



3 Test circuit

Figure 13. Switching times test circuit for resistive load

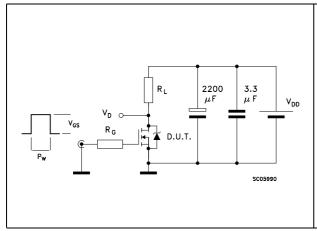


Figure 15. Test circuit for inductive load switching and diode recovery times

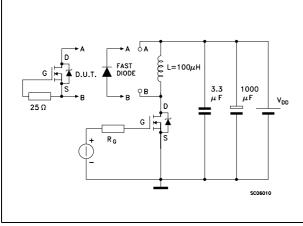


Figure 17. Unclamped inductive waveform

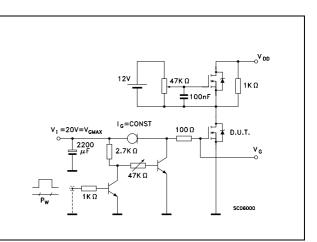
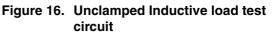


Figure 14. Gate charge test circuit



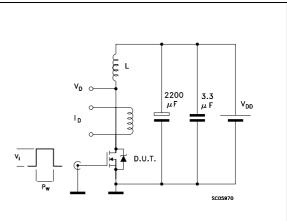
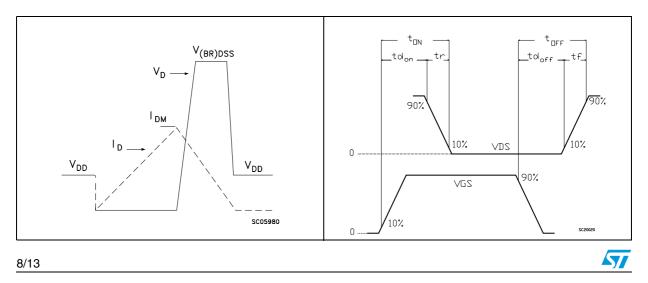


Figure 18. Switching time waveform



4 Package mechanical data

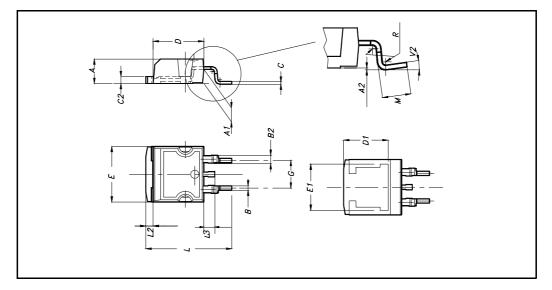
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com



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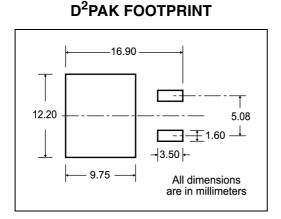
DIM.		mm.			inch	
	MIN.	ТҮР	MAX.	MIN.	TYP.	MAX
А	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
В	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
С	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
М	2.4		3.2	0.094		0.126
R		0.4			0.015	

D²PAK MECHANICAL DATA

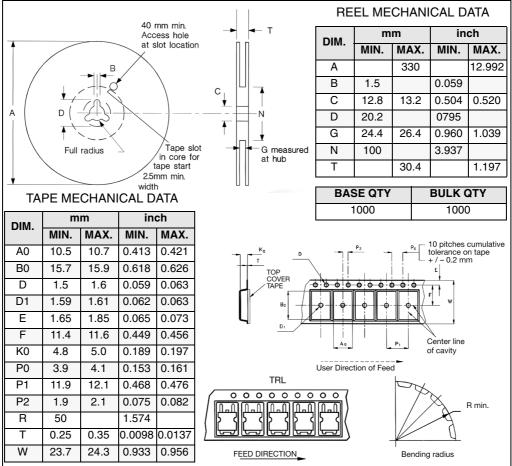


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Packing mechanical data



TAPE AND REEL SHIPMENT



* on sales type



6 Revision history

Date	Revision	Changes
21-Jun-2004	1	First release
26-Jun-2006	2	New template, no content change



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