STB42N60M2-EP, STP42N60M2-EP, STW42N60M2-EP

N-channel 600 V, 0.076 Ω typ., 34 A MDmesh™ M2 EP Power MOSFETs in D²PAK, TO-220 and TO-247 packages

Datasheet - production data

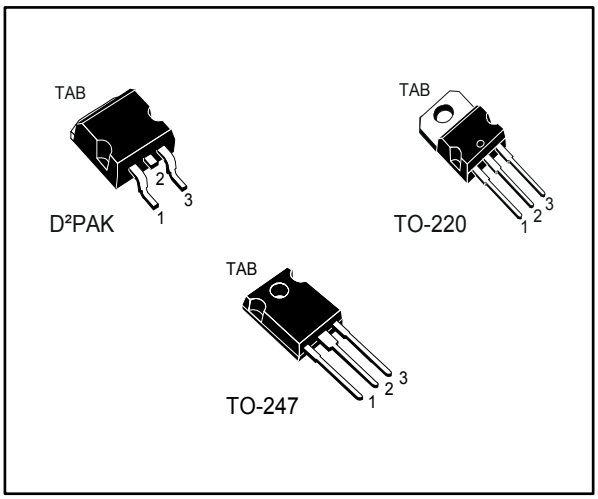
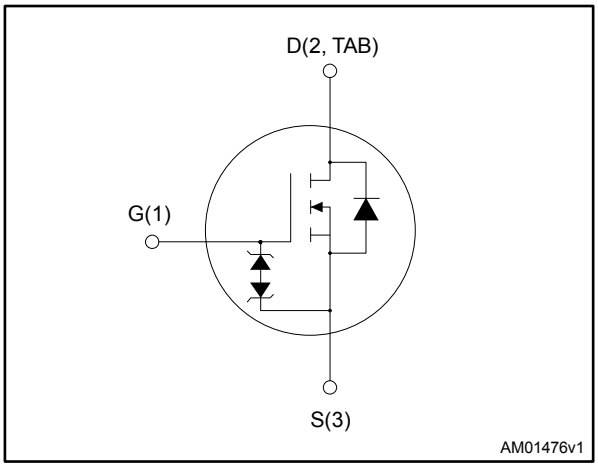


Figure 1: Internal schematic diagram



Features

Order code	V_{DS} @ T_{Jmax}	$R_{DS(on)}$ max.	I_D
STB42N60M2-EP	650 V	0.087 Ω	34 A
STP42N60M2-EP			
STW42N60M2-EP			

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- Very low turn-off switching losses
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications
- Tailored for very high frequency converters (f > 150 kHz)

Description

These devices are N-channel Power MOSFETs developed using MDmesh™ M2 EP enhanced performance technology. Thanks to their strip layout and improved vertical structure, the devices exhibit low on-resistance and optimized switching characteristics with very low turn-off switching losses, rendering them suitable for the most demanding very high frequency converters.

Table 1: Device summary

Order code	Marking	Package	Packing
STB42N60M2-EP	42N60M2EP	D²PAK	Tape and reel
STP42N60M2-EP		TO-220	Tube
STW42N60M2-EP		TO-247	

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at T_C = 25 °C	34	A
I_D	Drain current (continuous) at T_C = 100 °C	22	A
I_{DM}(1)	Drain current (pulsed)	136	A
P_{TOT}	Total dissipation at T_C = 25 °C	250	W
dv/dt(2)	Peak diode recovery voltage slope	15	V/ns
dv/dt(3)	MOSFET dv/dt ruggedness	50	V/ns
T_{stg}	Storage temperature range	- 55 to 150	°C
T_j	Operating junction temperature range		°C

Notes:

(1)Pulse width limited by safe operating area.

(2)I_{SD} ≤ 34 A, di/dt ≤ 400 A/µs; $V_{DS(peak)}$ < $V_{(BR)DSS}$, V_{DD} = 400 V.

(3)V_{DS} ≤ 480 V

Table 3: Thermal data

Symbol	Parameter	Value			Unit
		D²PAK	TO-220	TO-247	
$R_{thj\text{-}case}$	Thermal resistance junction-case	0.5			°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb	30			°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient		62.5	50	°C/W

Notes:

(1)When mounted on FR-4 board of inch², 2oz Cu.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetetive or not repetitive (pulse width limited by T_{jmax})	6	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}; V_{DD} = 50 V)	800	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 5: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage Drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C(1)			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 17 A		0.076	0.087	Ω

Notes:

(1)Defined by design, not subject to production test

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	2370	-	pF
C_{oss}	Output capacitance		-	112	-	pF
C_{rss}	Reverse transfer capacitance		-	2.5	-	pF
$C_{oss\ eq.}$(1)	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	454	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	4.5	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 34 A, V_{GS} = 0 to 10 V (see *Figure 18: "Test circuit for gate charge behavior"*)	-	55	-	nC
Q_{gs}	Gate-source charge		-	8.5	-	nC
Q_{gd}	Gate-drain charge		-	25	-	nC

Notes:

(1)$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 7: Switching energy

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$E_{(off)}$	Turn-off energy (from 90% V_{GS} to 0% I_D)	V_{DD} = 400 V, I_D = 2.5 A, R_G = 4.7 Ω, V_{GS} = 10 V	–	13	–	µJ
		V_{DD} = 400 V, I_D = 5 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	14.5	-	µJ

Table 8: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 17 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 17: "Test circuit for resistive load switching times"* and *Figure 22: "Switching time waveform"*)	-	16.5	-	ns
t_r	Rise time		-	9.5	-	ns
$t_{d(off)}$	Turn-off-delay time		-	96.5	-	ns
t_f	Fall time		-	8	-	ns

Table 9: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		34	A
I_{SDM} (1)	Source-drain current (pulsed)		-		136	A
V_{SD} (2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 34 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 34 A, di/dt = 100 A/µs, V_{DD} = 60 V (see *Figure 19: "Test circuit for inductive load switching and diode recovery times"*)	-	438		ns
Q_{rr}	Reverse recovery charge		-	9		µC
I_{RRM}	Reverse recovery current		-	41.5		A
t_{rr}	Reverse recovery time	I_{SD} = 34 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_j = 150 °C (see *Figure 19: "Test circuit for inductive load switching and diode recovery times"*)	-	538		ns
Q_{rr}	Reverse recovery charge		-	12		µC
I_{RRM}	Reverse recovery current		-	44.5		A

Notes:

(1)Pulse width is limited by safe operating area

(2)Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area for D²PAK and TO-220

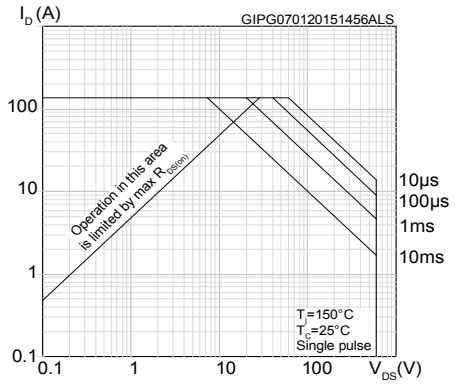


Figure 3: Thermal impedance for D²PAK and TO-220

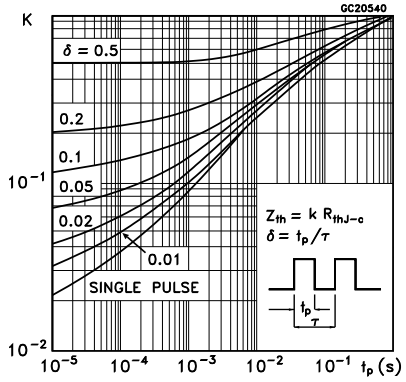


Figure 4: Safe operating area for TO-247

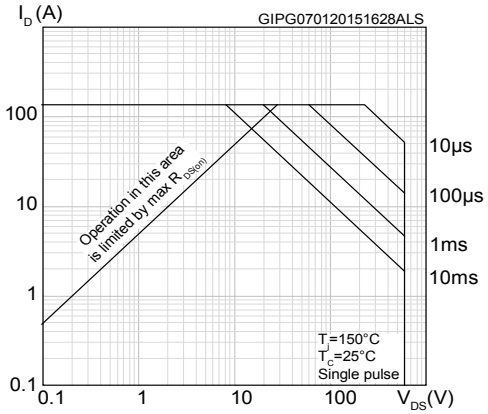


Figure 5: Thermal impedance for TO-247

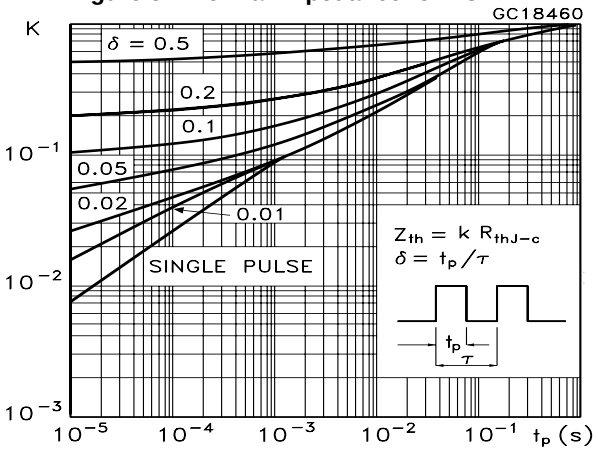


Figure 6: Output characteristics

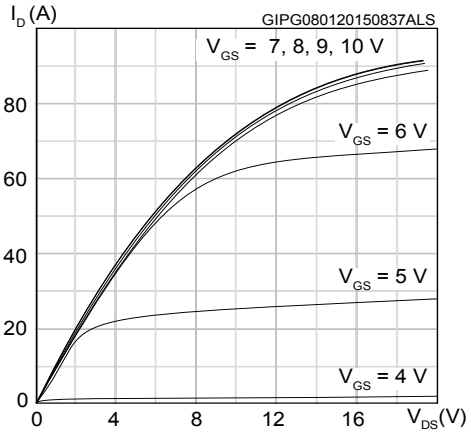


Figure 7: Transfer characteristics

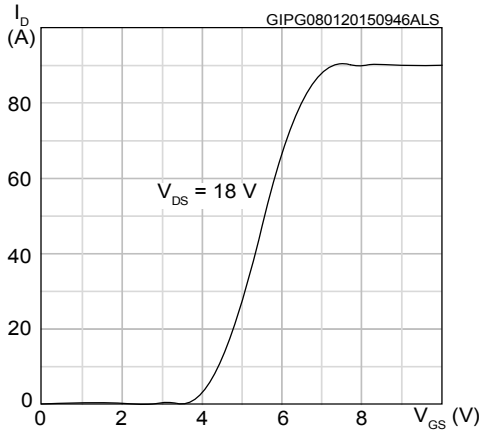


Figure 8: Gate charge vs gate-source voltage

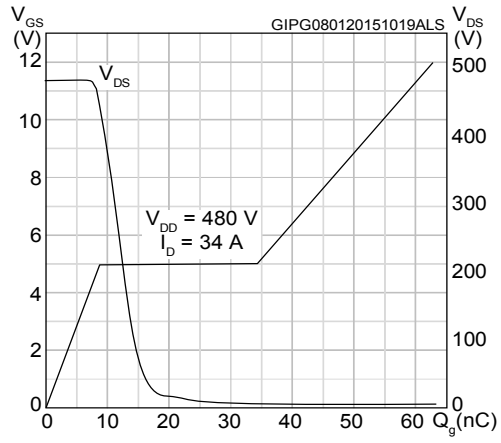


Figure 9: Static drain-source on-resistance

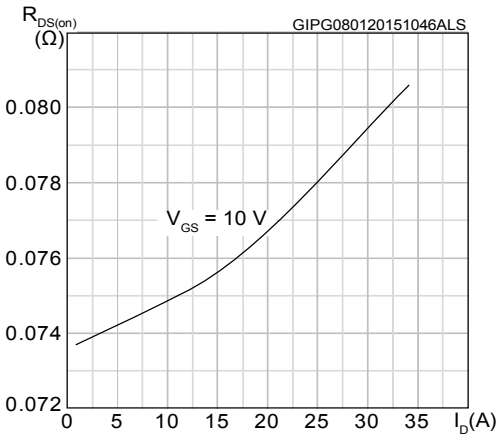


Figure 10: Capacitance variations

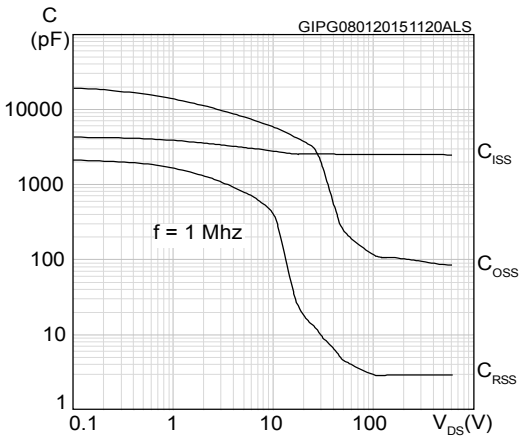


Figure 11: Output capacitance stored energy

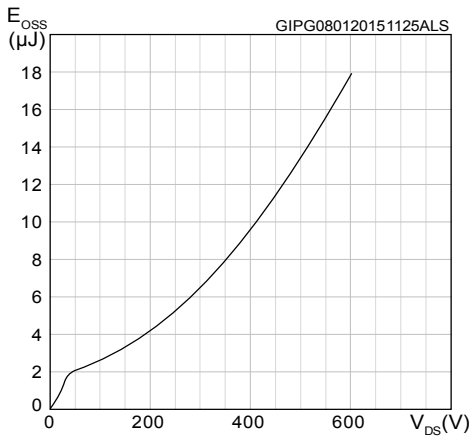


Figure 12: Turn-off switching energy vs drain current

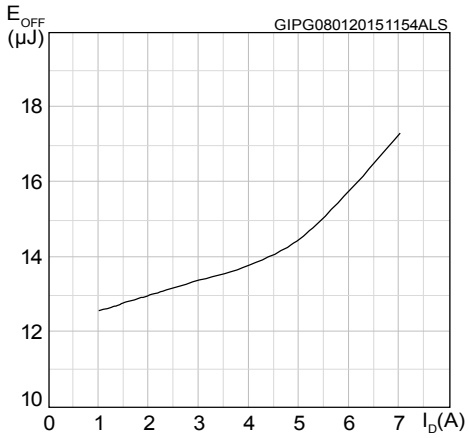


Figure 13: Normalized gate threshold voltage vs temperature

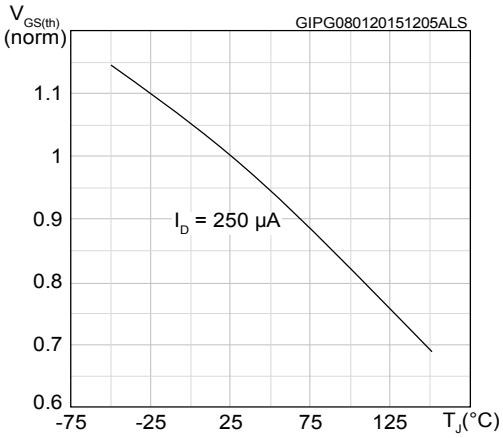


Figure 14: Normalized on-resistance vs temperature

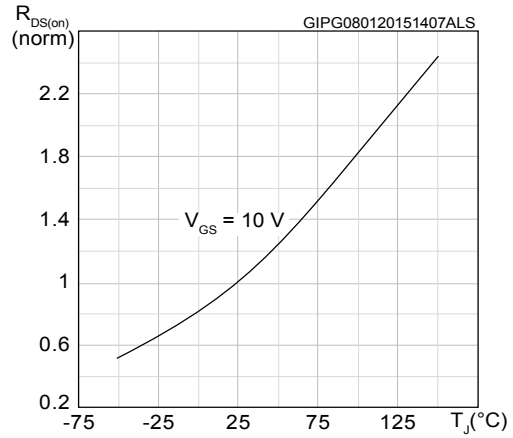


Figure 15: Source-drain diode forward characteristics

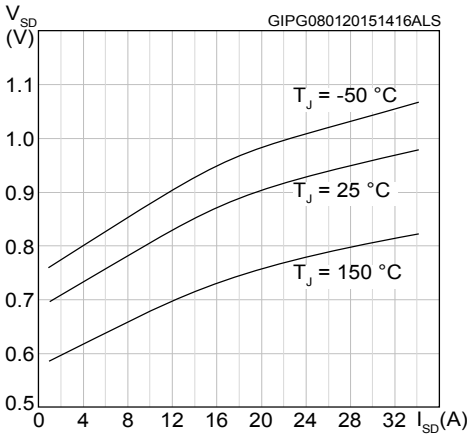
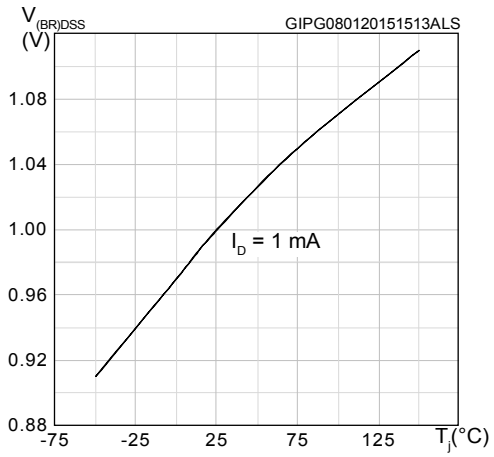


Figure 16: Normalized V(BR)DSS vs temperature



3 Test circuits

Figure 17: Test circuit for resistive load switching times

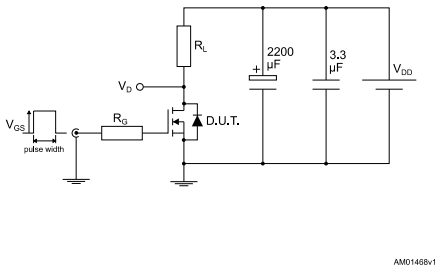


Figure 18: Test circuit for gate charge behavior

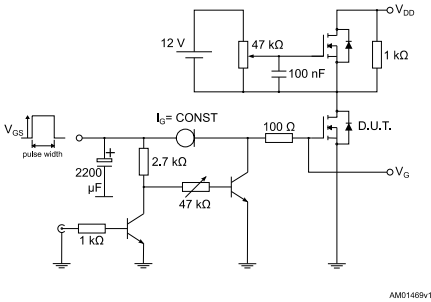


Figure 19: Test circuit for inductive load switching and diode recovery times

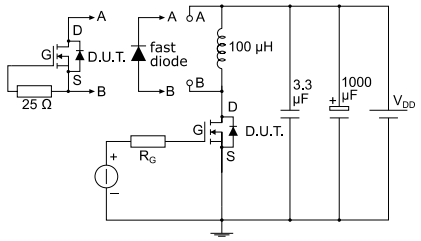


Figure 20: Unclamped inductive load test circuit

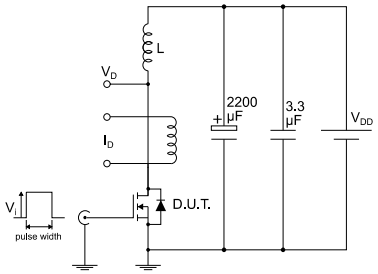


Figure 21: Unclamped inductive waveform

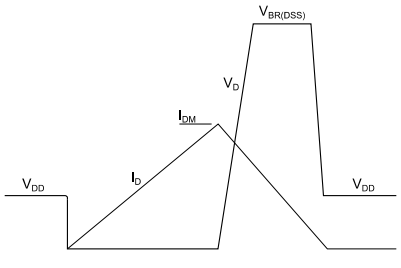
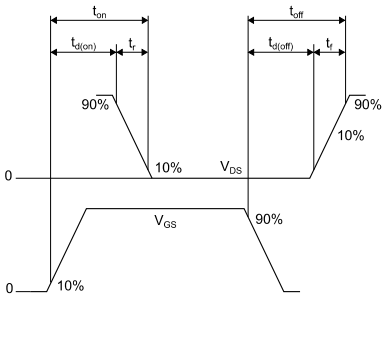


Figure 22: Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 D²PAK (TO-263) type A2 package information

Figure 23: D²PAK (TO-263) type A2 package outline

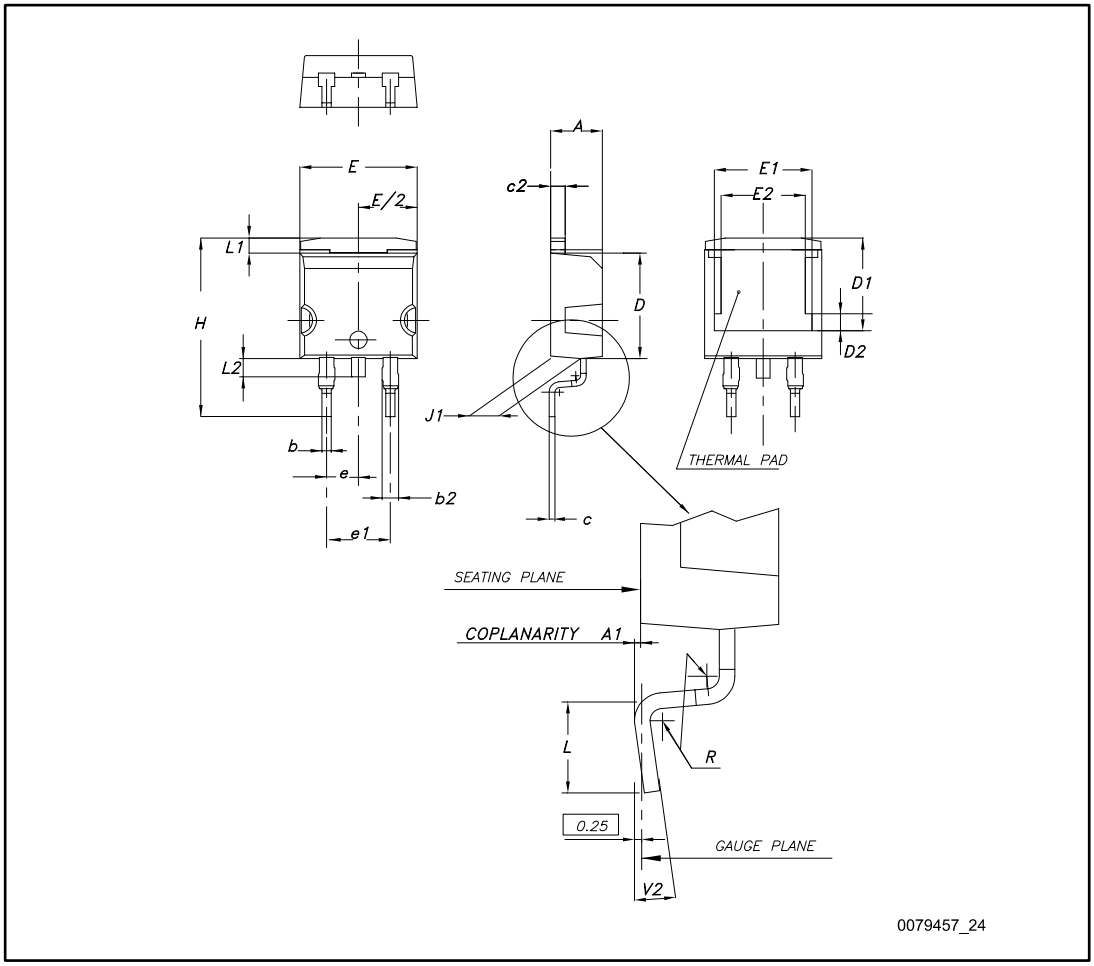
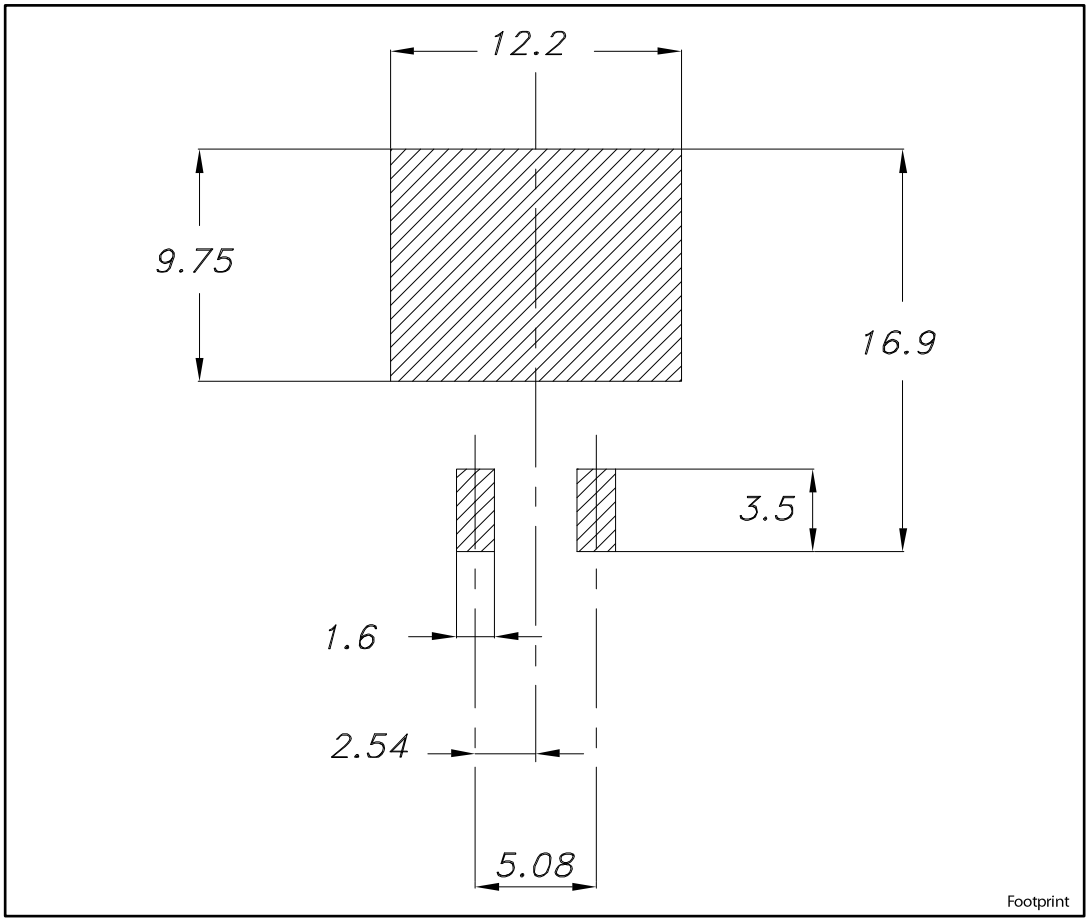


Table 10: D²PAK (TO-263) type A2 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.70	8.90	9.10
E2	7.30	7.50	7.70
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

Figure 24: D²PAK (TO-263) recommended footprint (dimensions are in mm)



4.2 TO-220 type A package information

Figure 25: TO-220 type A package outline

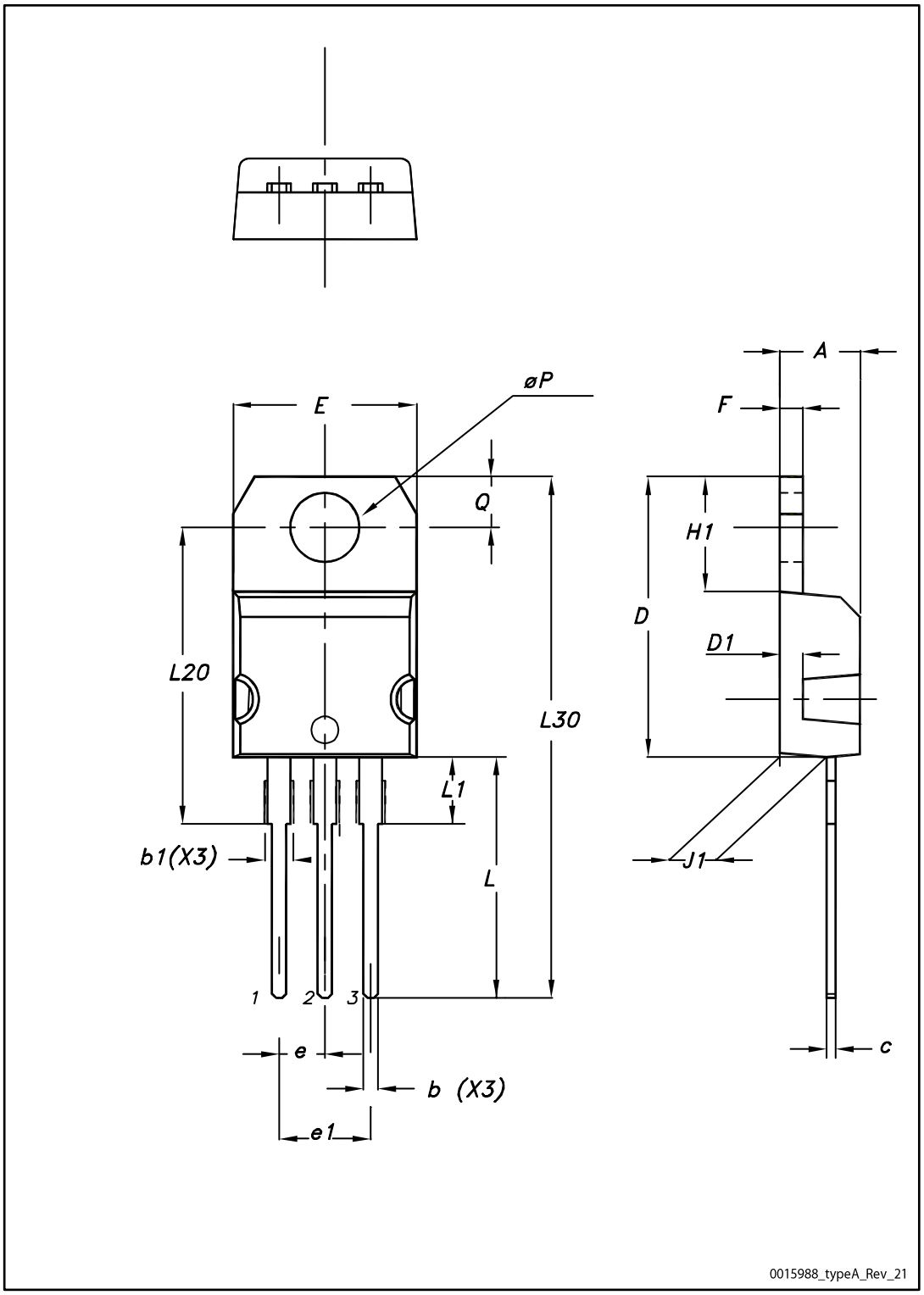


Table 11: TO-220 type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

4.3 TO-247 package information

Figure 26: TO-247 package outline

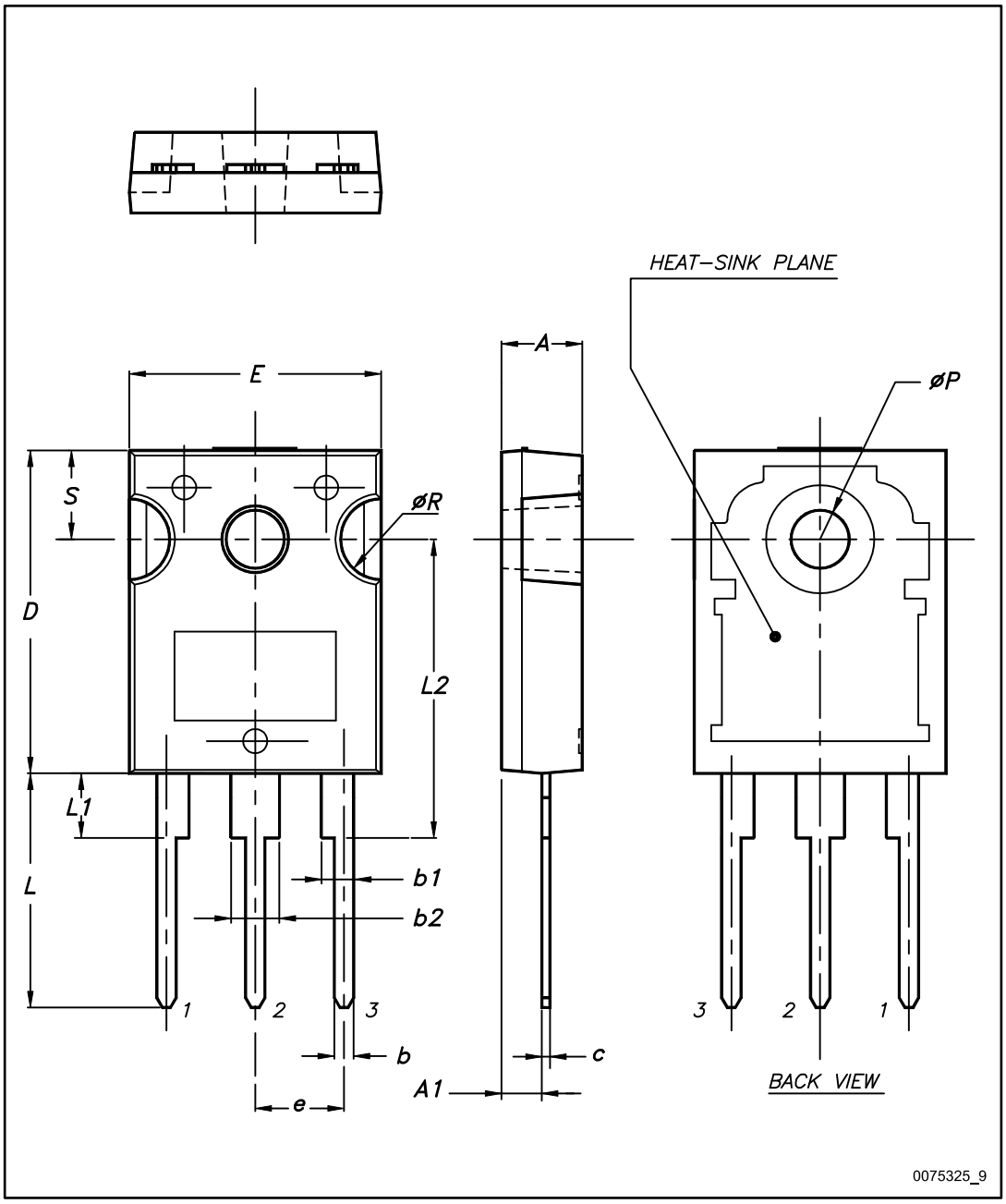


Table 12: TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

5 D²PAK packing information

Figure 27: D²PAK tape outline

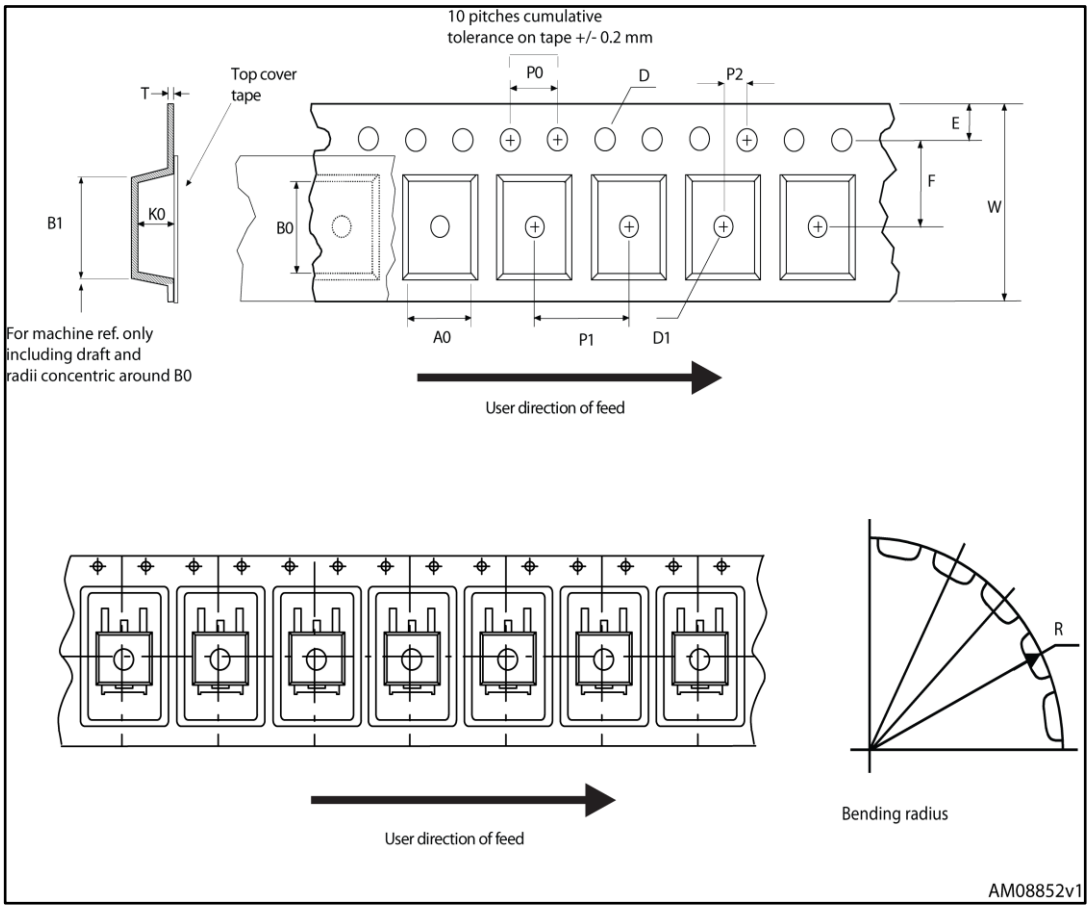


Figure 28: D²PAK reel outline

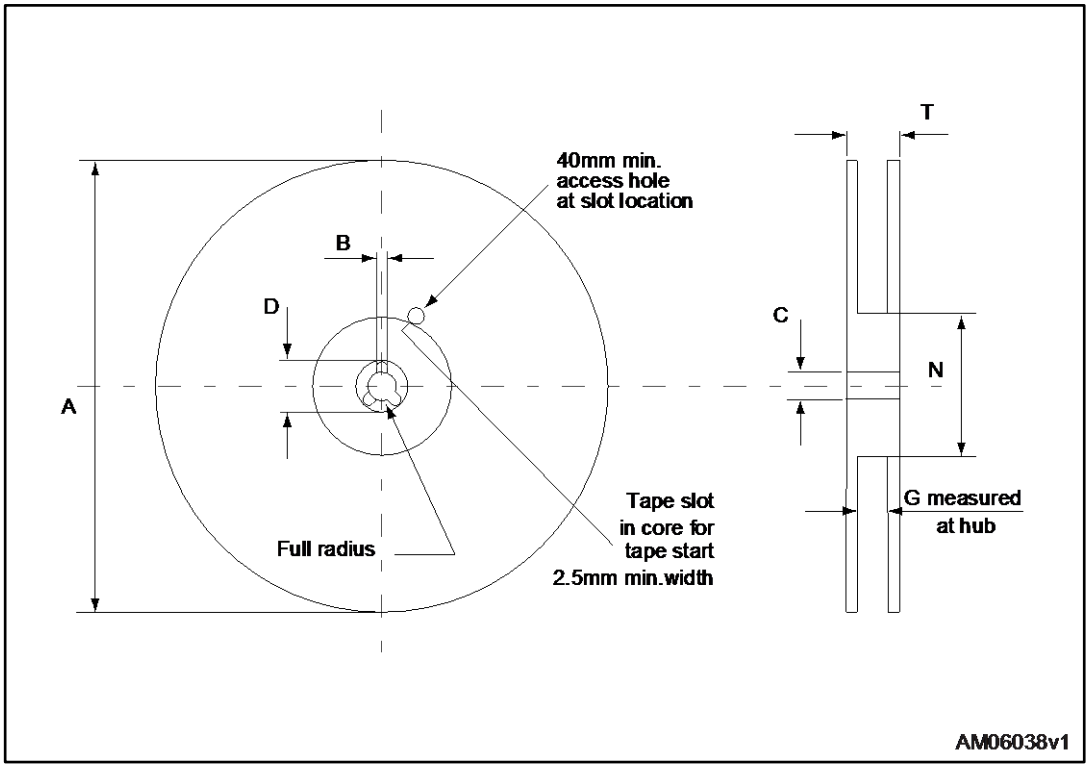


Table 13: D²PAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

6 Revision history

Table 14: Document revision history

Date	Revision	Changes
20-Jan-2015	1	First release.
03-Nov-2017	2	Updated *Section 4.1: "D²PAK (TO-263) type A2 package information"* and *Section 5: "D²PAK packing information"* Minor text changes.

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