

N-channel 300 V, 0.063 Ω typ., 42 A STripFET™ II
Power MOSFETs in D²PAK, TO-220 and TO-247 packages

Datasheet - production data

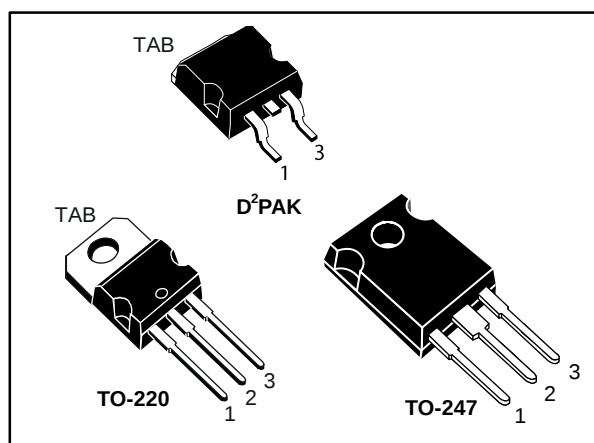
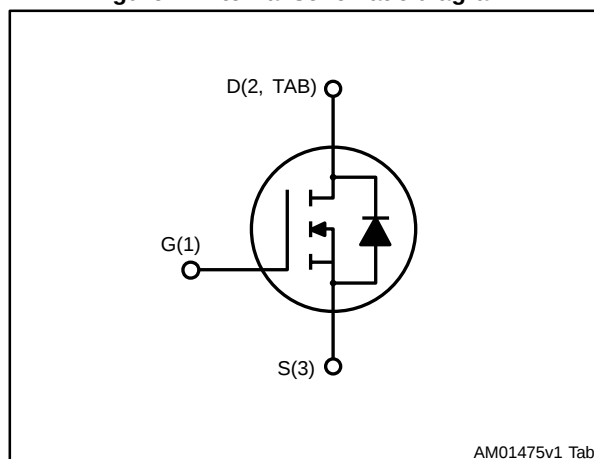


Figure 1: Internal schematic diagram



Features

Order code	V _{DSS}	R _{DS(on)} max.	I _D	P _w
STB46NF30	300 V	< 0.075 Ω	42 A	300 W
STP46NF30				
STW46NF30				

- Exceptional dv/dt capability
- 100% avalanche tested
- Low gate charge

Applications

- Switching applications

Description

These Power MOSFETs have been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the devices suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

Table 1: Device summary

Order code	Marking	Package	Packing
STB46NF30	46NF30	D ² PAK	Tape and reel
STP46NF30		TO-220	Tube
STW46NF30		TO-247	

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	300	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	42	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	27	A
$I_{DM}^{(1)}$	Drain current (pulsed)	168	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	300	W
	Derating factor	2	W/ $^{\circ}\text{C}$
$dv/dt^{(2)}$	Peak diode recovery voltage slope	10	V/ns
T_J	Operating junction temperature range	- 55 to 175	$^{\circ}\text{C}$
T_{stg}	Storage temperature range		

Notes:

(1) Pulse width limited by safe operating area.

(2) $I_{SD} \leq 34\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} = 80\% V_{(BR)DSS}$, $V_{DS\text{ peak}} < V_{(BR)DSS}$

Table 3: Thermal data

Symbol	Parameter	Value			Unit
		D ² PAK	TO-220	TO-247	
$R_{thj-case}$	Thermal resistance junction-case	0.5			$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	30	62.5	50	$^{\circ}\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	30			$^{\circ}\text{C}/\text{W}$
T_J	Maximum lead temperature for soldering purpose	300			$^{\circ}\text{C}$

Notes:(1) When mounted on FR-4 board of 1inch², 2oz Cu.

Table 4: Avalanche characteristics

Symbol	Parameter	Value	Unit
$I_{AR}^{(1)}$	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	26	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	290	mJ

Notes:(1) Pulse width limited by T_{jmax}

2 Electrical characteristics

$T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified

Table 5: On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$	300			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 300\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 300\text{ V}$ $T_C = 125\text{ }^{\circ}\text{C}$ ⁽¹⁾			10	μA
I_{GSS}	Gate body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 17\text{ A}$		0.063	0.075	Ω

Notes:

⁽¹⁾Defined by design, not subject to production test.

Table 6: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	3200	-	pF
C_{oss}	Output capacitance		-	442	-	pF
C_{rss}	Reverse transfer capacitance		-	57	-	pF
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 150\text{ V}$, $I_D = 17\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 16: "Test circuit for resistive load switching times")	-	25	-	ns
t_r	Rise time		-	38	-	ns
$t_{d(off)}$	Turn-off delay time		-	80	-	ns
t_f	Fall time		-	46	-	ns
Q_g	Total gate charge	$V_{DD} = 240\text{ V}$, $I_D = 34\text{ A}$ $V_{GS} = 10\text{ V}$ (see Figure 17: "Test circuit for gate charge behavior")	-	90	-	nC
Q_{gs}	Gate-source charge		-	16	-	nC
Q_{gd}	Gate-drain charge		-	40	-	nC

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		34	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		136	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 34\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 34\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see Figure 18: "Test circuit for inductive load switching and diode recovery times")	-	215		ns
Q_{rr}	Reverse recovery charge		-	1.7		μC
I_{RRM}	Reverse recovery current		-	16		A
t_{rr}	Reverse recovery time	$I_{SD} = 34\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 18: "Test circuit for inductive load switching and diode recovery times")	-	252		ns
Q_{rr}	Reverse recovery charge		-	2.3		μC
I_{RRM}	Reverse recovery current		-	19		A

Notes:⁽¹⁾Pulse width limited by safe operating area⁽²⁾Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.2 Electrical characteristics (curves)

Figure 2: Safe operating area for D²PAK and TO-220

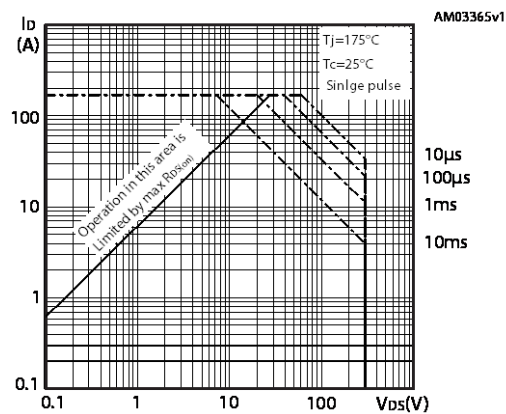


Figure 3: Thermal impedance for D²PAK and TO-220

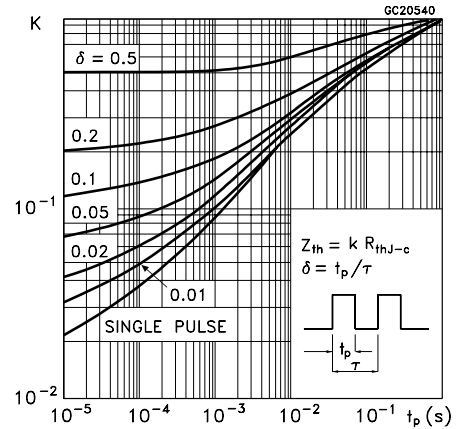


Figure 4: Safe operating area for TO-247

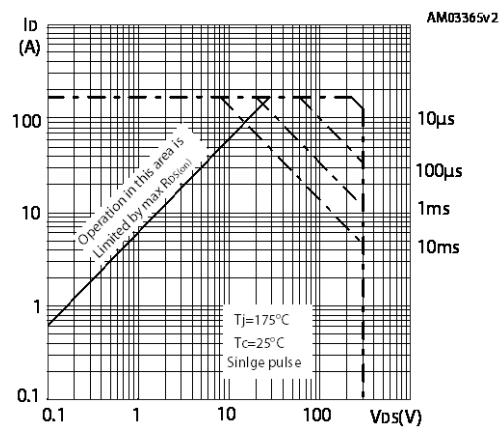


Figure 5: Thermal impedance for TO-247

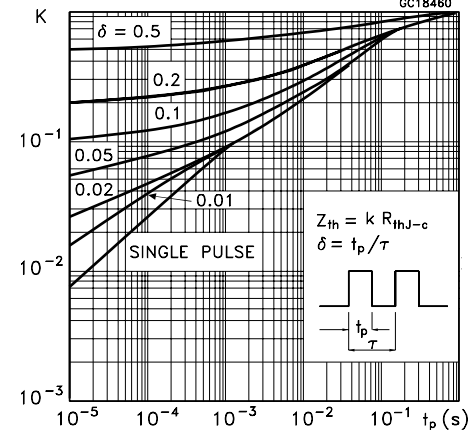


Figure 6: Output characteristics

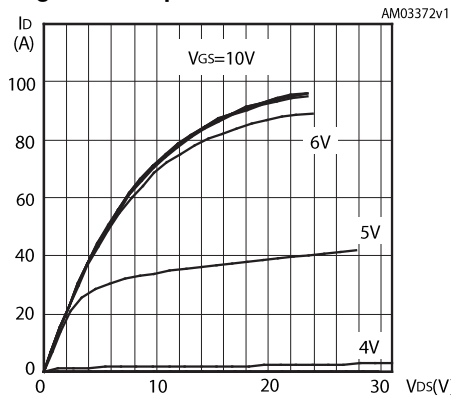


Figure 7: Transfer characteristics

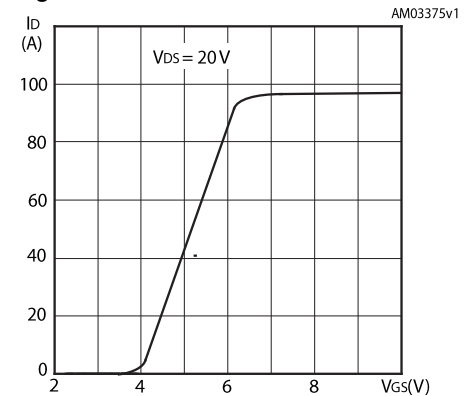


Figure 8: Gate charge vs gate-source voltage

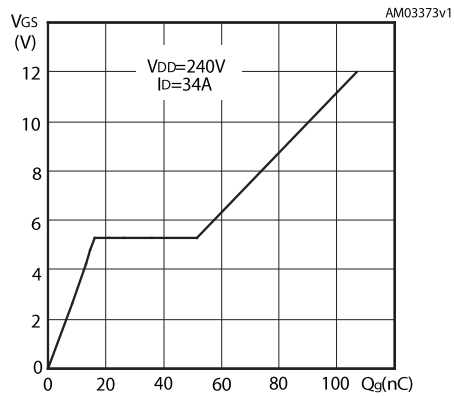


Figure 9: Static drain-source on-resistance

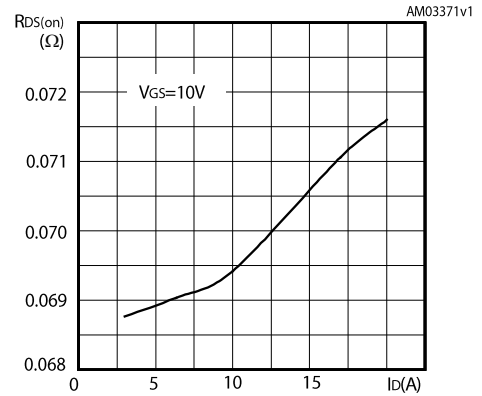


Figure 10: Capacitance variations

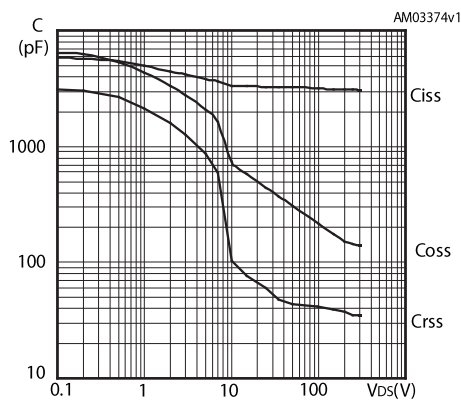


Figure 11: Normalized gate threshold voltage vs temperature

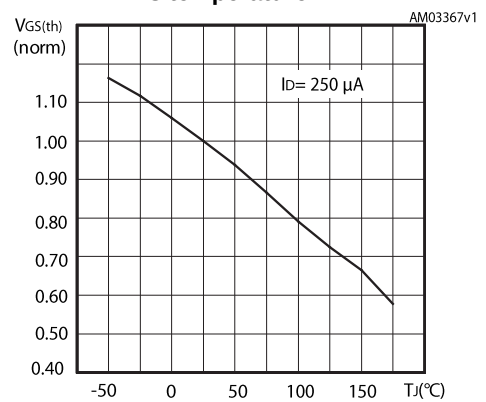


Figure 12: Normalized on-resistance vs temperature

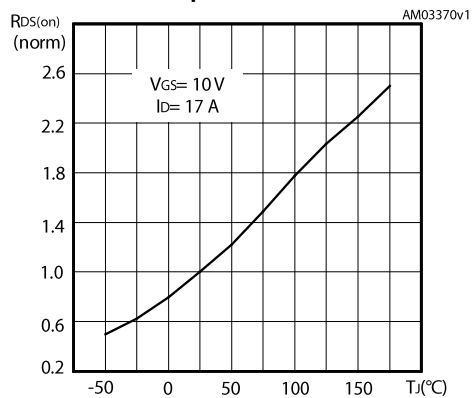
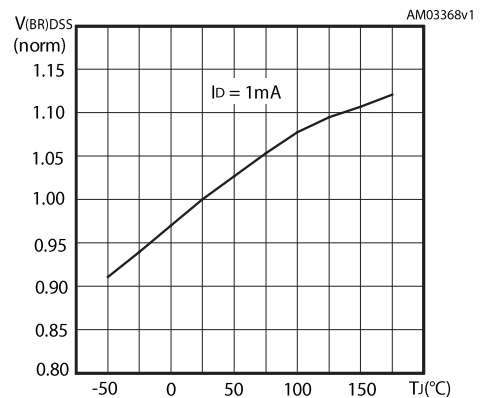
Figure 13: Normalized $V_{(BR)DSS}$ vs temperature

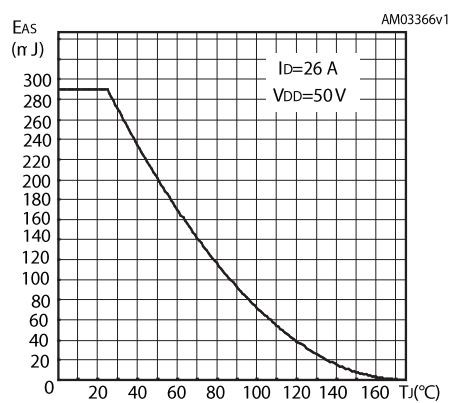
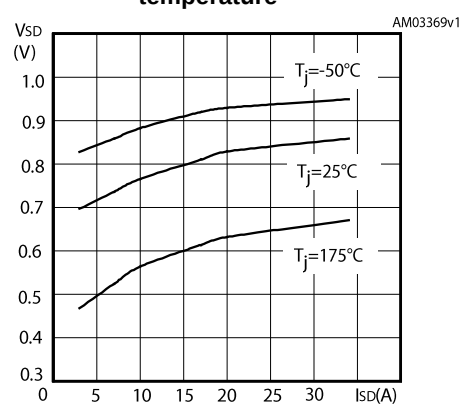
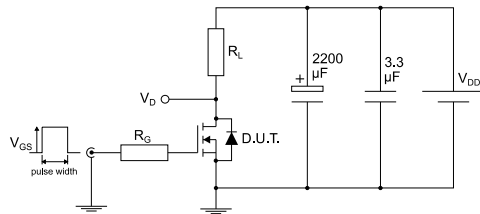
Figure 14: Avalanche energy vs starting T_j 

Figure 15: Source-drain diode forward vs temperature



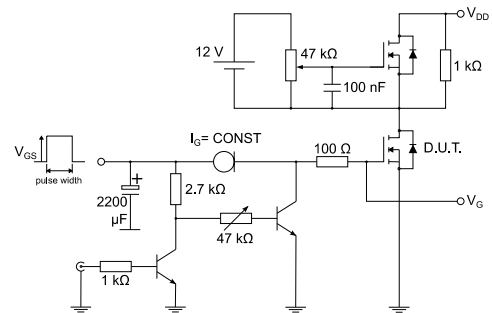
3 Test circuits

Figure 16: Test circuit for resistive load switching times



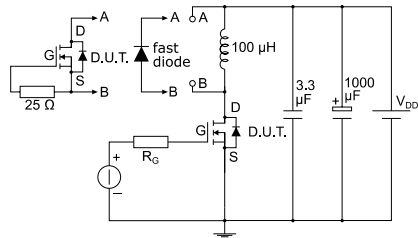
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Figure 17: Test circuit for gate charge behavior



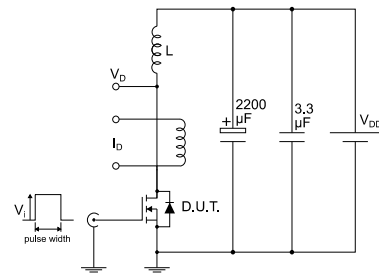
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Figure 18: Test circuit for inductive load switching and diode recovery times



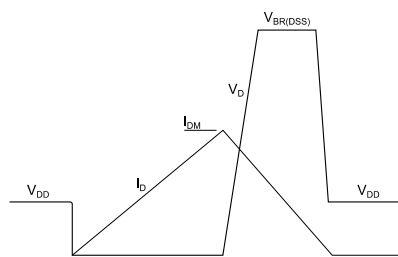
AM01470v1

Figure 19: Unclamped inductive load test circuit



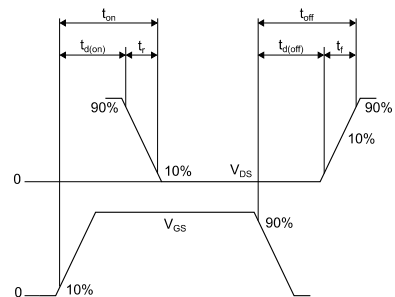
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Figure 20: Unclamped inductive waveform



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Figure 21: Switching time waveform



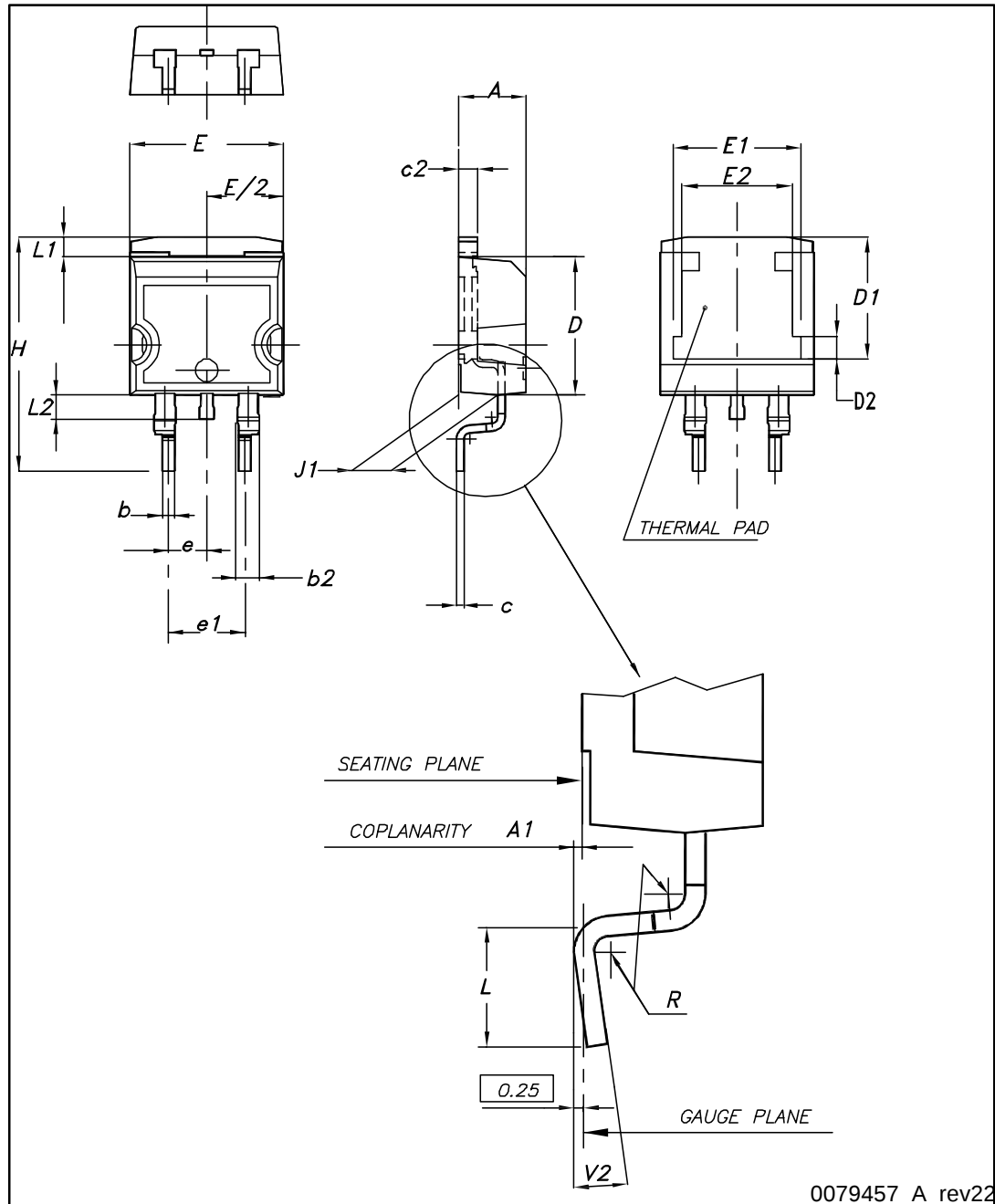
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 D²PAK (TO-263) package information

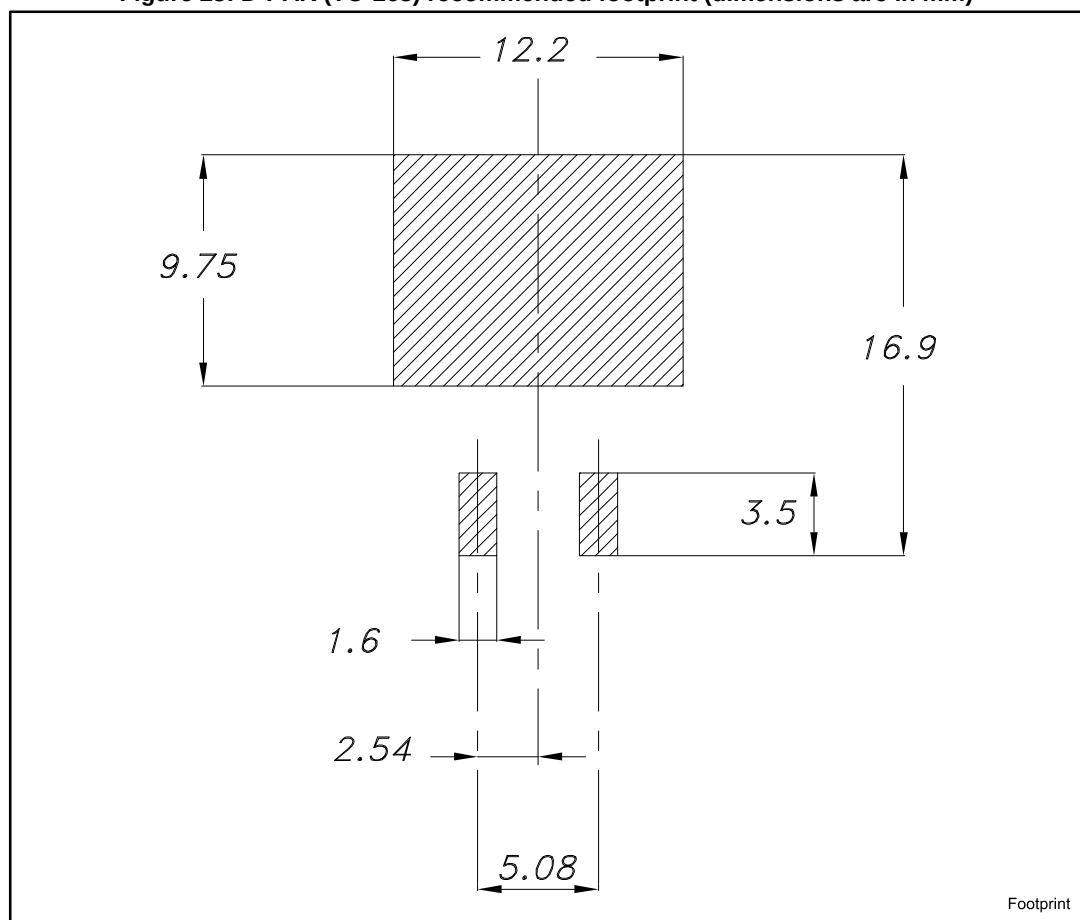
Figure 22: D²PAK (TO-263) type A package outline



0079457_A_rev22

Table 8: D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 23: D²PAK (TO-263) recommended footprint (dimensions are in mm)

4.2 D²PAK (TO-263) packing information

Figure 24: Tape outline

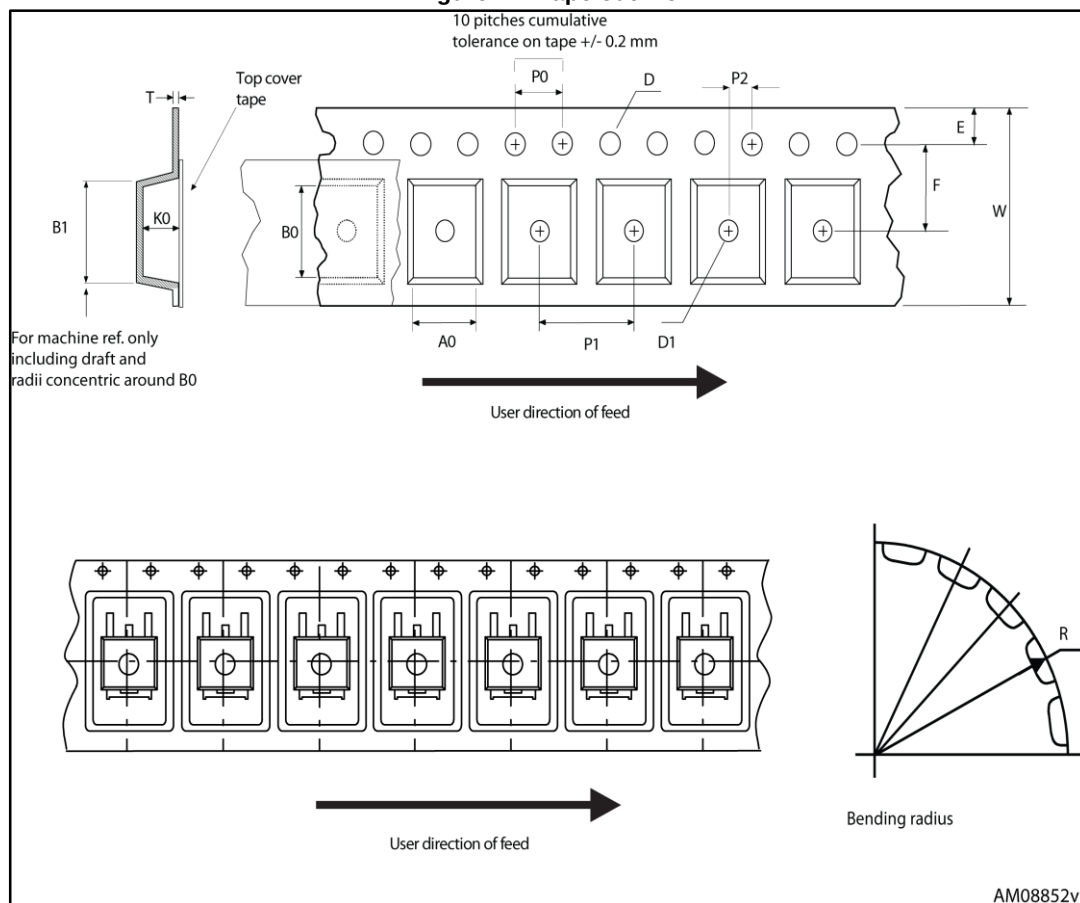
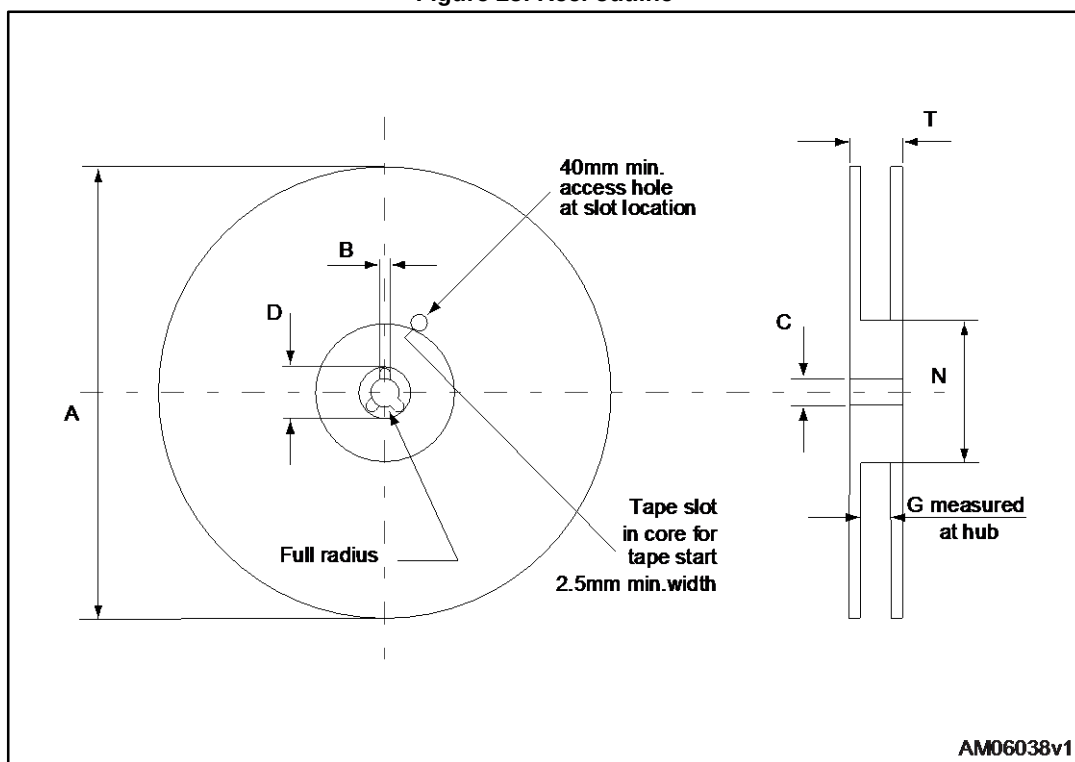


Figure 25: Reel outline

Table 9: D²PAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

4.3 TO-220 type A package information

Figure 26: TO-220 type A package outline

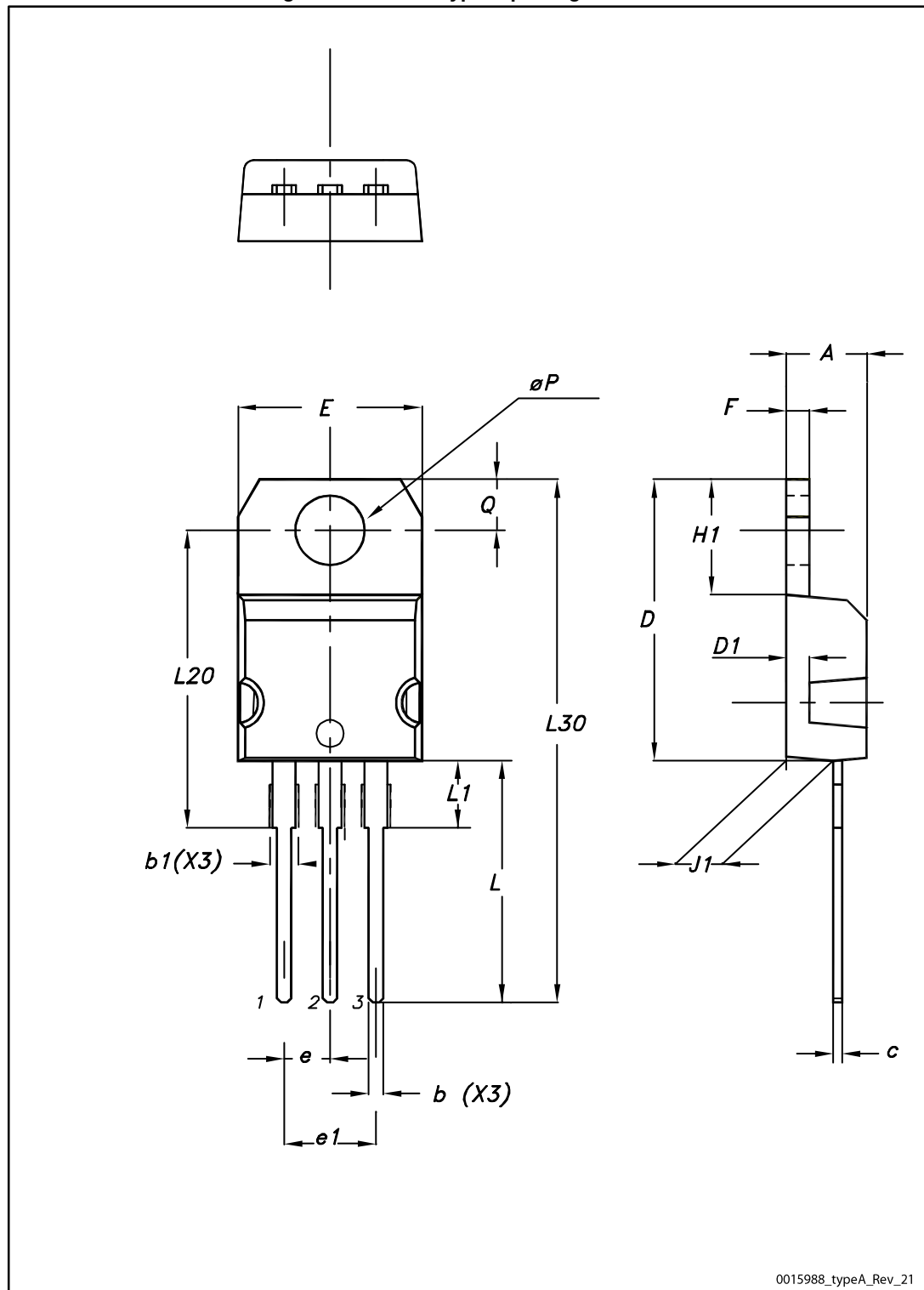


Table 10: TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

4.4 TO-247 package information

Figure 27: TO-247 package outline

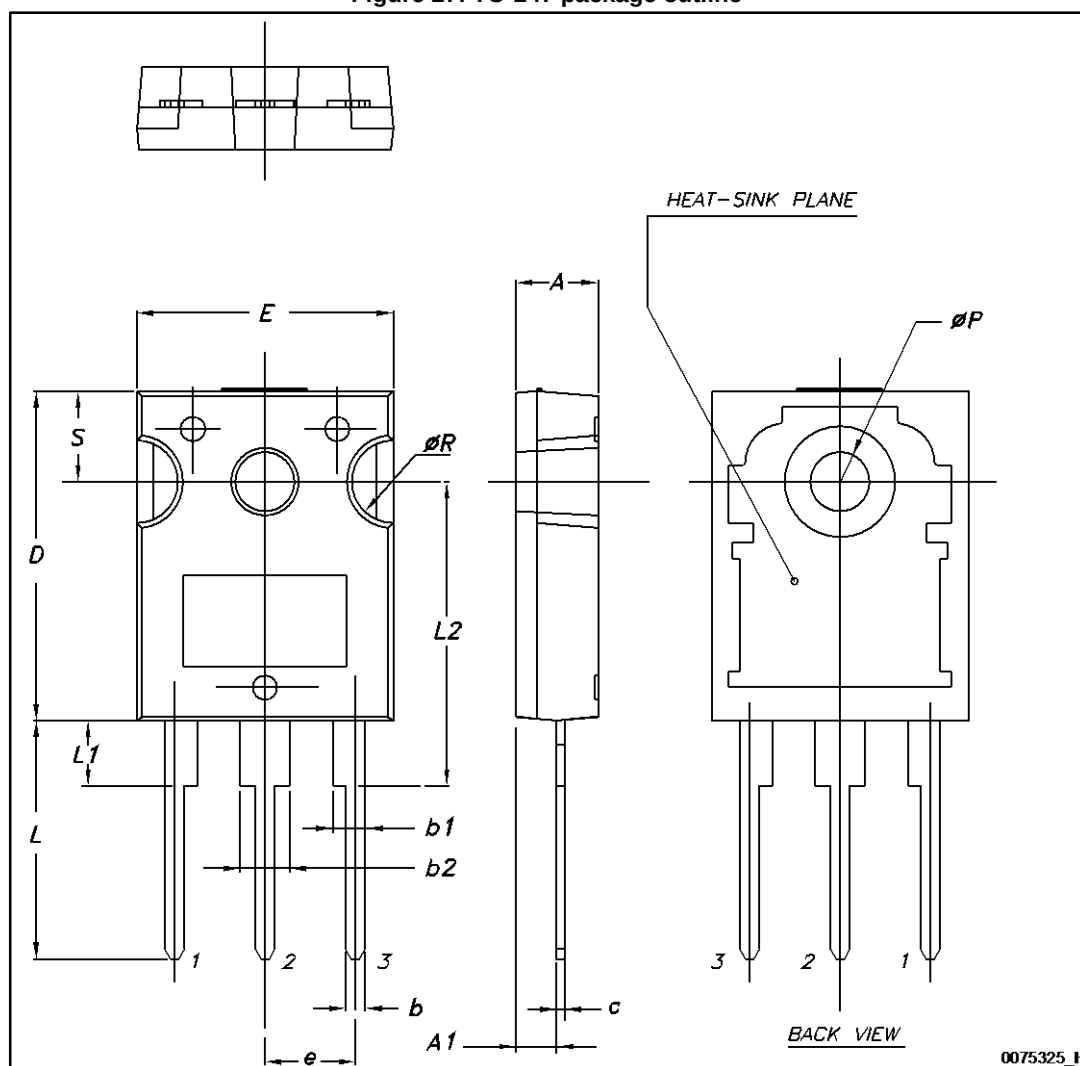


Table 11: TO-247 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

5 Revision history

Table 12: Document revision history

Date	Revision	Changes
28-Sep-2012	1	First release.
24-Aug-2016	2	Modified: Table 7: "Source-drain diode" Minor text changes

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