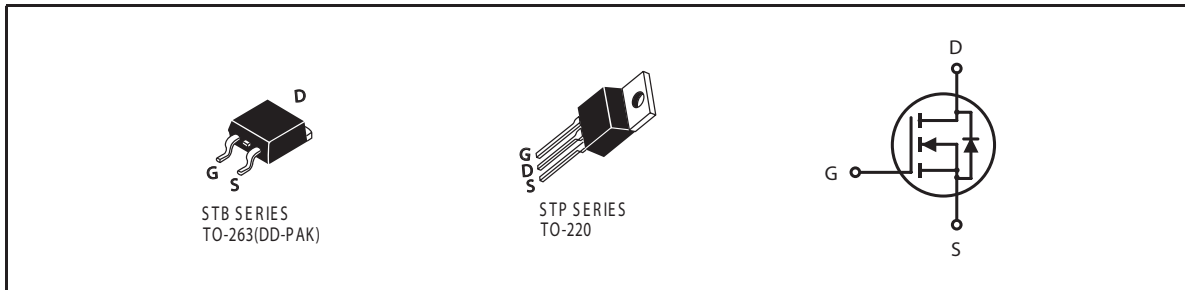


**N-Channel Logic Level Enhancement Mode Field Effect Transistor****PRODUCT SUMMARY**

V <sub>DSS</sub>	I <sub>D</sub>	R <sub>DS(ON)</sub> (mΩ) Typ
60V	70A	12 @ V <sub>GS</sub> =10V
		18 @ V <sub>GS</sub> =4.5V

**FEATURES**

- Super high dense cell design for extremely low R<sub>DS(ON)</sub>.
- High power and current handling capability.
- TO-220 & TO-263 package.

**ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Limit	Units
V <sub>DS</sub>	Drain-Source Voltage	60	V
V <sub>GS</sub>	Gate-Source Voltage	±20	V
I <sub>D</sub>	Drain Current-Continuous <sup>a</sup>	T <sub>C</sub> =25°C	70
		T <sub>C</sub> =70°C	58.6
I <sub>DM</sub>	-Pulsed <sup>b</sup>	206	A
E <sub>AS</sub>	Single Pulse Avalanche Energy <sup>d</sup>	272	mJ
P <sub>D</sub>	Maximum Power Dissipation <sup>a</sup>	T <sub>C</sub> =25°C	125
		T <sub>C</sub> =70°C	87.5
T <sub>J</sub> , T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to 175	°C

**THERMAL CHARACTERISTICS**

R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case <sup>a</sup>	1.2	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient <sup>a</sup>	62.5	°C/W

# STB/P70L60

Ver 1.1

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
B <sub>V</sub> DSS	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	60			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =48V, V <sub>GS</sub> =0V			1	uA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V			±100	nA
<b>ON CHARACTERISTICS</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	1	2	3	V
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =35A		12	16	m ohm
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =29A		18	25	m ohm
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =10V, I <sub>D</sub> =35A		38		S
<b>DYNAMIC CHARACTERISTICS °</b>						
C <sub>ISS</sub>	Input Capacitance	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V f=1.0MHz		2670		pF
C <sub>OSS</sub>	Output Capacitance			320		pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			210		pF
<b>SWITCHING CHARACTERISTICS °</b>						
t <sub>D(ON)</sub>	Turn-On Delay Time	V <sub>DD</sub> =30V I <sub>D</sub> =1A V <sub>GS</sub> =10V R <sub>GEN</sub> = 60 ohm		52		ns
t <sub>r</sub>	Rise Time			50		ns
t <sub>D(OFF)</sub>	Turn-Off Delay Time			105		ns
t <sub>f</sub>	Fall Time			16		ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =30V, I <sub>D</sub> =25A, V <sub>GS</sub> =10V		48		nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =30V, I <sub>D</sub> =25A,		6		nC
Q <sub>gd</sub>	Gate-Drain Charge	V <sub>GS</sub> =10V		13		nC
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
V <sub>SD</sub>	Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =15A		0.9	1.3	V
<b>Notes</b>						
a. Surface Mounted on FR4 Board, t ≤ 10sec. b. Pulse Test: Pulse Width ≤ 300us, Duty Cycle ≤ 2%. c. Guaranteed by design, not subject to production testing. d. Starting T <sub>J</sub> =25°C, L=0.5mH, V <sub>DD</sub> = 30V. (See Figure 13)						

Sep, 10, 2010

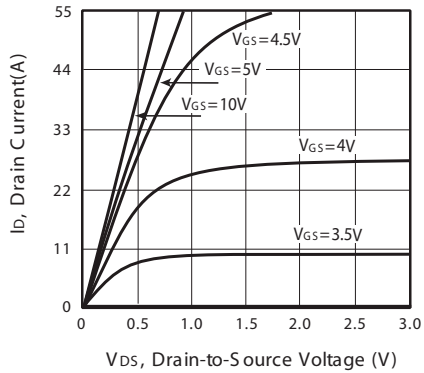


Figure 1. Output Characteristics

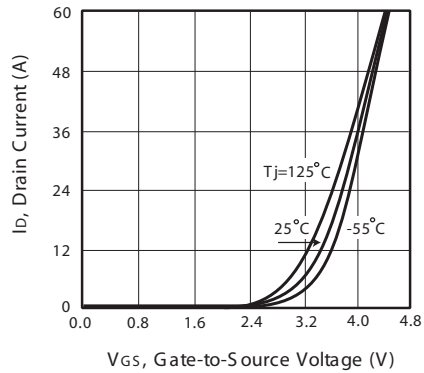


Figure 2. Transfer Characteristics

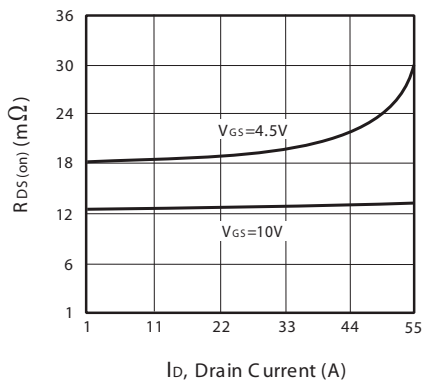


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

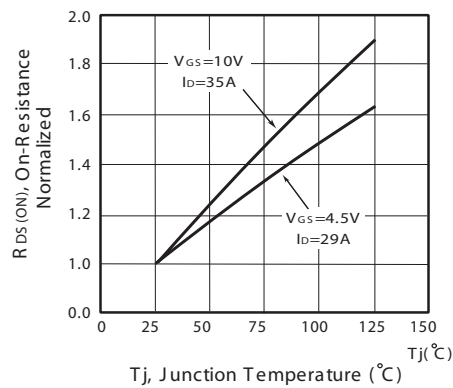


Figure 4. On-Resistance Variation with Drain Current and Temperature

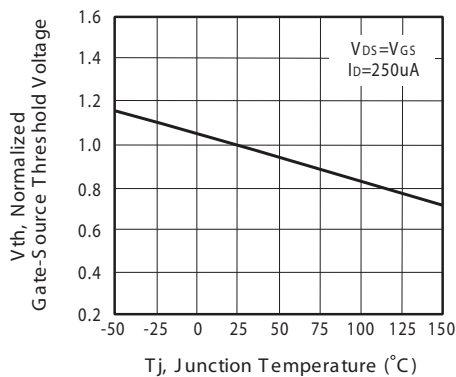


Figure 5. Gate Threshold Variation with Temperature

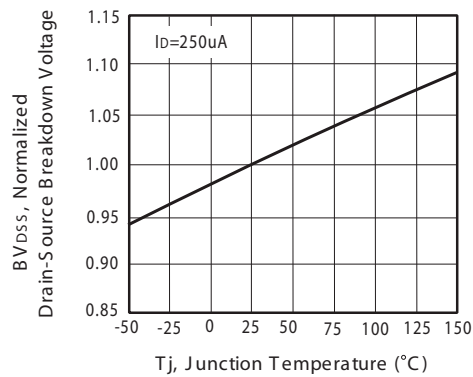


Figure 6. Breakdown Voltage Variation with Temperature

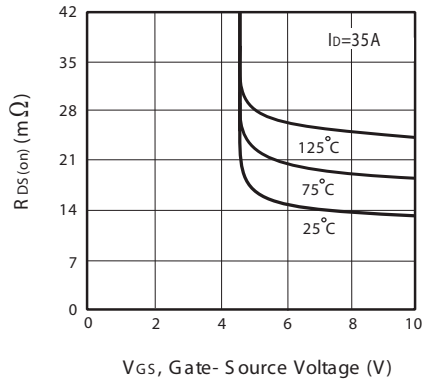


Figure 7. On-R-Resistance vs. Gate-Source Voltage

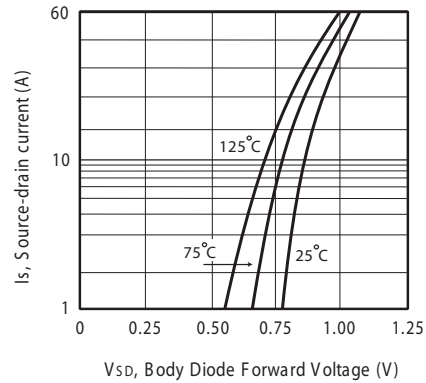


Figure 8. Body Diode Forward Voltage Variation with Source Current

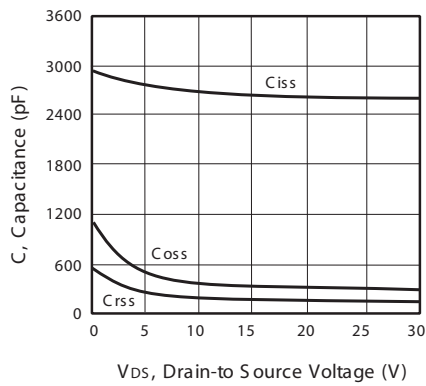


Figure 9. Capacitance

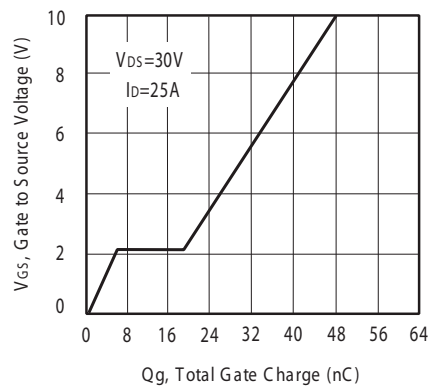


Figure 10. Gate Charge

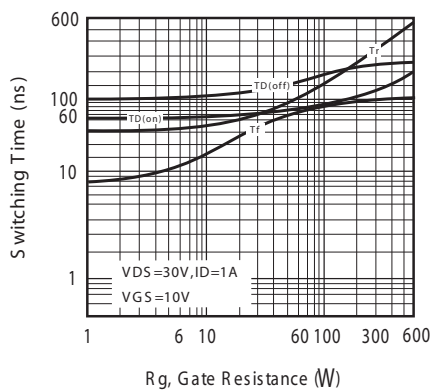


Figure 11. switching characteristics

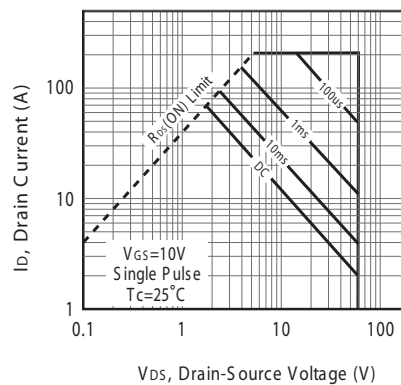
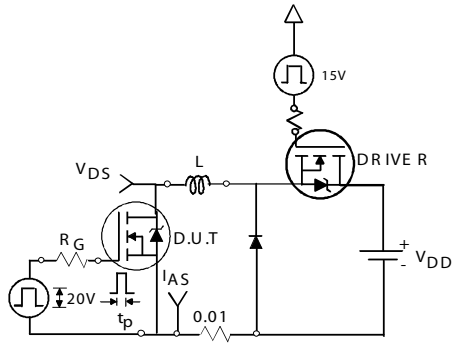
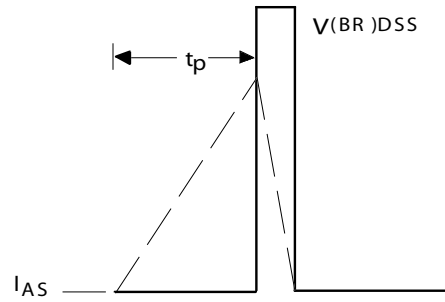


Figure 12. Maximum Safe Operating Area



Unclamped Inductive Test Circuit

Figure 13a.



Unclamped Inductive Waveforms

Figure 13b.

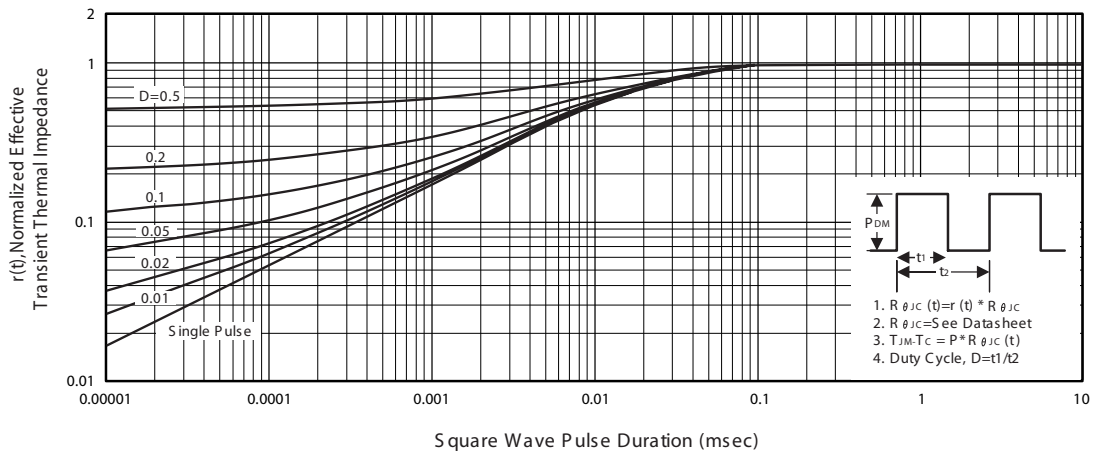


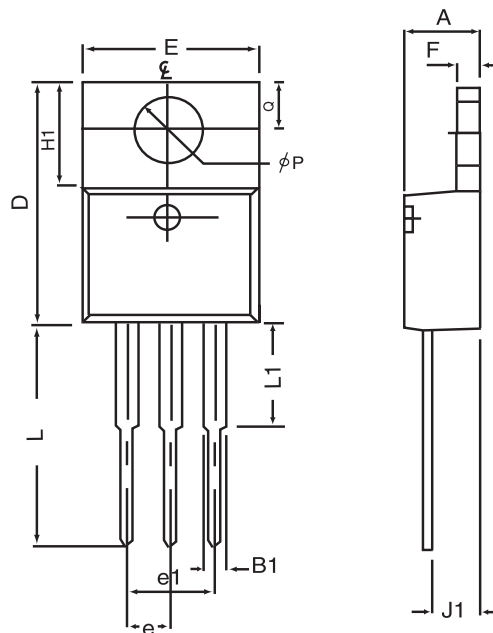
Figure 14. Normalized Thermal Transient Impedance Curve

# STB/P70L60

Ver 1.1

## PACKAGE OUTLINE DIMENSIONS

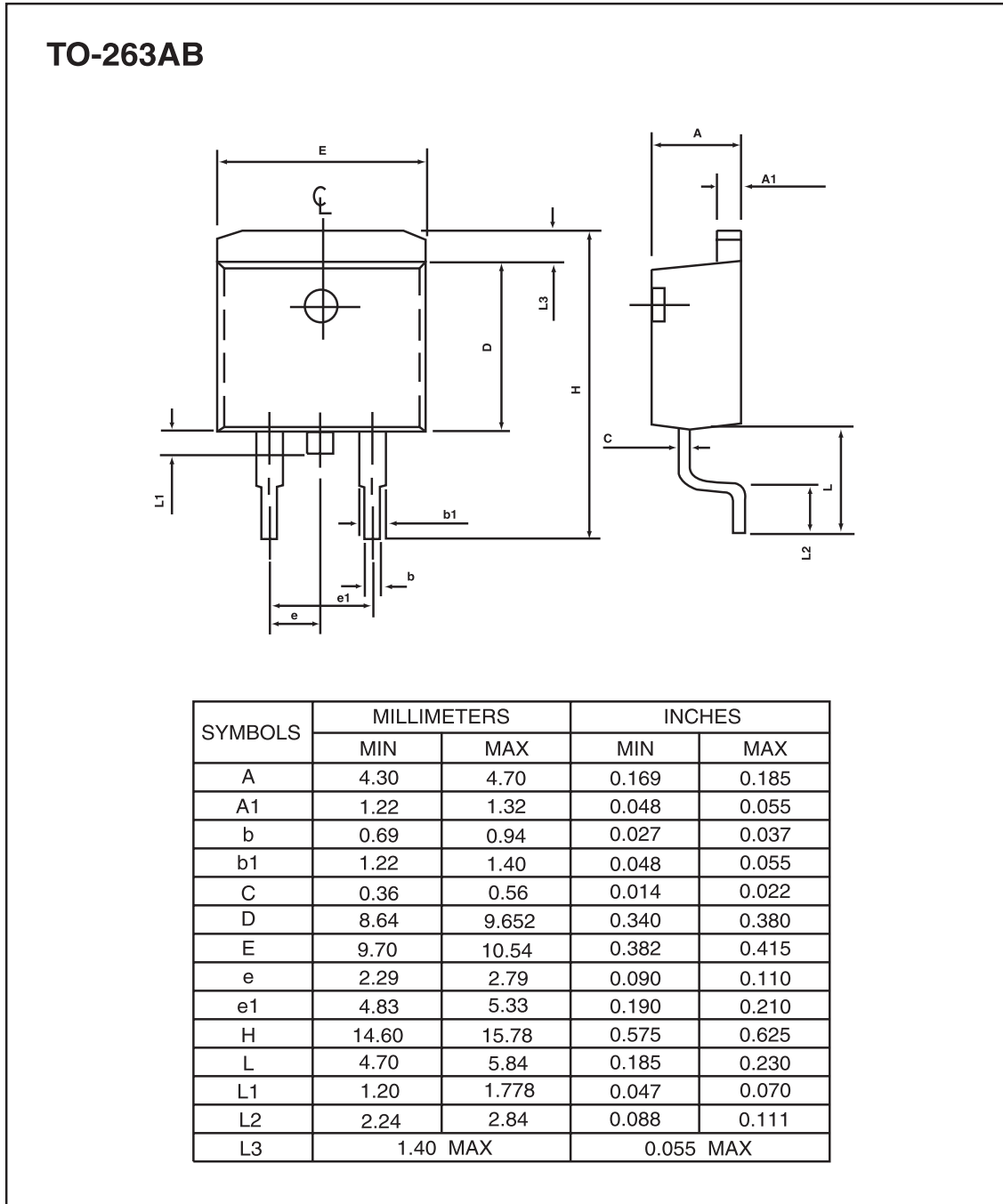
TO-220



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.32	4.80	0.170	0.189
B1	1.27	1.65	0.050	0.630
D	14.6	16.00	0.575	0.610
E	9.70	10.41	0.382	0.410
e	2.34	2.74	0.092	0.108
e1	4.68	5.48	0.184	0.216
F	1.14	1.40	0.045	0.055
H1	5.97	6.73	0.235	0.265
J1	2.20	2.79	0.087	0.110
L	12.88	14.22	0.507	0.560
L1	3.00	6.35	0.120	0.250
phi P	3.50	3.94	0.138	0.155
Q	2.54	3.05	0.100	0.120

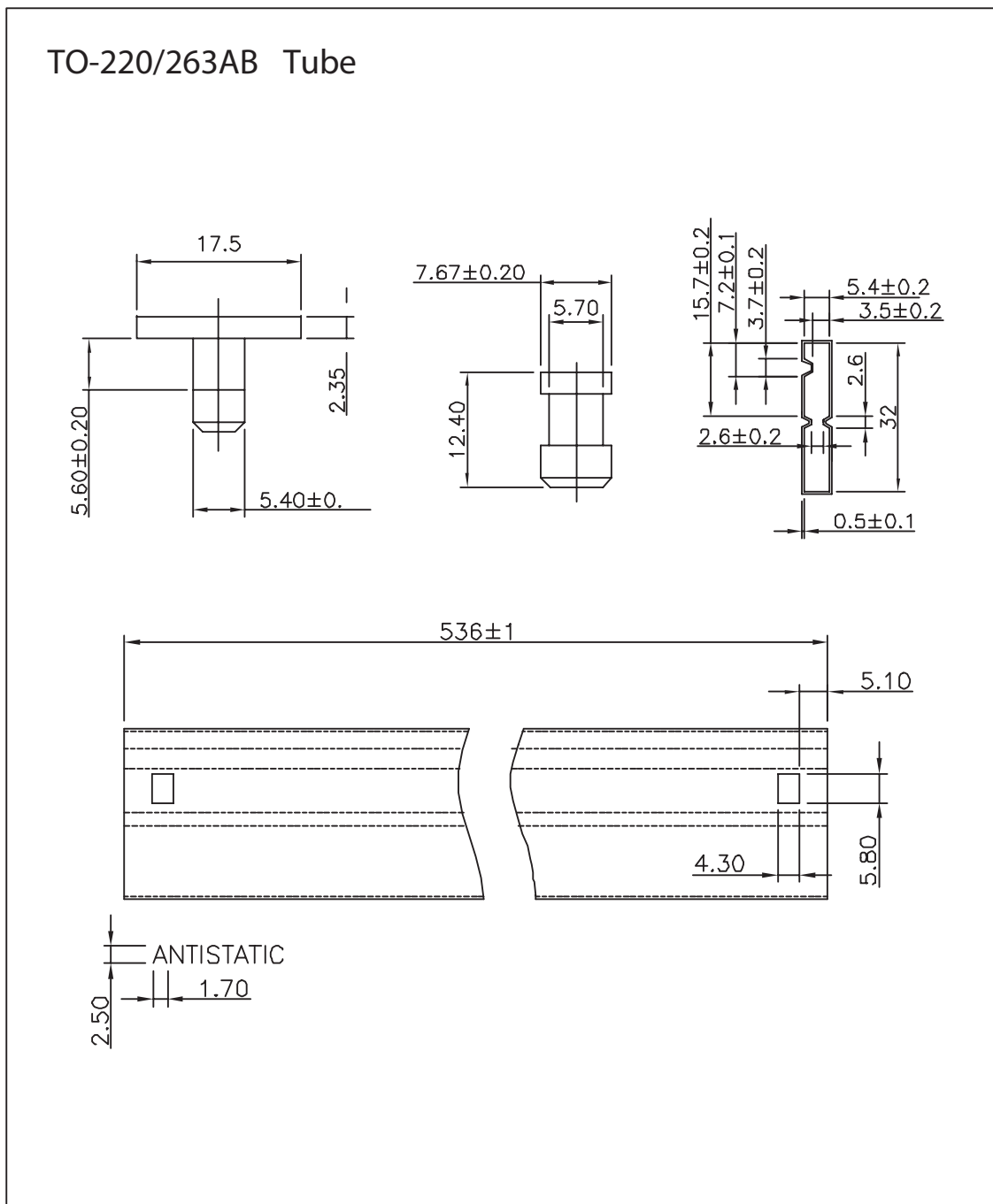
Sep,10,2010

## PACKAGE OUTLINE DIMENSIONS



# STB/P70L60

Ver 1.1



Sep,10,2010