



# STP75N15 STW75N15 - STB75N15

N-CHANNEL 150V - 0.02Ω - 75A TO-220/D<sup>2</sup>PAK/TO-247  
LOW GATE CHARGE STripFET™ MOSFET

TARGET SPECIFICATION

**Table 1: General Features**

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>	P <sub>w</sub>
STP75N15	150 V	< 0.023 Ω	75 A	300 W
STB75N15T4	150 V	< 0.023 Ω	75 A	300 W
STW75N15	150 V	< 0.023 Ω	75 A	350 W

- TYPICAL R<sub>DS(on)</sub> = 20 mΩ
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATIBILITY
- EXCELLENT FIGURE OF MERIT (R<sub>DS</sub>\*Q<sub>g</sub>)
- 100% AVALANCHE TESTED

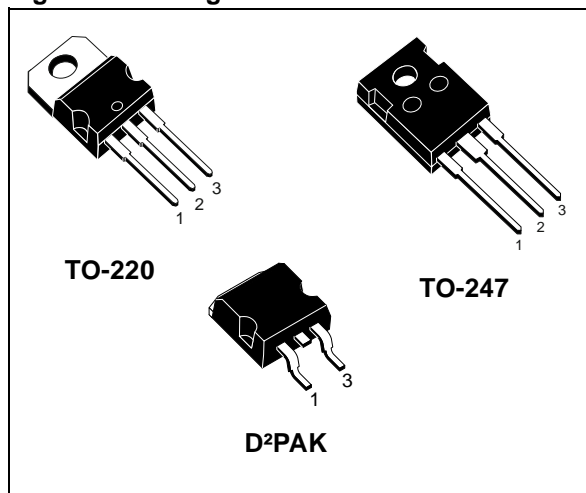
## DESCRIPTION

This MOSFET series realized with STMicroelectronics unique STripFET process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency isolated DC-DC converters.

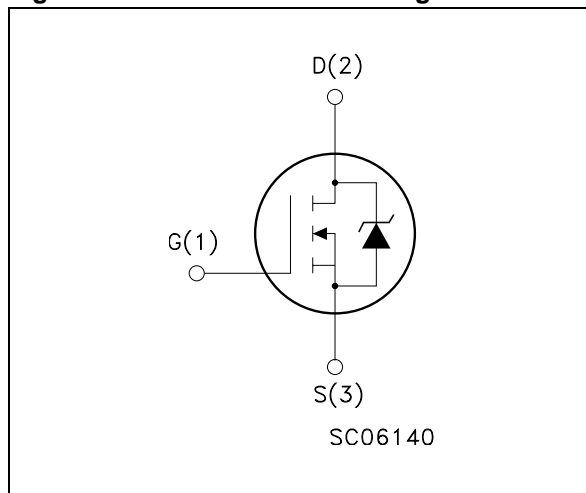
## APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- UPS

**Figure 1: Package**



**Figure 2: Internal Schematic Diagram**



**Table 2: Order Codes**

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP75N15	P75N15	TO-220	TUBE
STB75N15T4	B75N15	D <sup>2</sup> PAK	TAPE & REEL
STW75N15	W75N15	TO-247	TUBE

Rev. 1

**Table 3: Absolute Maximum ratings**

Symbol	Parameter	Value		Unit
		TO-220/D <sup>2</sup> PAK	TO-247	
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	150		V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	150		V
V <sub>GS</sub>	Gate- source Voltage	± 26		V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	75		A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	48		A
I <sub>DM</sub> (●)	Drain Current (pulsed)	300		A
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	300	350	W
	Derating Factor	2	2.38	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	TBD		V/ns
T <sub>j</sub> T <sub>stg</sub>	Operating Junction Temperature Storage Temperature	-55 to 150		°C

(●) Pulse width limited by safe operating area

(1) I<sub>SD</sub> ≤ 75A, di/dt ≤ 100A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>j</sub> ≤ T<sub>JMAX</sub>.

**Table 4: Thermal Data**

		TO-220/D <sup>2</sup> PAK	TO-247	Unit
R <sub>thj-case</sub>	Thermal Resistance Junction-case Max	0.5	0.42	°C/W
R <sub>thj-amb</sub>	Thermal Resistance Junction-ambient Max	62.5		°C/W
T <sub>l</sub>	Maximum Lead Temperature For Soldering Purpose	300		°C

**Table 5: Avalanche Characteristics**

Symbol	Parameter	Max Value	Unit
I <sub>AR</sub>	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T <sub>j</sub> max)	TBD	A
E <sub>AS</sub>	Single Pulse Avalanche Energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	TBD	mJ

**ELECTRICAL CHARACTERISTICS** ( $T_{CASE} = 25^{\circ}C$  UNLESS OTHERWISE SPECIFIED)**Table 6: On/Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0$	150			V
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}, T_C = 125^{\circ}C$			1 10	$\mu A$ $\mu A$
$I_{GSS}$	Gate-body Leakage Current ( $V_{DS} = 0$ )	$V_{GS} = \pm 26V$			$\pm 100$	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10V, I_D = 37.5 A$			0.023	$\Omega$

**Table 7: Dynamic**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (1)$	Forward Transconductance	$V_{DS} = 75 V, I_D = 37.5 A$		TBD		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25V, f = 1 \text{ MHz}, V_{GS} = 0$		4500 TBD TBD		pF pF pF
$t_{d(on)}$ $t_r$ $t_{d(off)}$ $t_f$	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	$V_{DD} = 75V, I_D = 37.5 A,$ $R_G = 4.7 \Omega, V_{GS} = 10 V$ ( see Figure 4)		TBD TBD TBD TBD		ns ns ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 126V, I_D = 75 A,$ $V_{GS} = 10V$ (Figure 7)		110 TBD TBD	TBD	nC nC nC

**Table 8: Source Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM} (2)$	Source-drain Current Source-drain Current (pulsed)				75 300	A A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 75 A, V_{GS} = 0$			1.5	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 37.5 A, di/dt = 100A/\mu s$ $V_{DD} = 75 V, T_j = 25^{\circ}C$ (see test circuit, Figure 5)		TBD TBD TBD		ns $\mu C$ A
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 37.5 A, di/dt = 100A/\mu s$ $V_{DD} = 75 V, T_j = 150^{\circ}C$ (see test circuit, Figure 5)		TBD TBD TBD		ns $\mu C$ A

(1) Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %.

(2) Pulse width limited by safe operating area.

Figure 3: Unclamped Inductive Load Test Circuit

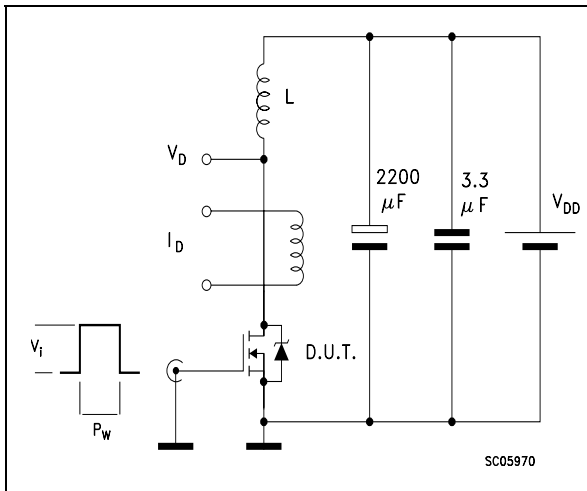


Figure 4: Switching Times Test Circuit For Resistive Load

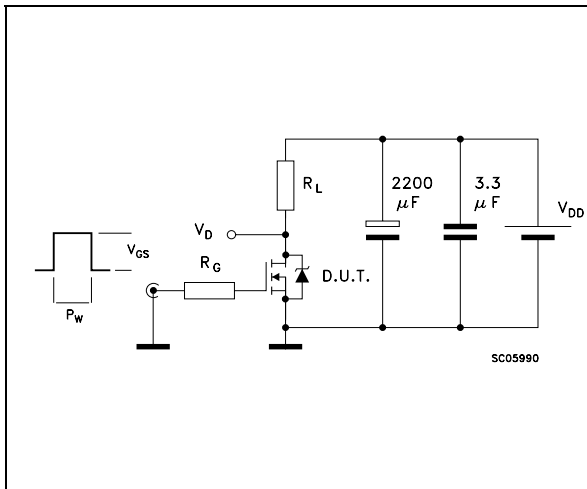


Figure 5: Test Circuit For Inductive Load Switching and Diode Recovery Times

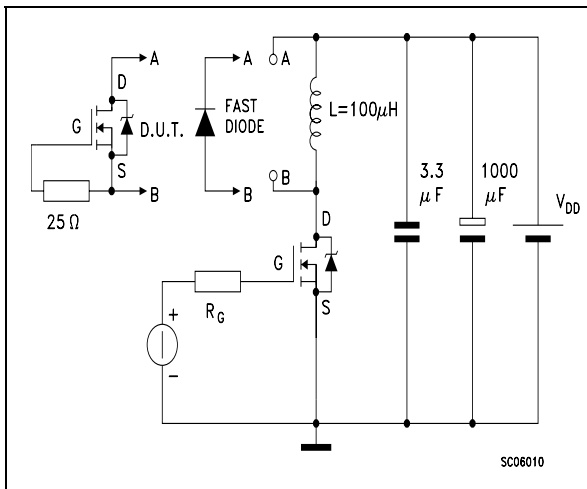


Figure 6: Unclamped Inductive Waferform

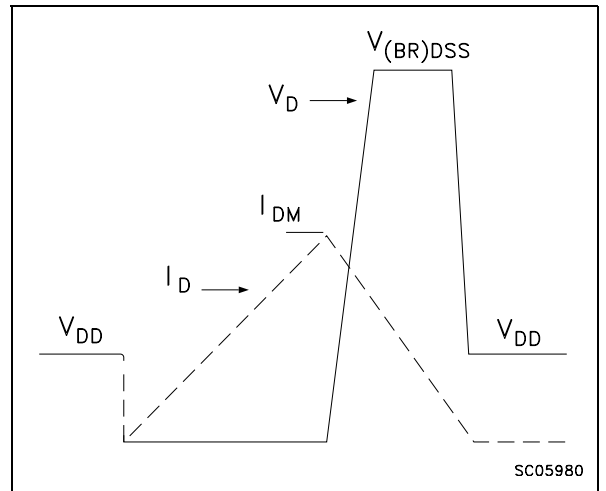
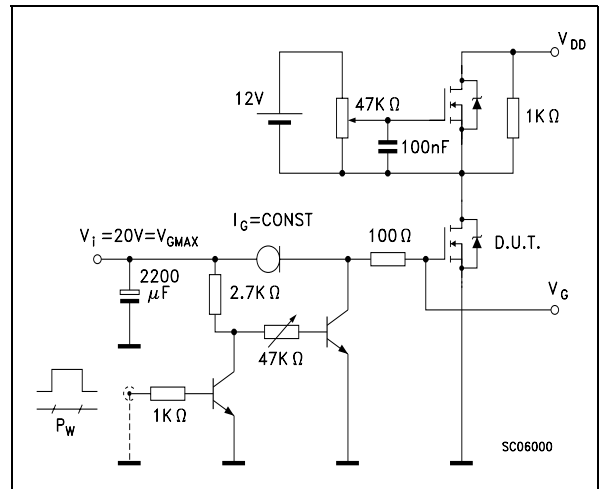
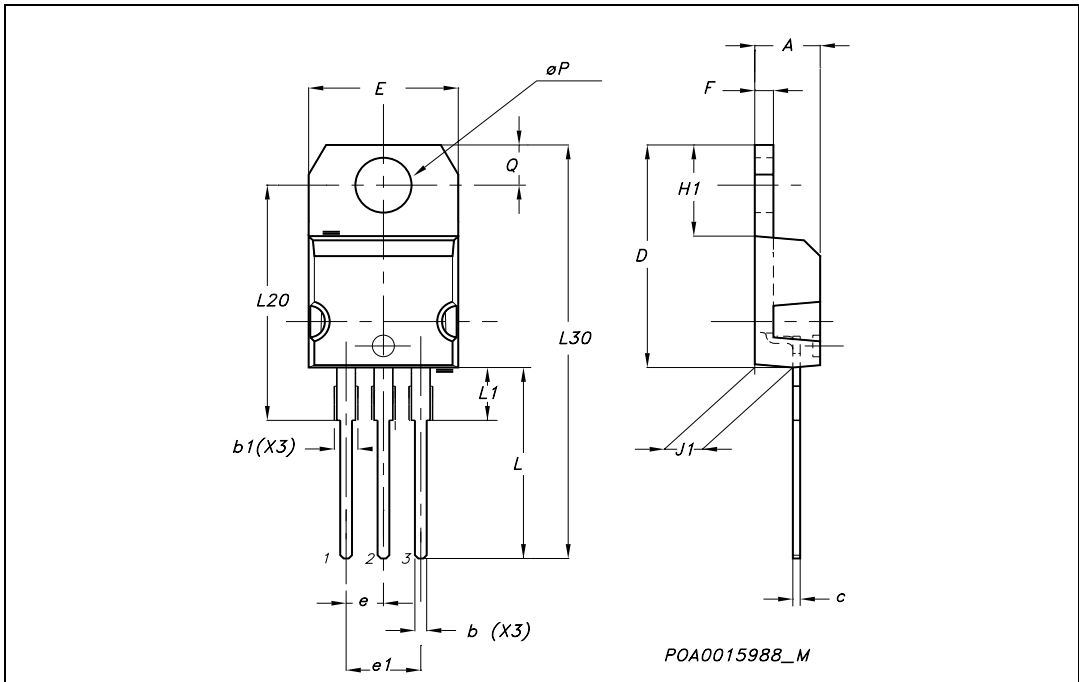


Figure 7: Gate Charge Test Circuit



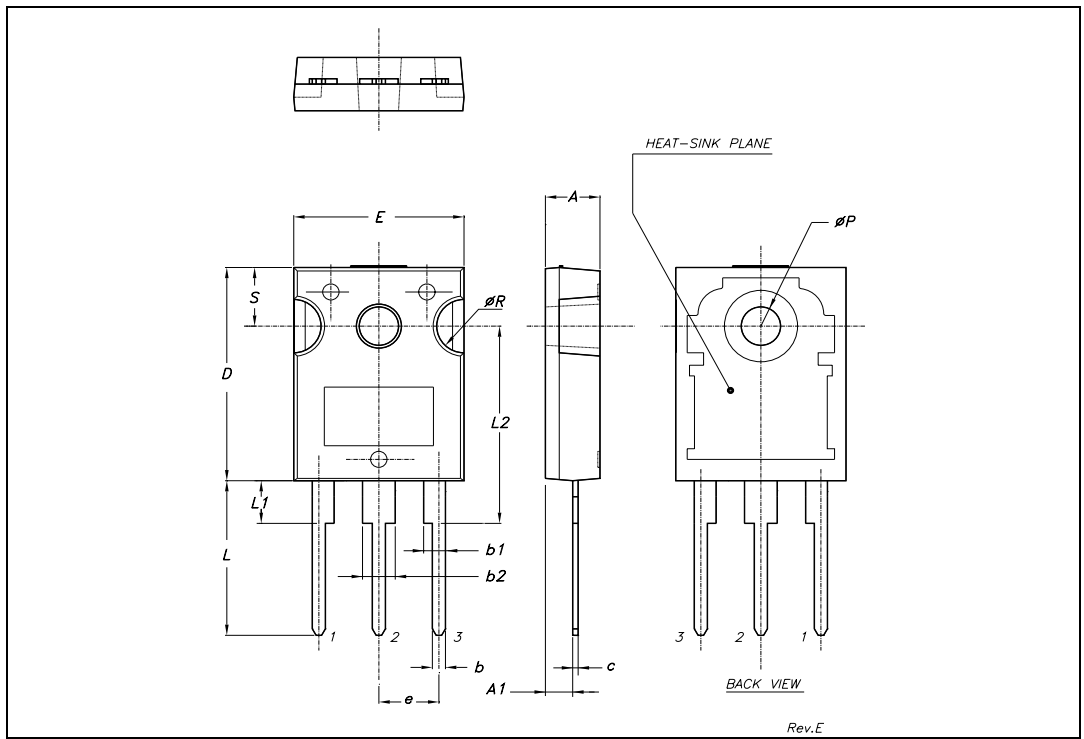
**TO-220 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



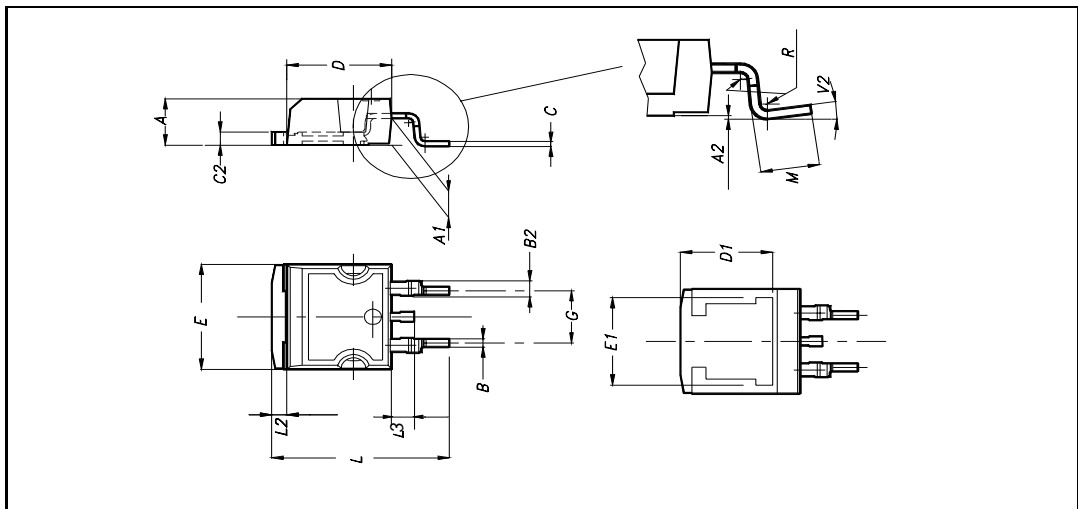
**TO-247 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	

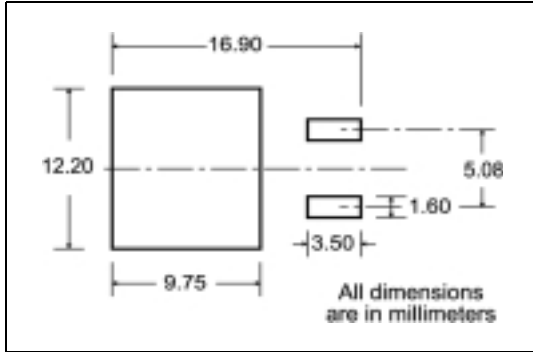


**D<sup>2</sup>PAK MECHANICAL DATA**

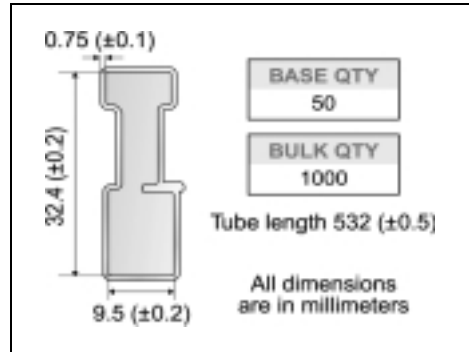
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			



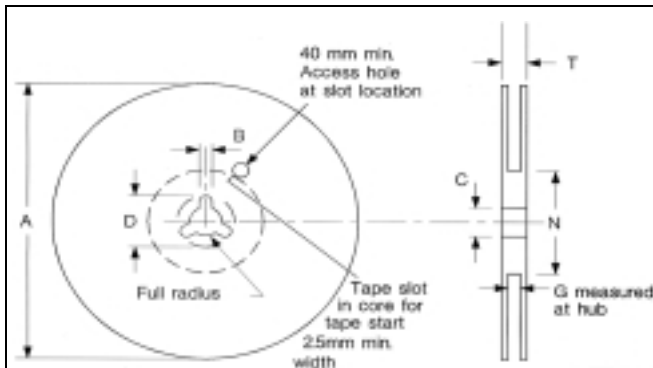
**D<sup>2</sup>PAK FOOTPRINT**



**TUBE SHIPMENT (no suffix)\***



**TAPE AND REEL SHIPMENT (suffix "T4")\***



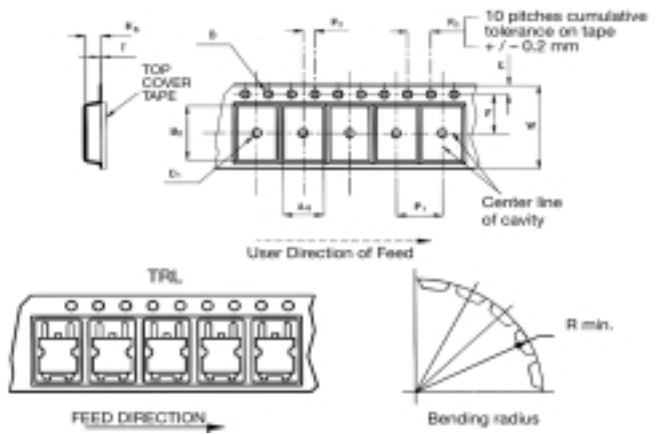
TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956

REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

BASE QTY	BULK QTY
1000	1000



\* on sales type



Table 9: Revision History

Date	Revision	Description of Changes
08-Nov-2004	1	First Release.

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