

STC5DNF30V

Dual N-channel 30V - 0.032Ω - 4.5A - TSSOP8 2.7V-Driver STripFET™ Power MOSFET

General features

Туре	V _{DSS}	R _{DS(on)}	I _D
STC5DNF30V	30V	< 0.035Ω (@4.5V) < 0.040Ω (@2.7V)	4.5A

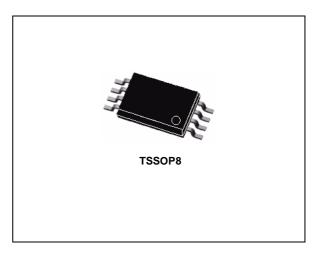
- Standard outline for easy automated surface mount assembly
- Ultra low threshold gate drive (2.7V)

Description

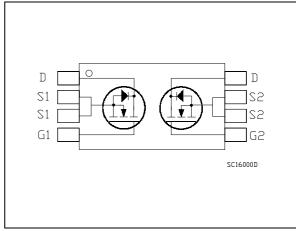
This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility. No electrical connections are shared between mosfets.

Applications

Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STC5DNF30V	C5DNF30V	TSSOP8	Tape & reel

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1 Electrical ratings

Table 1.	Absolute	maximum	ratings
	Absolute	maximum	ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage (V _{GS} = 0)	30	V
V _{GS}	Gate- source voltage	± 8	V
I _D ⁽¹⁾	Drain current (continuous) at T _C = 25°C	4.5	Α
I _D ⁽¹⁾	Drain current (continuous) at T _C = 100°C	2.8	А
I _{DM} ⁽²⁾	Drain current (pulsed)	18	Α
P _{TOT} ⁽¹⁾	Total dissipation at $t_c = 25^{\circ}C$	1.3	W

1. When mounted on FR-4 board with 1inch² pad, 2 Oz of Cu and t<10sec.

2. Pulse width limited by safe operating area

Table 2. Thermal data	Table	e 2.	Thermal	data
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Symbol	Parameter	Value	Unit
	Thermal resistance junction-pcb max	120	°C/W
Rthj-pcb ⁽²⁾	Thermal resistance junction-pcb max	97.5	°C/W
Т _ј	Operating junction temperature	-55 to 150	°C
T _{stg}	Storage temperature	-55 to 150	°C

1. When mounted on minimum recommended footprint.

2. When mounted on FR-4 board with 1inch² pad, 2 Oz of Cu and t<10sec.

2 Electrical characteristics

(T_J =25°C unless otherwise specified)

Table 5.						
Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 250µA, V _{GS} = 0	30			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = Max rating V _{DS} = Max rating,T _C =125°C			1 10	μΑ μΑ
I _{GSS}	Gate-body leakage current (V _{DS} = 0)	$V_{GS} = \pm 8V$			±100	nA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	0.6			V
R _{DS(on)}	Static drain-source on resistance	$V_{GS} = 4.5V, I_D = 2.3A$ $V_{GS} = 2.7V, I_D = 2.3A$		0.032 0.036	0.035 0.040	Ω Ω

Table 3. On/off

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
9 _{fs}	Forward transconductance	V _{DS} =25V _; I _D = 2.3A		9.5		S
C _{iss} C _{oss} C _{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V _{DS} = 25V, f = 1 MHz, V _{GS} = 0		460 200 50		pF pF pF
Q _g Q _{gs} Q _{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 16V, I_D = 4.5A,$ $V_{GS} = 4.5V$ (see Figure 14)		8.5 1.8 2.4	11.5	ns ns ns

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)} t _r t _{d(off)} t _r	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD} = 10V, I_D = 2.3A,$ $R_G = 4.7\Omega V_{GS} = 4.5V$ (see Figure 13)		7 33 27 10		ns ns ns ns
t _{r(Voff)} t _f t _c	Off-voltage rise time Fall time Cross-over time	$V_{DD} = 16V, I_D = 2.3A, R_G = 4.7\Omega, V_{GS} = 4.5V$ (see Figure 17)		26 11 21		ns ns ns

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD} I _{SDM} ⁽¹⁾	Source-drain current Source-drain current (pulsed)				4.5 18	A A
V _{SD} ⁽²⁾	Forward on voltage	$I_{SD} = 4.5A, V_{GS} = 0$			1.2	V
t _{rr} Q _{rr} I _{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 4.5A$, di/dt =100A/µs, $V_{DD} = 10V$, $T_j = 150^{\circ}C$ (see Figure 15)		26 13 1		ns nC A

Table 6.Source drain diode

1. Pulse width limited by safe operating area.

2. Pulsed: Pulse duration = $300 \ \mu$ s, duty cycle 1.5 %.



2.1 Electrical characteristics (curves)

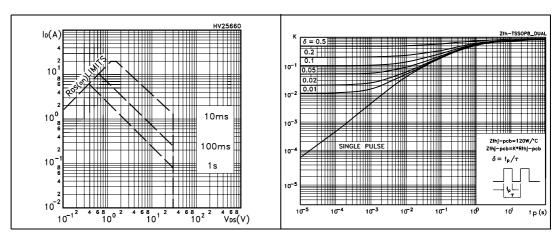
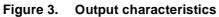
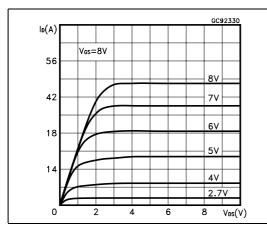


Figure 1. Safe operating area

Figure 2. Thermal impedance







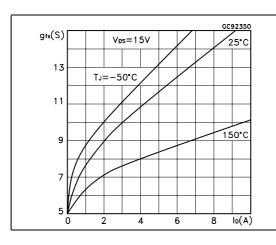


Figure 4. Transfer characteristics

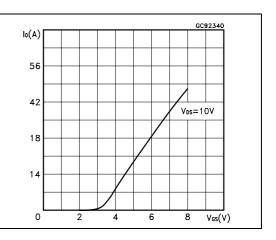
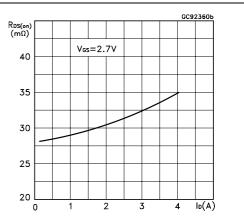


Figure 6. Static drain-source on resistance





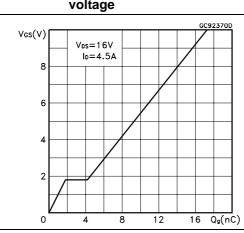


Figure 7. Gate charge vs gate-source Figure 8. Capacitance variations voltage

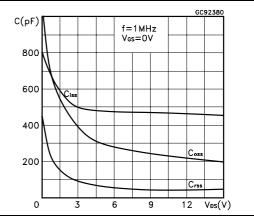


Figure 9. Normalized gate thereshold voltage vs temperature

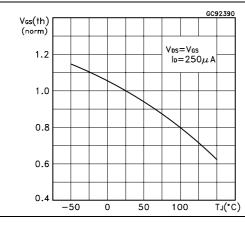


Figure 10. Normalized on resistance vs temperature

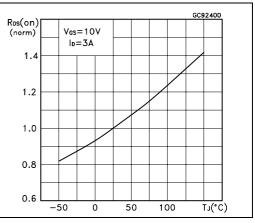
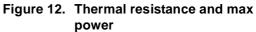
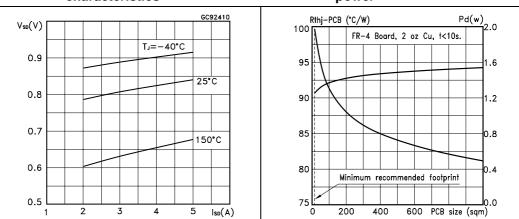


Figure 11. Source-drain diode forward characteristics



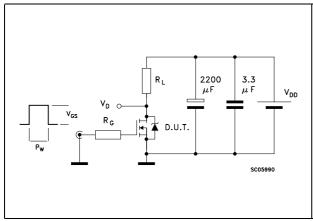




1KΩ

3 Test circuits

Figure 13. Switching times test circuit for resistive load



 $V_{1} = 20V = V_{OMAX}$ $I_{0} = CONST$ 100Ω $I_{0} = D.U.T.$ V_{0} $\frac{2200}{2.7K \Omega}$ $47K \Omega$ $K \Omega$ Scoecooc

47K Ω

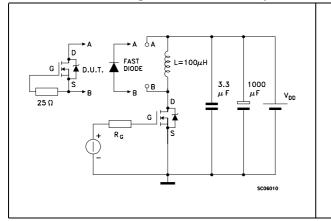
‡100nF

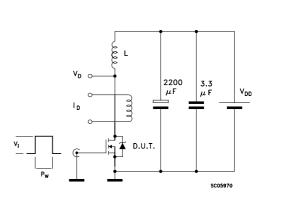
Figure 14. Gate charge test circuit

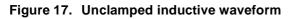
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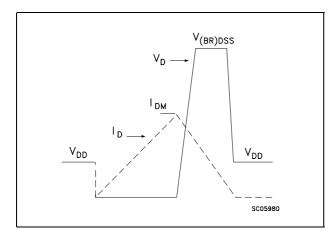
Figure 15. Test circuit for inductive load switching and diode recovery times

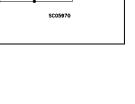












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4 Package mechanical data

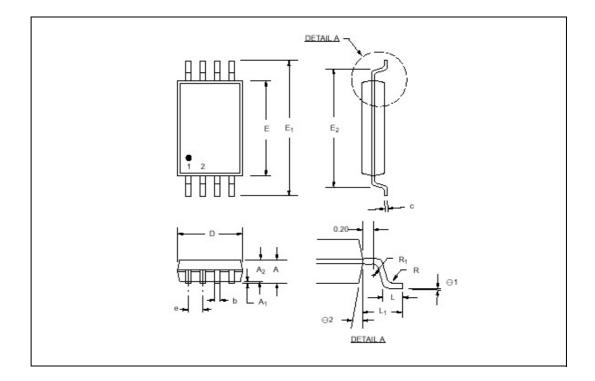
In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com



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DIM.	mm.			inch			
DIM.	MIN.	TYP	MAX.	MIN.	TYP.	MAX.	
А	1.05		1.20	0.041		0.047	
A1	0.05		0.15	0.002		0.006	
A2	0.80		1.05	0.032		0.041	
b	0.19		0.30	0.008		0.012	
С		0.127			0.005		
D	2.90		3.10	0.114		0.122	
E	4.30		4.50	0.170		0.177	
E1	6.20		6.60	0.240		0.260	
E2	5.14		5.24	0.202		0.206	
е		0.65			0.025		
L	0.45		0.75	0.018		0.030	
L1	0.90		1.10	0.0355		0.0433	
R	0.09			0.004			
R1	0.09			0.004			
θ1	0°		8°	0°		8°	





5 Revision history

Table 7.

Date	Revision	Changes
11-Apr-2006	1	First release



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