

# STC9492C Series

## CMOS 1,200bps PSK SINGLE CHIP MODEM

- Compatible with Bell212A (High speed)/CCITT V.22
- Tone Generator Incorporated
- Call Progress Tone Detection Function Provided

### DESCRIPTION

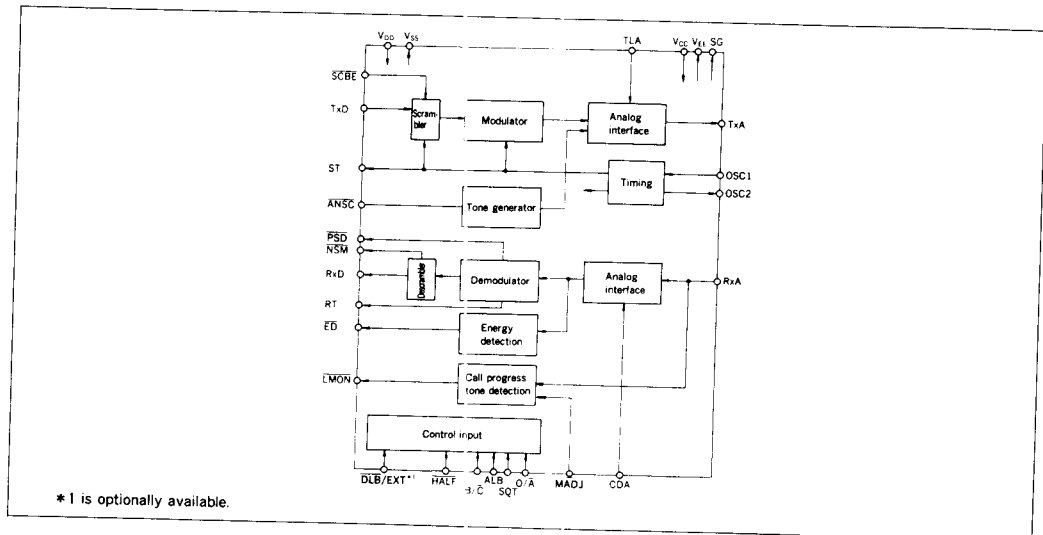
The STC9492C Series is a Bell 212A (high speed)/CCITT V.22 compatible, single chip, 1,200 bps CMOS LSI for a PSK MODEM. The built-in additional functions include answer and guard tones generation functions and a call progress tone detection function.

The high quality switched capacitor circuits and the adaptive equalizing algorithm are adopted in the signal processing, so that they realize highly reliable data quality.

### FEATURES

- Compatible with Bell 212A (high speed), CCITT V.22
- Built-in Tone Generator (2,225Hz/2,100Hz/1,800Hz)
- Call Progress Tone Detector On Chip
- Adaptive Equalizer On Chip
- 4.032MHz Crystal Oscillation ..... Quartz oscillator and capacitors externally connected
- Test Function ..... Analog Loop-back Test  
Digital Remote Loop-back Test
- Low Power Consumption ..... Operation : 120mW (Typ)  
Power down : 10 $\mu$ W (Max)
- Input/Output Interface ..... CMOS level
- Single Power Supply ..... 5V  $\pm$  10%
- Package ..... 28-pin DIP (plastic)/28-pin SOP (plastic)

### BLOCK DIAGRAM



## ■ PIN CONFIGURATION (This also applies to DIP and SOP.)

|                 |    |    |                 |
|-----------------|----|----|-----------------|
| ST              | 1  | 28 | OSC2            |
| LMON            | 2  | 27 | OSC1            |
| PSD             | 3  | 26 | NSM             |
| V <sub>SS</sub> | 4  | 25 | RxD             |
| ED              | 5  | 24 | RT              |
| TxD             | 6  | 23 | O/A             |
| SCBE            | 7  | 22 | ALB             |
| DLB/EXT *1      | 8  | 21 | SQT             |
| HALF            | 9  | 20 | ANSC            |
| B/C             | 10 | 19 | V <sub>DD</sub> |
| MADJ            | 11 | 18 | V <sub>CC</sub> |
| V <sub>EE</sub> | 12 | 17 | SG              |
| CDA             | 13 | 16 | TxA             |
| RxA             | 14 | 15 | TxA             |

\*1 Optionally available.

## ■ PIN DESCRIPTION

| Pin Name        | Pin No. | I/O   | Functions                                                                                                                                                                                                       |
|-----------------|---------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| ST              | 1       | O     | [Transmit timing output]<br>Outputs a transmit timing signal synchronized with the internal operation.                                                                                                          |
| LMON            | 2       | O     | [Call progress tone detection output]<br>Detects call progress tones generated during line connection, and outputs their energy envelope.                                                                       |
| PSD             | 3       | O     | [PSK signal detection output]<br>When detects the PSK carrier in a receive signal, this produces low level.                                                                                                     |
| V <sub>SS</sub> | 4       | —     | [V <sub>SS</sub> supply for the digital section] 0V                                                                                                                                                             |
| ED              | 5       | O     | [Carrier detection output]<br>When detects the appointed energy within receive band, this produces low level.                                                                                                   |
| TxD             | 6       | I * 1 | [Transmit data input]<br>Inputs transmit data for PSK modulation.<br>Mark : High level    Space : Low level                                                                                                     |
| SCBE            | 7       | I *   | [Scrambler control input]<br>The low level input enables the scrambler active.<br>This should be high level for transmitting non-scrambled data.                                                                |
| DLB             | 8 * 2   | I *   | [Digital remote loop-back test input]<br>The low level input sets a remote digital loop.<br>RxD produces mark continuously during this test mode.                                                               |
| EXT             |         | I *   | [External transmit timing input]<br>The external transmit timing can be input to this terminal.<br>Tolerance : within $\pm 0.01\%$ of data transmit speed                                                       |
| HALF            | 9       | I *   | [1,200bps/600bps selection input]<br>Selects the transmit speed.<br>1,200bps : High level    600bps : Low level                                                                                                 |
| B/C             | 10      | I *   | [Bell/CCITT mode selection input]<br>Controls answer tone or guard tone connected with Bell/CCITT mode.<br>Bell : High level    CCITT : Low level                                                               |
| MADJ            | 11      | I     | [Call progress tone detection level adjust]<br>The call progress tone detection level can be adjusted by supplied voltage.<br>When unused, this should be connected to SG, V <sub>CC</sub> or V <sub>EE</sub> . |
| V <sub>EE</sub> | 12      | —     | [V <sub>EE</sub> supply for the analog section] 0V                                                                                                                                                              |

\*1 I\* has a built-in pull-up resistor.

\*2 Optional selection

| Pin Name        | Pin No. | I/O   | Functions                                                                                                                                                                                                                             |
|-----------------|---------|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CDA             | 13      | I/O   | [Carrier detection level adjust]<br>Can adjust a carrier detection level by potential difference with SG.<br>(when opened, produces $\approx V_{SG} + 1.0V$ )                                                                         |
| RxA             | 14      | I     | [Receive analog input]<br>Inputs the receive analog signal.                                                                                                                                                                           |
| TxA             | 15      | O     | [Transmit analog output]<br>Outputs the transmit analog signal.                                                                                                                                                                       |
| TLA             | 16      | I/O   | [Transmit level adjust]<br>Can adjust a transmit signal output level by potential difference with SG.<br>(When opened, produces $\approx V_{SG} + 1.0V$ )                                                                             |
| SG              | 17      | O     | [Signal ground]<br>Outputs a reference potential of an analog signal.<br>(When opened, produces $\approx 2.5V$ )                                                                                                                      |
| V <sub>CC</sub> | 18      | —     | [V <sub>CC</sub> supply for the analog section] +5V                                                                                                                                                                                   |
| V <sub>DD</sub> | 19      | —     | [V <sub>DD</sub> supply for the digital section] +5V                                                                                                                                                                                  |
| ANSC            | 20      | I* *1 | [Answer tone control input]<br>The low level input enables answer tone generation during SQT is high level.                                                                                                                           |
| SQT             | 21      | I*    | [Squelch transmitter]<br>The high level input squelches the carrier transmitting.                                                                                                                                                     |
| ALB             | 22      | I*    | [Analog loop-back test input]<br>The high level input leads to connection of modulated output to demodulated input, so that enables the analog loop-back test.<br>Both ALB and SQT are made high, the power-down mode is established. |
| O/ $\bar{A}$    | 23      | I*    | [Originate or Answer mode selection input]<br>Originate mode : High level    Answer mode : Low level                                                                                                                                  |
| RT              | 24      | O     | [Receive timing output]<br>Outputs a receive timing signal.                                                                                                                                                                           |
| RxD             | 25      | O     | [Receive data output]<br>Outputs the PSK demodulated serial data. This produces high level continuously when $\overline{PSD}$ is high level or $\overline{DLB}$ is low level.<br>Mark : High level    Space : Low level               |
| NSM             | 26      | O     | [Non-scrambled mark detection output]<br>Outputs low level when 64 or more continuous mark signals are detected in the input of the descrambler.                                                                                      |
| OSC1            | 27      | I     | [Oscillation input/output]<br>Connects a 4.032MHz crystal oscillator and capacitors.                                                                                                                                                  |
| OSC2            | 28      | O     |                                                                                                                                                                                                                                       |

\*1 I\* has a built-in pull-up resistor.

#### ■STC9492C SERIES

| Name                   | Optional Selection (#8 pin) | Package    |
|------------------------|-----------------------------|------------|
| STC9492C <sub>ID</sub> | $\overline{DLB}$            | 28-pin DIP |
| STC9492M <sub>ID</sub> |                             | 28-pin SOP |
| STC9492C <sub>IE</sub> | EXT                         | 28-pin DIP |
| STC9492M <sub>IE</sub> |                             | 28-pin SOP |

## ■ABSOLUTE MAXIMUM RATINGS

| Parameter                      |               | Symbol        | Ratings                          | Unit |
|--------------------------------|---------------|---------------|----------------------------------|------|
| Supply voltage                 |               | $V_{CC}$      | 7                                | V    |
|                                |               | $V_{DD}$      | 7                                | V    |
| Input voltage                  | Analog input  | $V_{IA}^{*1}$ | $V_{EE} - 0.3$ to $V_{CC} + 0.3$ | V    |
|                                | Digital input | $V_{ID}^{*2}$ | $V_{SS} - 0.3$ to $V_{DD} + 0.3$ | V    |
| Power dissipation              |               | $P_D$         | 500                              | mW   |
| Storage temperature            |               | $T_{stg}$     | -65 to 150                       | °C   |
| Soldering temperature and time |               | $T_{sol}$     | 260°C, 10s (at lead)             | —    |

\*1.....TLA, CDA, RxA, MADJ

\*2.....OSC1, TxD, SQT, ALB, O/A, ANSC, SCBE, HALF, DLB, B/C, EXT

## ■RECOMMENDED OPERATING CONDITIONS

( $f_{osc} = 4.032\text{MHz}$ ,  $V_{SS} = V_{EE} = 0V$ )

| Parameter                          | Symbol           | Conditions             | Min      | Typ | Max      | Unit |
|------------------------------------|------------------|------------------------|----------|-----|----------|------|
| Supply voltage for analog section  | $V_{CC}$         | —                      | 4.75     | 5.0 | 5.25     | V    |
| Supply voltage for digital section | $V_{DD}$         | —                      | 4.75     | 5.0 | 5.25     | V    |
| Analog input voltage               | $V_{IA}$         | —                      | $V_{EE}$ | —   | $V_{CC}$ | V    |
| Digital input voltage              | $V_{ID}$         | —                      | $V_{SS}$ | —   | $V_{DD}$ | V    |
| Operating temperature              | $T_{opr}$        | —                      | -10      | 25  | 70       | °C   |
| Oscillating frequency tolerance    | $\Delta f_{osc}$ | Crystal/External clock | -0.01    | 0   | +0.01    | %    |

## ■ELECTRICAL CHARACTERISTICS

### ●DC Electrical Characteristics

( $V_{DD} = 5.0V$ ,  $V_{SS} = V_{EE} = 0V$ ,  $T_a = 25^\circ\text{C}$ )

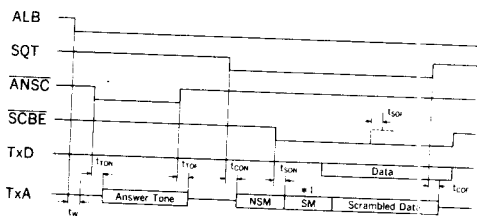
| Parameter                                    |            | Symbol     | Conditions                   | Min      | Typ | Max      | Unit          |
|----------------------------------------------|------------|------------|------------------------------|----------|-----|----------|---------------|
| Digital section operating current            | Operating  | $I_{DDO}$  | SQT or ALB = "L"             | —        | 3   | 5        | mA            |
|                                              | Power-down | $I_{DDs}$  | SQT = ALB = "H"              | —        | —   | 1        | $\mu\text{A}$ |
| High level input voltage                     |            | $V_{IH}$   | *1                           | 3.5      | —   | $V_{DD}$ | V             |
| Low level input voltage                      |            | $V_{IL}$   |                              | $V_{SS}$ | —   | 1.5      | V             |
| High level input current                     |            | $I_{IH}$   | *1                           | —        | —   | 1        | $\mu\text{A}$ |
| Low level input current                      |            | $I_{IL}$   |                              | 5        | 10  | 30       | $\mu\text{A}$ |
| High level output current                    |            | $I_{OH}$   | $V_{OH} = 4.5V^{*2}$         | —        | 3.5 | —        | mA            |
| Low level output current                     |            | $I_{OL}$   | $V_{OL} = 0.5V^{*2}$         | —        | 3.5 | —        | mA            |
| Analog section operating current             | Operating  | $I_{CCO}$  | SQT or ALB = "L"             | —        | 20  | 30       | mA            |
|                                              | Power-down | $I_{CCs}$  | SQT = ALB = "H"              | —        | —   | 1        | $\mu\text{A}$ |
| Output DC impedance                          |            | $Z_{SG}$   | SG                           | —        | 70  | 150      | $\Omega$      |
|                                              |            | $Z_{TxA}$  | TxA                          | —        | 150 | 250      | $\Omega$      |
| Reference voltage generator output impedance |            | $Z_{TLA}$  | $V_{TLA} - V_{SG} \geq 1.0V$ | 20       | —   | 500      | $k\Omega$     |
|                                              |            | $Z_{CDA}$  | $V_{CDA} - V_{SG} \geq 1.0V$ | 20       | —   | 500      | $k\Omega$     |
| Input DC impedance                           |            | $Z_{RxA}$  | RxA                          | 5        | —   | —        | $M\Omega$     |
|                                              |            | $Z_{MADJ}$ | MADJ                         | 5        | —   | —        | $M\Omega$     |

\*1 Digital input terminal except for OSC1. (pull-up resistor is built-in)

\*2 ST, LMON, PSD, ED, RT, RxD, NSM

## ● AC Electrical Characteristics

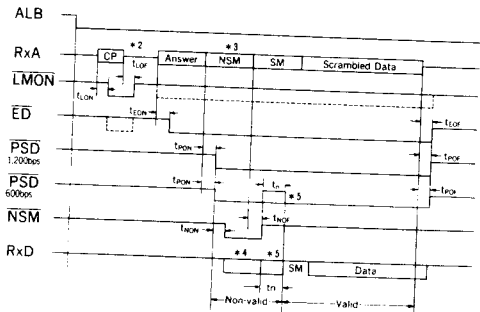
### ○ Transmit



\*1 The scramble start in Bell mode ( $B/\bar{C} = "H"$ ) requires the training signal (voluntary serial data including "0") to TxD after SCBE→"L".

NSM : Non Scrambled Mark  
SM : Scrambled Mark

### ○ Receive



\*2 Call Progress Tone  
\*3 Non Scrambled Mark  
\*4 During NSM = "L" ; Rx D→"H" (fixed) when  $B/\bar{C} = "H"$   
Rx D→"L" (fixed) when  $B/\bar{C} = "L"$   
\*5 Rx D output or PSD output are invalid because the demodulator is capturing.

### ○ Transmitter

( $f_{osc} = 4.032\text{MHz}$ ,  $V_{DD} = V_{CC} = 5.0\text{V}$ ,  $T_a = 25^\circ\text{C}$ )

| Delay time           | Trigger signal      | Symbol    | Min | Typ | Max  | Unit |
|----------------------|---------------------|-----------|-----|-----|------|------|
| Power-on             | ALB or SQT→"L"      | $t_w$     | —   | 50  | 100  | ms   |
| Answer tone transmit | SQT = "H", ANSC→"L" | $t_{TON}$ | —   | —   | 2    | ms   |
| Answer tone stop     | SQT = "H", ANSC→"H" | $t_{TOF}$ | —   | —   | 2    | ms   |
| Carrier transmit     | SQT→"L"             | $t_{CON}$ | —   | —   | 2    | ms   |
| Carrier stop         | ANSC = "H", SQT→"H" | $t_{COF}$ | —   | —   | 2    | ms   |
| Scrambler start      | SQT = "L", SCBE→"L" | $t_{SON}$ | —   | —   | 70*6 | ms   |
| Scrambler stop       | SQT = "L", SCBE→"H" | $t_{SOF}$ | —   | —   | 10   | ms   |

\*6 In case of CCITT mode, 1,200 bps

### ○ Receiver

( $f_{osc} = 4.032\text{MHz}$ ,  $V_{DD} = V_{CC} = 5.0\text{V}$ ,  $T_a = 25^\circ\text{C}$ )

| Delay time                        | Input signal                    | Symbol    | Min | Typ | Max | Unit |
|-----------------------------------|---------------------------------|-----------|-----|-----|-----|------|
| Call progress tone detection time | Call progress tone              | $t_{LON}$ | —   | —   | 150 | ms   |
|                                   |                                 | $t_{LOF}$ | —   | —   | 150 | ms   |
| Carrier detection time            | Signal within receive band      | $t_{EON}$ | —   | —   | 20  | ms   |
|                                   |                                 | $t_{EOF}$ | —   | 40  | 70  | ms   |
| PSK energy detection time         | Phase shifted signal (600 baud) | $t_{PON}$ | —   | 200 | 300 | ms   |
|                                   |                                 | $t_{POF}$ | —   | —   | 100 | ms   |
| Non-scrambled mark detection time | Non-scrambled mark              | $t_{NON}$ | —   | —   | 60  | ms   |
|                                   |                                 | $t_{NOF}$ | —   | —   | 10  | ms   |
| Settling time                     | Scrambled data                  | $t_n$     | —   | —   | 600 | ms   |

## ● Analog Characteristics

### ○ Transmitter

( $V_{CC}=5.0V$ ,  $T_a=25^{\circ}C$ , TLA is opened)

| Parameter                 | Symbol | Condition         | Min   | Typ   | Max   | Unit |
|---------------------------|--------|-------------------|-------|-------|-------|------|
| Tone frequency            | $f_r$  | Bell Answer tone  | 2,205 | 2,225 | 2,245 | Hz   |
|                           |        | CCITT Answer tone | 2,090 | 2,100 | 2,110 |      |
|                           |        | CCITT Guard tone  | 1,790 | 1,800 | 1,810 |      |
| Transmit level            | P      | Answer tone       | -12.0 | -10.5 | -9.0  | dBm  |
|                           |        | PSK carrier       | -13.5 | -12.0 | -10.5 |      |
| Unexpected transmit level | $P_E$  | $f=4$ to 8kHz     | —     | —     | P-20  | dBm  |
|                           |        | $f=8$ to 12kHz    | —     | —     | P-40  |      |
|                           |        | $f \geq 12kHz$    | —     | —     | P-60  |      |

### ○ Receiver

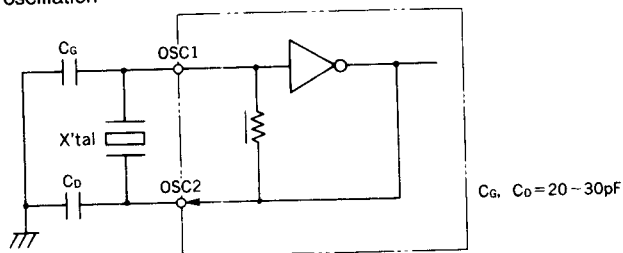
( $V_{CC}=5.0V$ ,  $T_a=25^{\circ}C$ , CDA is opened)

| Parameter                          | Symbol    | Condition                          | Min | Typ | Max | Unit |
|------------------------------------|-----------|------------------------------------|-----|-----|-----|------|
| Allowable input range              | DR        | at RxA                             | -40 | —   | -5  | dBm  |
| Carrier detection level            | $L_{ON}$  | OFF→ON (On level)                  | -43 | —   | —   | dBm  |
|                                    | $L_{OFF}$ | ON→OFF (Off level)                 | —   | —   | -48 | dBm  |
|                                    | $L_H$     | Hysteresis width                   | 1   | 2   | —   | dB   |
| Call progress tone detection level | $L_D$     | $V_{EE} \leq V_{MADJ} \leq V_{CC}$ | —   | —   | -32 | dBm  |
|                                    | $L_{AR}$  | $L_D$ (Max) - $L_D$ (Min)          | 10  | —   | —   | dB   |

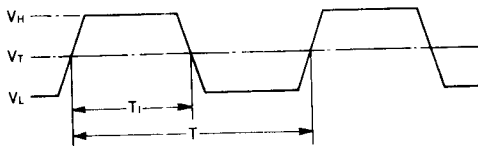
## ■ FUNCTIONS

### ● Oscillating Circuit

#### ○ Crystal quartz oscillation



#### ○ External clock into OSC1



| Parameter | Symbol  | Condition            | Tolerance    |
|-----------|---------|----------------------|--------------|
| Amplitude | $V_H$   | $\geq V_{DD} - 1.0V$ | —            |
|           | $V_L$   | $\leq V_{SS} + 1.0V$ | —            |
| Frequency | $1/T$   | 4.032MHz             | $\pm 0.01\%$ |
| Duty      | $T_I/T$ | 50%                  | $\pm 15\%$   |

## ●Operation Mode

| ALB        | SQT        | Mode                              |
|------------|------------|-----------------------------------|
| High level | Low level  | Normal mode (transmission enable) |
|            | High level | Transmission disable mode         |
| Low level  | Low level  | Analog loop-back test mode        |
|            | High level | Power-down mode                   |

### ○Power-down mode

During both ALB and SQT are high level, oscillation stops and operating current is to be below  $2\mu A$ .

### ○Analog loop-back test mode

In the analog loop-back test mode, the functional test (including LSI) should be easily done, because transmission data into TxD are sent to the demodulator through the modulator automatically and appear from RxD again.

During this mode, transmit buffer so operates that test signal can be monitored, and, input signal into RxD is ignored by the demodulator but call progress tone can be detected.

### ○Transmission disable mode

In this mode, the transmitter stops its operation but the receiver operates.

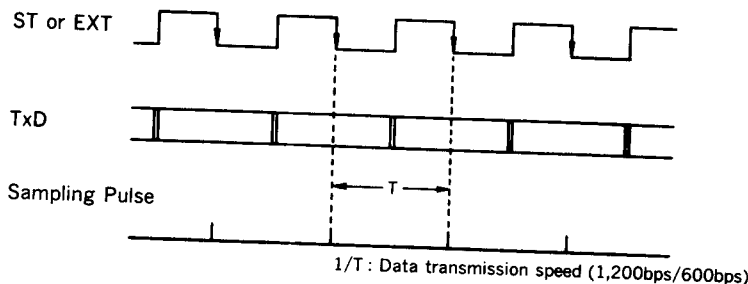
And the answer tone should be transmitted by  $\overline{ANSC}$  being low level.

### ○Normal mode

Both the transmitter and the receiver become active, the PSK modulated signal which has a center frequency of 1,200Hz or 2,400Hz (depend on  $O/\overline{A}$  input) can be transmitted, and a  $1,800 \pm 10$ Hz guard tone can be transmitted when  $\overline{ANSC} = "L"$  and CCITT answer mode are selected.

## ●Transmitter

### ○Relation between input data and transmit timing signal



In case of using an external transmit timing (EXT), the frequency tolerance of EXT should be less than  $\pm 0.01\%$  of data transmission speed.

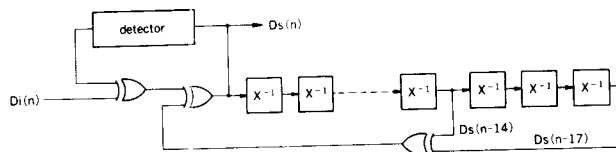
## ○ Scrambler

[Scrambler control]

| Transmit data | SCBE       | Algorithm                             |
|---------------|------------|---------------------------------------|
| Scrambled     | Low level  | $Ds(n) = Di(n) + Ds(n-14) + Ds(n-17)$ |
| Non-scrambled | High level | $Ds(n) = Di(n)$                       |

- $Di(n)$  ; Input data (TxD)
- $Ds(n-k)$  ; Scrambler output (k is output data of k times before)
- + ; Logical addition (mod 2)

[Construction]



- $x^{-1}$  ; 1 bit delay circuit
- detector ; In the CCITT mode ( $B/\bar{C} = "L"$ ), if it detects 64 or more continuous mark data in the output of the scrambler, this inverts the polarity of the following input data.  
In the Bell mode ( $B/\bar{C} = "H"$ ), the detector output becomes invalid, so that the training signal (voluntary serial data including "0") are required into TxD to start the scrambler.

## ○ Modulation

[Base-band modulation]

- 4-phase differential modulation

| 1,200bps | 600bps | Phase shift (deg) |
|----------|--------|-------------------|
| 0 0      | 0      | + 90              |
| 0 1      | —      | + 0               |
| 1 1      | 1      | +270              |
| 1 0      | —      | +180              |

- Roll off characteristic .....75% cosine roll off

[Transmit carrier frequency]

Originate mode .....1,200Hz  $\pm$  0.01%

Answer mode .....2,400Hz  $\pm$  0.01%

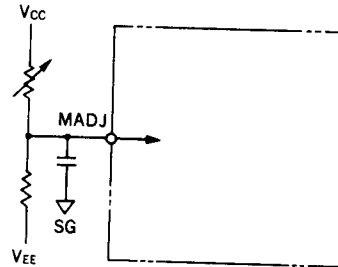
## ○ Tone Generator

| Name        | SQT | ANSC | O/A | B/C | Frequency          |
|-------------|-----|------|-----|-----|--------------------|
| Answer tone | "H" | "L"  | —   | "L" | 2,100Hz $\pm$ 10Hz |
|             |     |      |     | "H" | 2,225Hz $\pm$ 20Hz |
| Guard tone  | "L" | "H"  | "L" | "L" | 1,800Hz $\pm$ 10Hz |

● **Receiver**

- **Call progress tone detection**

The definitions of the call progress tone are different in each country, so that an appropriate detection level can be adjusted by some external voltage through the MADJ terminal.



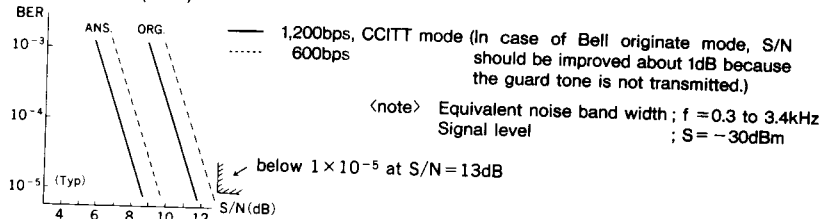
### ○ Demodulation

[Demodulated carrier frequency]

| Mode      | O/A | Carrier frequency | Tolerance    |
|-----------|-----|-------------------|--------------|
| Originate | H   | 2,400Hz           | $\pm 0.01\%$ |
| Answer    | L   | 1,200Hz           | $\pm 0.01\%$ |

[Data reliability]

- Bit error rate (BER)



- Allowable range of the factor which makes the line characteristic worse

| Factor           | Symbol     | Range    | Unit |
|------------------|------------|----------|------|
| Frequency offset | $\Delta f$ | $\pm 7$  | Hz   |
| Phase jitter     | $\theta_j$ | $\pm 20$ | deg  |

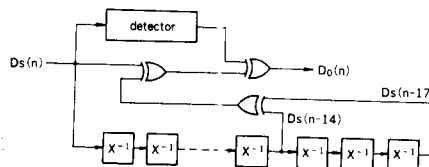
- **Descrambler**

**[Algorithm]**

$$D_o(n) = D_s(n) + D_s(n-14) + D_s(n-17)$$

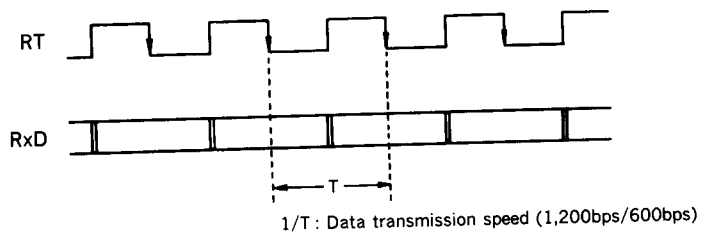
- $Do(n)$  ; Output data (RxD)
- $Ds(n-k)$  ; Descrambler input (k is input data of k times before)
- $+$  ; Logical addition (mod 2)

[Construction]



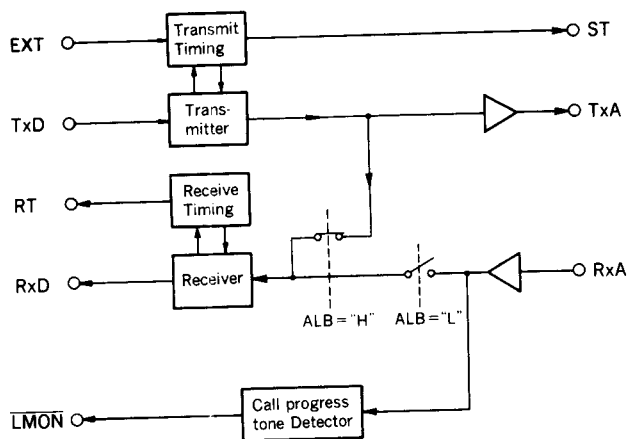
- $x^{-1}$  : 1 bit delay circuit
- detector: In the CCITT mode ( $B/\overline{C}$ ="L"), if it detects 64 or more continuous mark data in the input of the descrambler, this inverts the polarity of the following output data and outputs low level to  $\overline{NSM}$ .  
In the Bell mode ( $B/\overline{C}$ ="H"), the detector output is invalid for the descrambler, but valid for the  $\overline{NSM}$  output.

○ Relation between output data (RxD) and receive timing output (RT)

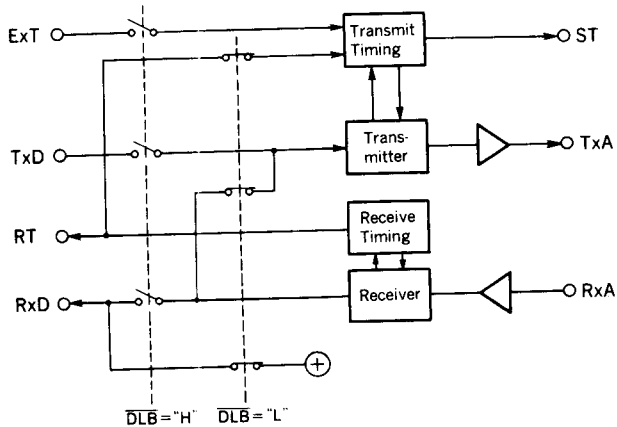


■ TEST FUNCTIONS

● Analog loop-back test



● Digital remote loop-back test



●Circuit for intelligent MODEM card



**C28**

28-pin DIP

1.472Max  
(37.4Max)  
1.445±0.004  
(36.7±0.1)

28 15

0.628±0.004  
(15.94±0.1)

1 14

0.059  
(1.5)

0.024±0.004  
(0.6±0.1)

0.181±0.004  
(4.6±0.1)

0.139±0.004  
(3.53±0.1)

0.100±0.010  
(2.54±0.25)

0.018±0.004  
(0.46±0.1)

0.600  
(15.24)

0.600-0.655  
(15.24-16.64)

0.010-0.004  
0.03  
0.25±0.1

unit : inch  
(mm)

