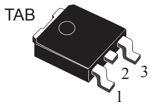
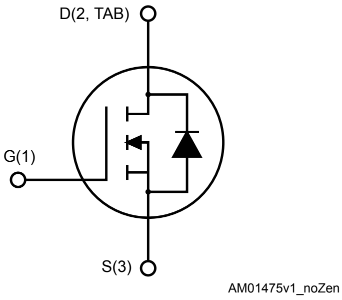
# STD10NF30

Datasheet

# Automotive-grade N-channel 300 V, 0.28 Ω typ., 10 A, MESH OVERLAY™ Power MOSFET in a DPAK package



**DPAK**



## Features

| Order code | $V_{DS}$ | $R_{DS(on)}$ max. | $I_D$ |
|---|---|---|---|
| STD10NF30 | 300 V | 0.33 Ω | 10 A |

- AEC-Q101 qualified
- 100% avalanche tested
- Low capacitance and gate charge
- 175 °C maximum junction temperature

## Applications

- Switching applications

## Description

This fully clamped MOSFET is produced using ST’s latest advanced Mesh overlay process, which is based on an innovative strip layout. The inherent benefits of the new technology coupled with the extra clamping capabilities make this product particularly suitable for the harshest operation conditions, such as those encountered in the automotive environment. The device is also well-suited for other applications where extra ruggedness is required.

| Product status link |
|---|
| STD10NF30 |

| Product summary | |
|---|---|
| **Order code** | STD10NF30 |
| **Marking** | 10NF30 |
| **Package** | DPAK |
| **Packing** | Tape and reel |

# 1 Electrical ratings

Table 1. **Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source voltage | 300 | V |
| $V_{GS}$ | Gate-source voltage | ±20 | V |
| $I_D$ | Drain current (continuous) at $T_C$ = 25 °C | 10 | A |
|  | Drain current (continuous) at $T_C$ = 100 °C | 6.3 | A |
| $I_{DM}$(1) | Drain current (pulsed) | 40 | A |
| $P_{TOT}$ | Total dissipation at $T_C$ = 25 °C | 103 | W |
| dv/dt(2). | Peak diode recovery voltage slope | 12 | V/ns |
| $T_{stg}$ | Storage temperature range | -55 to 175 | °C |
| $T_j$ | Operating junction temperature range |  |  |

1. *Pulse width limited by safe operating area.*
2. *$I_{SD}$ ≤ 10 A, di/dt ≤ 200 A/μs, $V_{DD}$= 80% $V_{(BR)DSS}$*

Table 2. **Thermal data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj\text{-}case}$ | Thermal resistance junction-case | 1.45 | °C/W |
| $R_{thj\text{-}pcb}$(1) | Thermal resistance junction-pcb | 50 | °C/W |

1. *When mounted on 1 inch² FR-4, 2 Oz copper board.*

Table 3. **Avalanche characteristics**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $I_{AR}$ | Avalanche current, repetitive or non-repetitive<br>(pulse width limited by $T_{Jmax}$) | 6 | A |
| $E_{AS}$ | Single pulse avalanche energy<br>(starting $T_j$ = 25 °C, $I_D$ = $I_{AR}$, $V_{DD}$ = 50 V) | 175 | mJ |

## 2 Electrical characteristics

$T_{CASE}$ = 25 °C unless otherwise specified.

Table 4. **On/off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS}$ = 0 V, $I_D$ = 1 mA | 300 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current | $V_{GS}$ = 0 V, $V_{DS}$ = 300 V | | | 1 | µA |
| | | $V_{GS}$ = 0 V, $V_{DS}$ = 300 V,<br>$T_C$ = 125 °C(1) | | | 10 | µA |
| $I_{GSS}$ | Gate body leakage current | $V_{DS}$ = 0 V, $V_{GS}$ = ±20 V | | | ±100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DD}$ = $V_{GS}$, $I_D$ = 250 µA | 2 | 3 | 4 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS}$ = 10 V, $I_D$ = 5 A | | 0.28 | 0.33 | Ω |

1. *Defined by design, not subject to production test.*

Table 5. **Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$ | Input capacitance | $V_{DS}$ = 25 V, f = 1 MHz,<br>$V_{GS}$ = 0 V | - | 780 | - | pF |
| $C_{oss}$ | Output capacitance | | - | 110 | - | pF |
| $C_{rss}$ | Reverse transfer capacitance | | - | 15 | - | pF |
| $Q_g$ | Total gate charge | $V_{DD}$ = 240 V, $I_D$ = 10 A<br>$V_{GS}$ = 0 to 10 V<br>(see Figure 13. Test circuit for gate charge behavior) | - | 23 | - | nC |
| $Q_{gs}$ | Gate-source charge | | - | 3.5 | - | nC |
| $Q_{gd}$ | Gate-drain charge | | - | 11.3 | - | nC |

Table 6. **Switching times**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD}$ = 150 V, $I_D$ = 5 A,<br>$R_G$ = 4.7 Ω, $V_{GS}$ = 10 V<br>(see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform) | - | 13.5 | - | ns |
| $t_r$ | Rise time | | - | 9.5 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 32 | - | ns |
| $t_f$ | Fall time | | - | 9.5 | - | ns |

Table 7. **Source-drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | - | | 10 | A |
| $I_{SDM}$(1) | Source-drain current (pulsed) | | - | | 40 | A |
| $V_{SD}$(2) | Forward on voltage | $I_{SD}$ = 10 A, $V_{GS}$ = 0 V | - | | 1.5 | V |

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 10 A, di/dt = 100 A/µs,<br>$V_{DD}$ = 60 V<br>(see Figure 14. Test circuit for inductive load switching and diode recovery times) | - | 145 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 0.76 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 10.3 | | A |
| $t_{rr}$ | Reverse recovery time | $I_{SD}$ = 10 A, di/dt = 100 A/µs,<br>$V_{DD}$ = 60 V, $T_J$ = 150 °C<br>(see Figure 14. Test circuit for inductive load switching and diode recovery times) | - | 174 | | ns |
| $Q_{rr}$ | Reverse recovery charge | | - | 1.08 | | µC |
| $I_{RRM}$ | Reverse recovery current | | - | 12.5 | | A |

1. *Pulse width limited by safe operating area*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%*

## 2.1 Electrical characteristics (curves)

**Figure 1.** **Safe operating area**

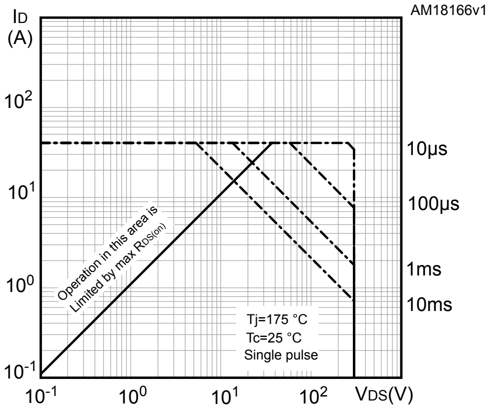


**Figure 2.** **Thermal impedance**

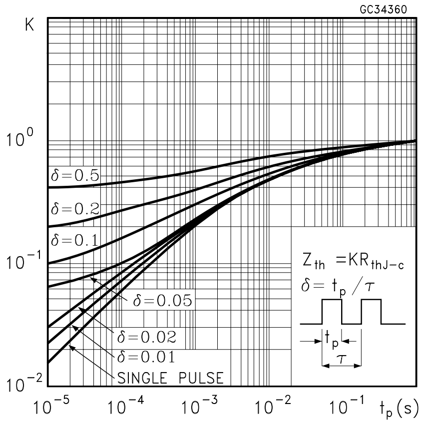


**Figure 3.** **Output characteristics**

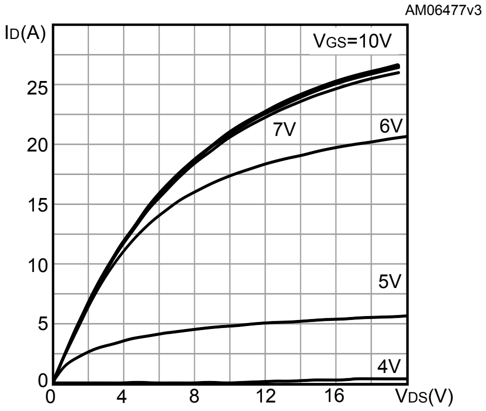


**Figure 4.** **Transfer characteristics**

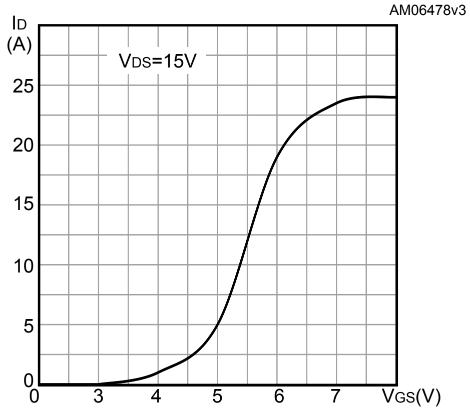


**Figure 5.** **Static drain-source on-resistance**

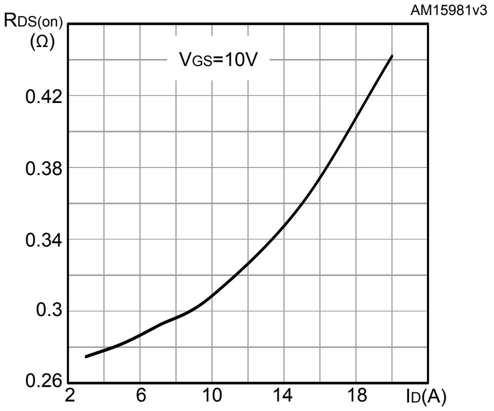


**Figure 6.** **Gate charge vs gate-source voltage**

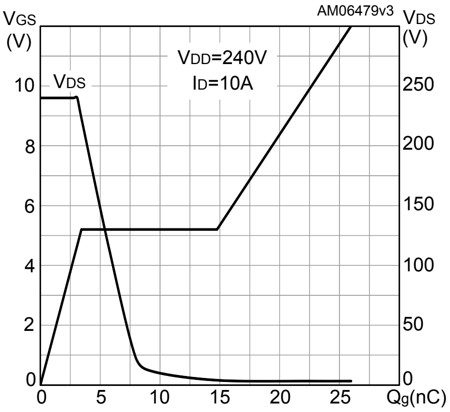


**Figure 7.** Capacitance variations

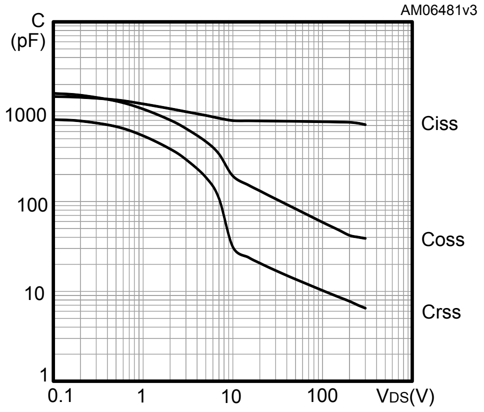


**Figure 8.** Normalized gate threshold voltage vs temperature

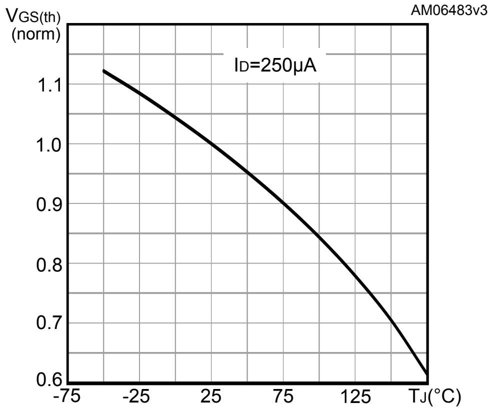


**Figure 9.** Normalized on-resistance vs temperature

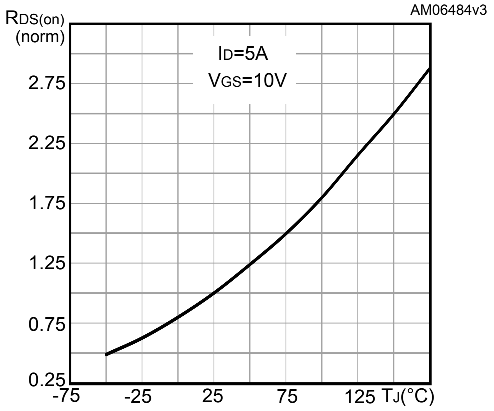


**Figure 10.** Normalized $V_{(BR)DSS}$ vs temperature

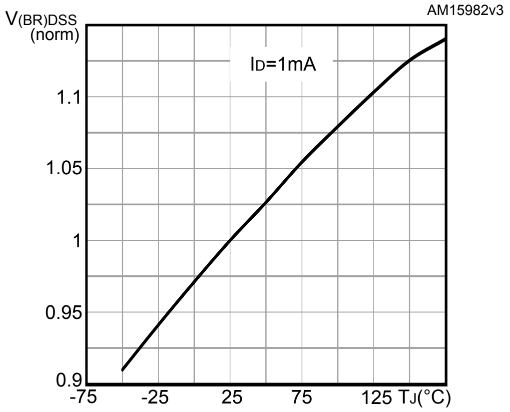
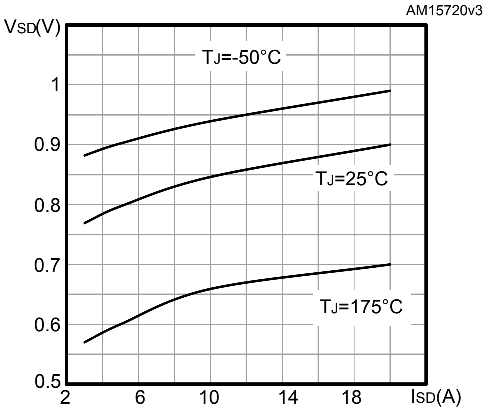


**Figure 11.** Source-drain diode forward characteristics



# 3 Test circuits

**Figure 12.** Test circuit for resistive load switching times

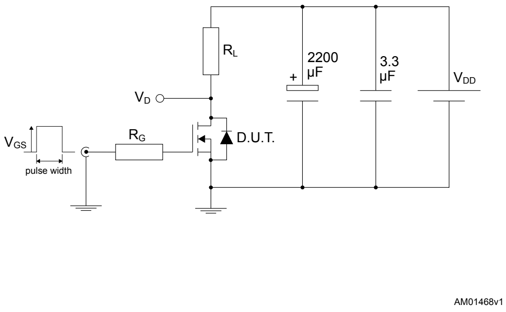


**Figure 13.** Test circuit for gate charge behavior

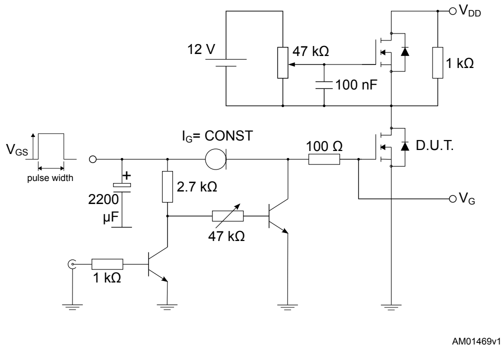


**Figure 14.** Test circuit for inductive load switching and diode recovery times

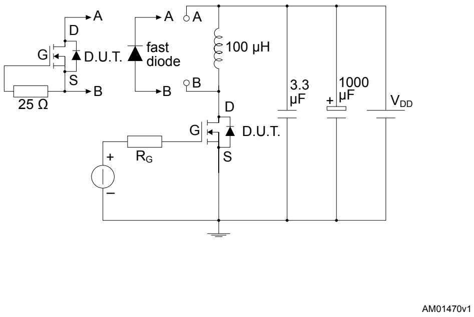


**Figure 15.** Unclamped inductive load test circuit

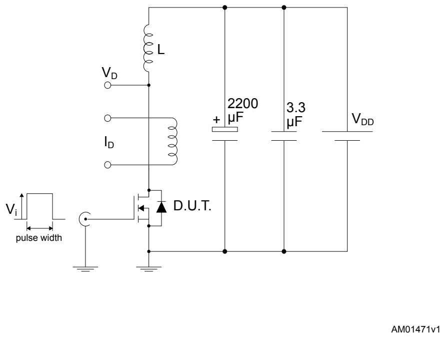


**Figure 16.** Unclamped inductive waveform

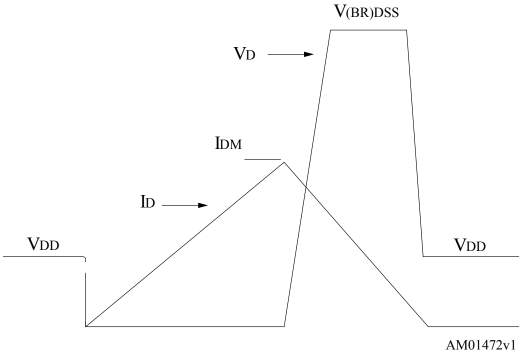
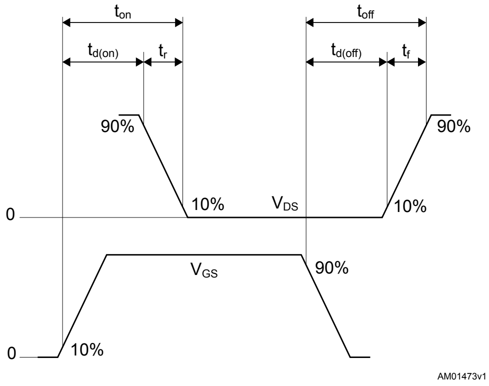


**Figure 17.** Switching time waveform

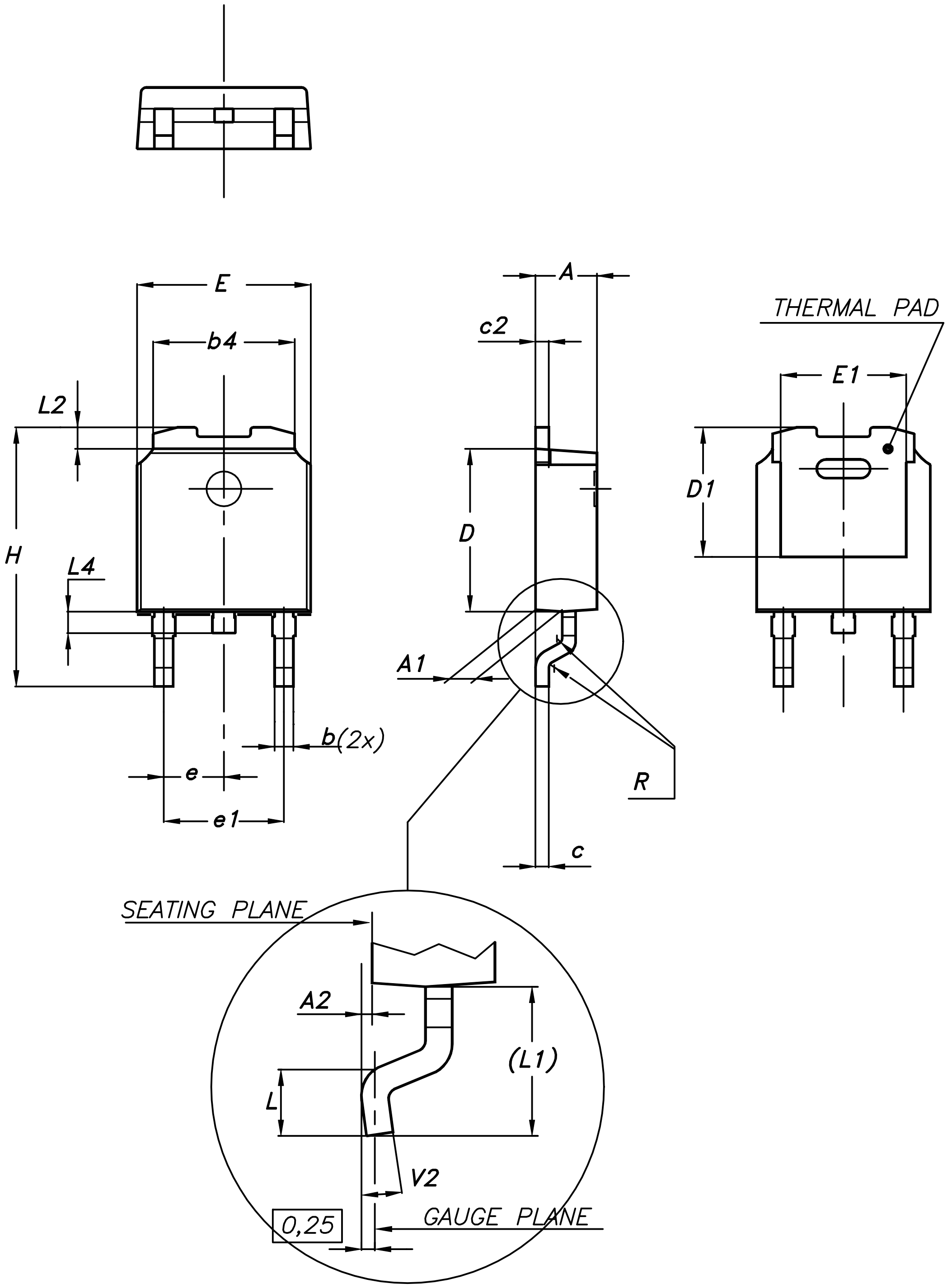


# 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

## 4.1 DPAK (TO-252) type A2 package information

**Figure 18.** DPAK (TO-252) type A2 package outline

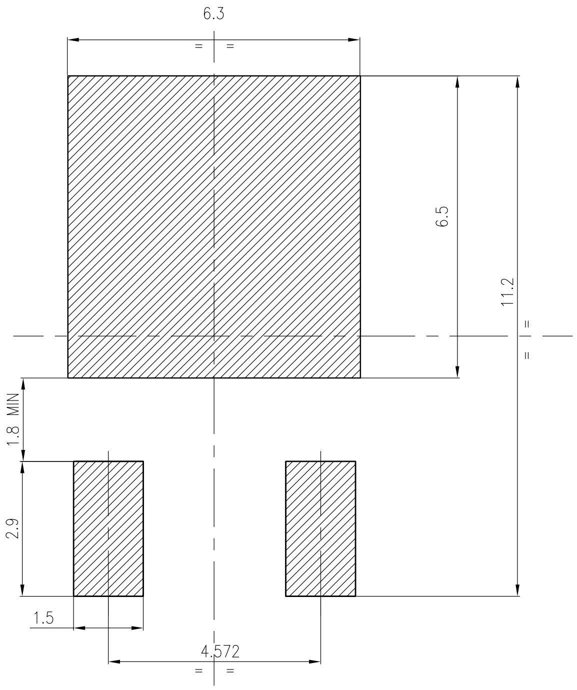


0068772_type-A2_rev25

Table 8. **DPAK (TO-252) type A2 mechanical data**

| Dim. | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 2.20 | | 2.40 |
| A1 | 0.90 | | 1.10 |
| A2 | 0.03 | | 0.23 |
| b | 0.64 | | 0.90 |
| b4 | 5.20 | | 5.40 |
| c | 0.45 | | 0.60 |
| c2 | 0.48 | | 0.60 |
| D | 6.00 | | 6.20 |
| D1 | 4.95 | 5.10 | 5.25 |
| E | 6.40 | | 6.60 |
| E1 | 5.10 | 5.20 | 5.30 |
| e | 2.159 | 2.286 | 2.413 |
| e1 | 4.445 | 4.572 | 4.699 |
| H | 9.35 | | 10.10 |
| L | 1.00 | | 1.50 |
| L1 | 2.60 | 2.80 | 3.00 |
| L2 | 0.65 | 0.80 | 0.95 |
| L4 | 0.60 | | 1.00 |
| R | | 0.20 | |
| V2 | 0° | | 8° |

**Figure 19.** DPAK (TO-252) recommended footprint (dimensions are in mm)



FP_0068772_25

## 4.2 DPAK (TO-252) packing information

**Figure 20. DPAK (TO-252) tape outline**

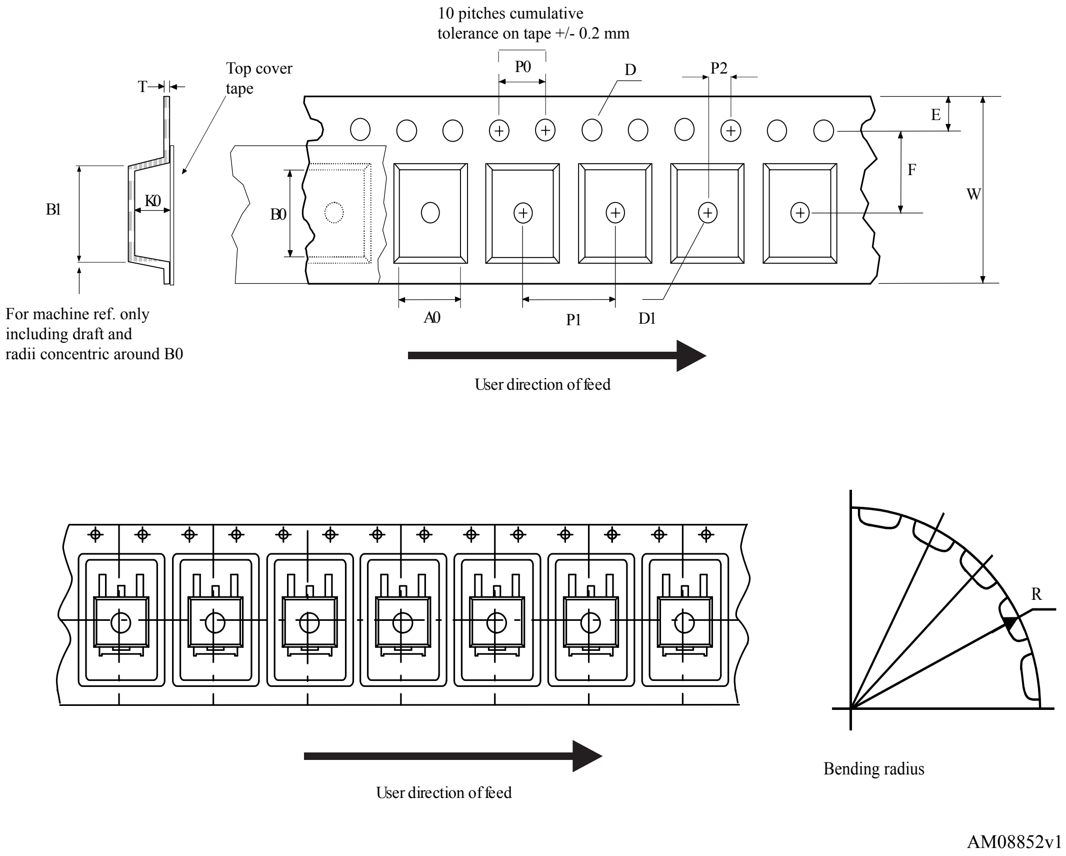
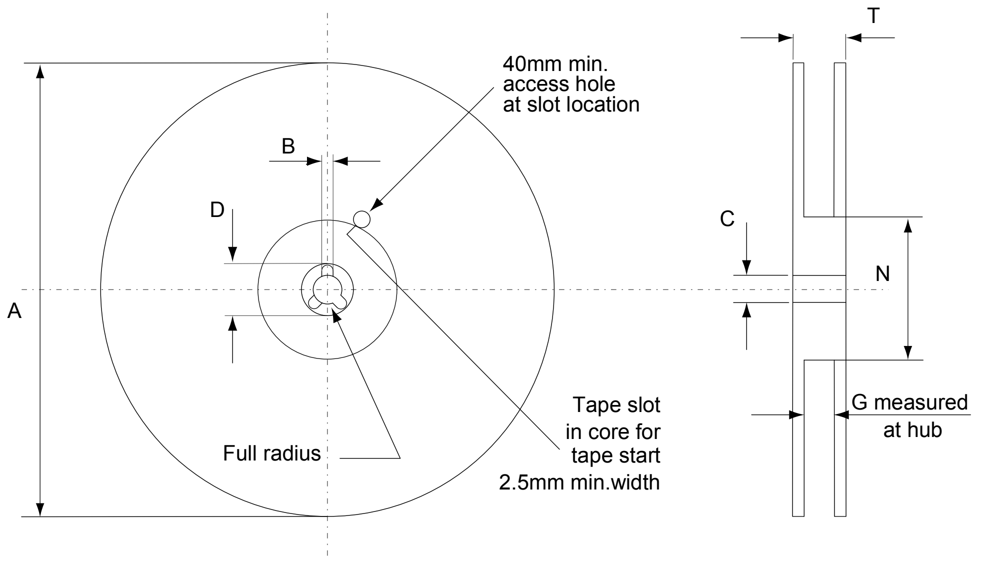


Figure 21. **DPAK (TO-252) reel outline**



AM06038v1

Table 9. **DPAK (TO-252) tape and reel mechanical data**

| Tape | | | Reel | | |
|---|---|---|---|---|---|
| Dim. | mm | | Dim. | mm | |
| | Min. | Max. | | Min. | Max. |
| A0 | 6.8 | 7 | A | | 330 |
| B0 | 10.4 | 10.6 | B | 1.5 | |
| B1 | | 12.1 | C | 12.8 | 13.2 |
| D | 1.5 | 1.6 | D | 20.2 | |
| D1 | 1.5 | | G | 16.4 | 18.4 |
| E | 1.65 | 1.85 | N | 50 | |
| F | 7.4 | 7.6 | T | | 22.4 |
| K0 | 2.55 | 2.75 | | | |
| P0 | 3.9 | 4.1 | Base qty. | | 2500 |
| P1 | 7.9 | 8.1 | Bulk qty. | | 2500 |
| P2 | 1.9 | 2.1 | | | |
| R | 40 | | | | |
| T | 0.25 | 0.35 | | | |
| W | 15.7 | 16.3 | | | |

## Revision history

Table 10. **Document revision history**

| Date | Version | Changes |
|---|---|---|
| 27-Mar-2014 | 1 | Initial release. |
| 02-Jul-2018 | 2 | Removed maturity status indication from cover page. The document status is production data.<br>Updated Section 4.1 DPAK (TO-252) type A2 package information.<br>Minor text changes. |

## Contents