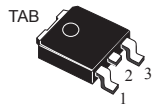
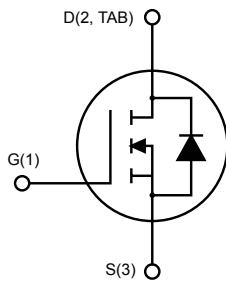


# N-channel 60 V, 3.1 mΩ typ., 80 A STripFET F7 Power MOSFET in a DPAK package


**DPAK**


AM01475v1\_noZen

## Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	P <sub>TOT</sub>
STD140N6F7	60 V	3.8 m Ω	80 A	134 W

- Among the lowest R<sub>DS(on)</sub> on the market
- Excellent FoM (figure of merit)
- Low C<sub>rss</sub>/C<sub>iss</sub> ratio for EMI immunity
- High avalanche ruggedness

## Applications

- Switching applications

## Description

This N-channel Power MOSFET utilizes STripFET F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.



### Product status

STD140N6F7

### Product summary

<b>Order code</b>	STD140N6F7
<b>Marking</b>	140N6F7
<b>Package</b>	DPAK
<b>Packing</b>	Tape and reel

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	60	V
$V_{GS}$	Gate-source voltage	±20	V
$I_D^{(1)}$	Drain current (continuous) at $T_{case} = 25\text{ °C}$	80	A
	Drain current (continuous) at $T_{case} = 100\text{ °C}$	80	
$I_{DM}^{(2)}$	Drain current (pulsed)	320	A
$P_{TOT}$	Total power dissipation at $T_{case} = 25\text{ °C}$	134	W
$E_{AS}^{(3)}$	Single pulse avalanche energy	200	mJ
$dv/dt^{(4)}$	Drain-body diode dynamic $dv/dt$ ruggedness	7.1	V/ns
$T_{stg}$	Storage temperature range	-55 to 175	°C
$T_j$	Operating junction temperature range		

1. Current is limited by package.
2. Pulse width is limited by safe operating area.
3. starting  $T_j = 25\text{ °C}$ ,  $I_D = 20\text{ A}$ ,  $V_{DD} = 30\text{ V}$ .
4.  $I_{SD} = 80\text{ A}$ ;  $di/dt = 600\text{ A}/\mu\text{s}$ ;  $V_{DD} = 48\text{ V}$ ;  $T_j < T_{jmax}$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	50	°C/W
$R_{thj-c}$	Thermal resistance junction-case	1.12	

1. When mounted on FR-4 board of 1 inch<sup>2</sup>, 2oz Cu,  $t < 10\text{ s}$ .

## 2 Electrical characteristics

( $T_{\text{case}} = 25\text{ °C}$  unless otherwise specified)

**Table 3. On/off-states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	60			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 60\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 40\text{ A}$		3.1	3.8	m $\Omega$

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 30\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	3100	-	pF
$C_{oss}$	Output capacitance		-	1520	-	
$C_{rss}$	Reverse transfer capacitance		-	193	-	
$Q_g$	Total gate charge	$V_{DD} = 30\text{ V}$ , $I_D = 80\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 13. Test circuit for gate charge behavior)	-	55	-	nC
$Q_{gs}$	Gate-source charge		-	19	-	
$Q_{gd}$	Gate-drain charge		-	18	-	

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 30\text{ V}$ , $I_D = 40\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	24	-	ns
$t_r$	Rise time		-	68	-	
$t_{d(off)}$	Turn-off delay time		-	39	-	
$t_f$	Fall time		-	20	-	

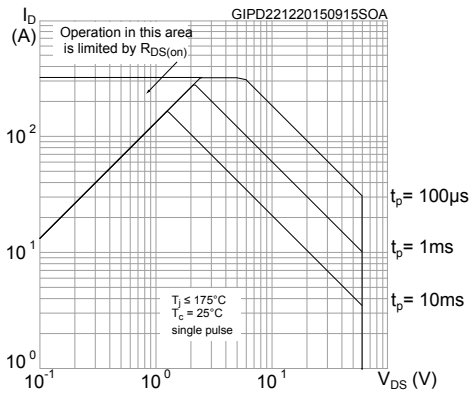
**Table 6. Source-drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(1)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 80\text{ A}$	-		1.2	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 80\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 48\text{ V}$ (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	42.4		ns
$Q_{rr}$	Reverse recovery charge		-	36.2		nC
$I_{RRM}$	Reverse recovery current		-	1.8		A

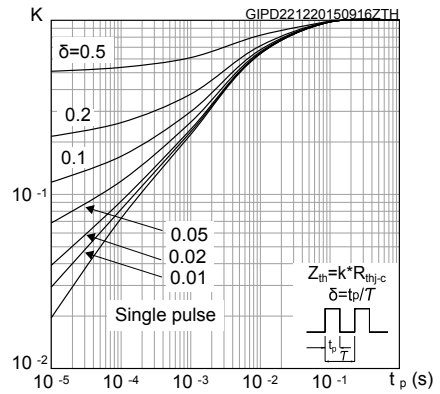
1. Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Characteristics curves

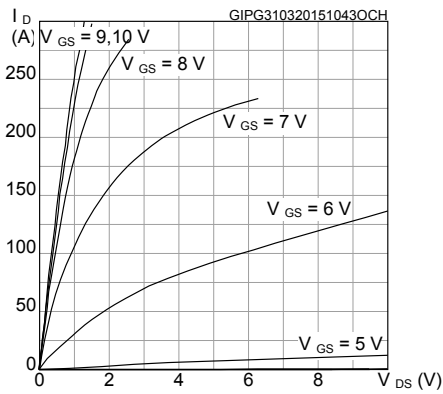
**Figure 1. Safe operating area**



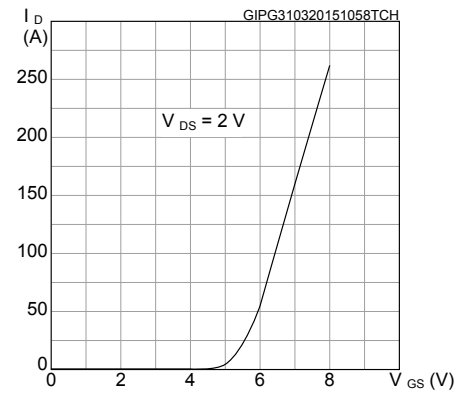
**Figure 2. Thermal impedance**



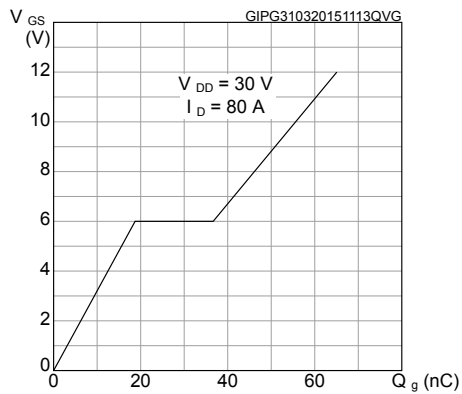
**Figure 3. Output characteristics**



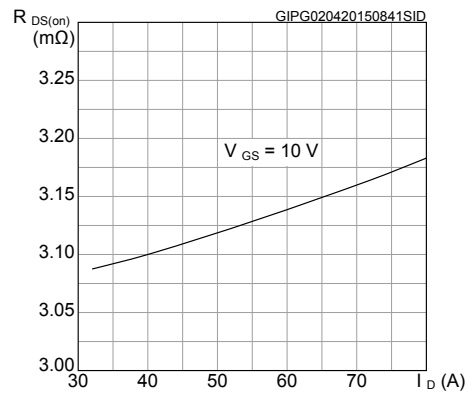
**Figure 4. Transfer characteristics**



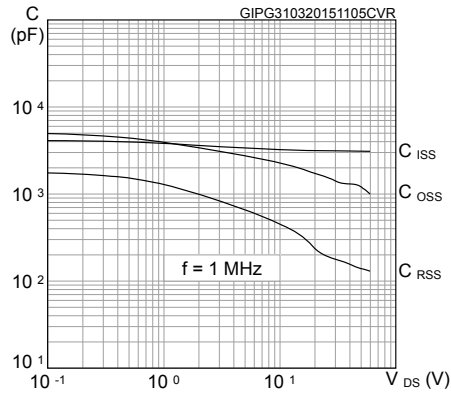
**Figure 5. Gate charge vs gate-source voltage**



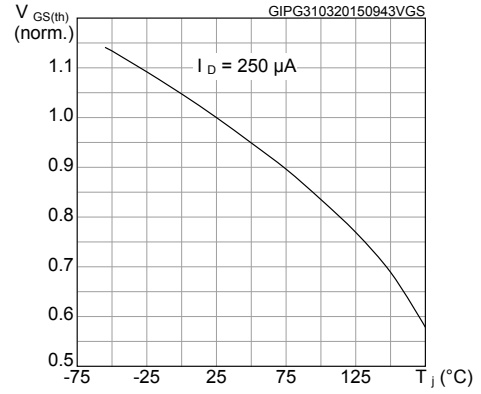
**Figure 6. Static drain-source on-resistance**



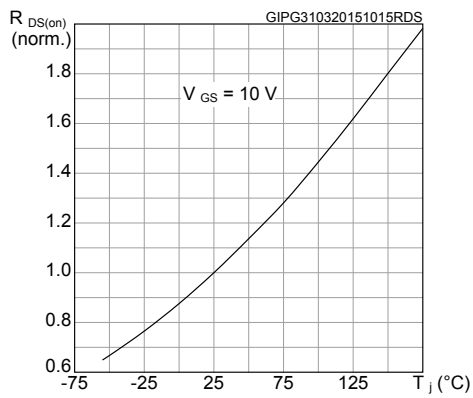
**Figure 7. Capacitance variations**



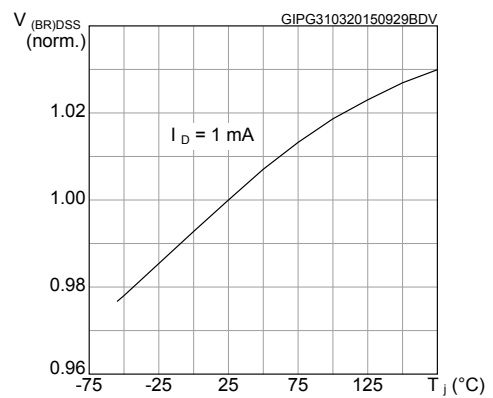
**Figure 8. Normalized gate threshold voltage vs temperature**



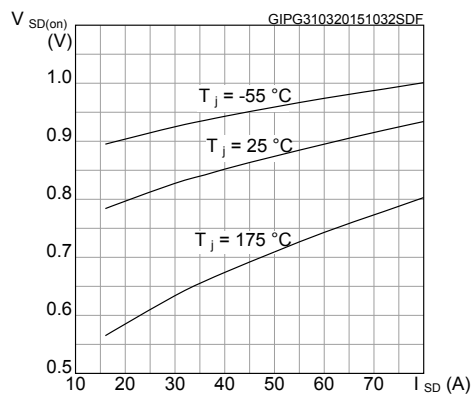
**Figure 9. Normalized on-resistance vs temperature**



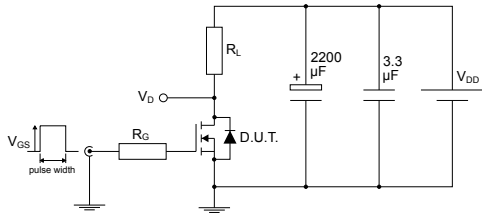
**Figure 10. Normalized V\_(BR)DSS vs temperature**



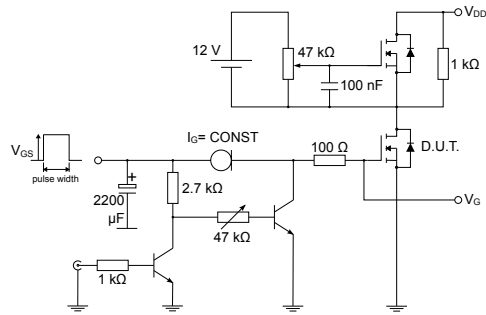
**Figure 11. Source-drain diode forward characteristics**



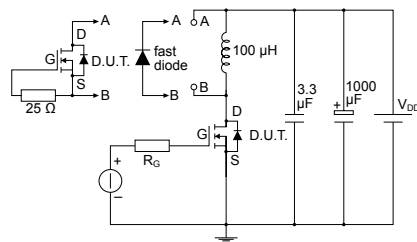
### 3 Test circuits

**Figure 12. Test circuit for resistive load switching times**


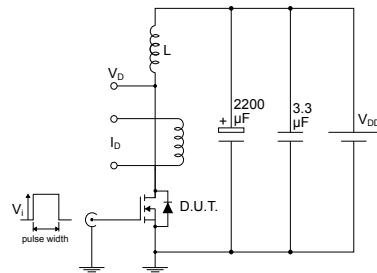
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**Figure 13. Test circuit for gate charge behavior**


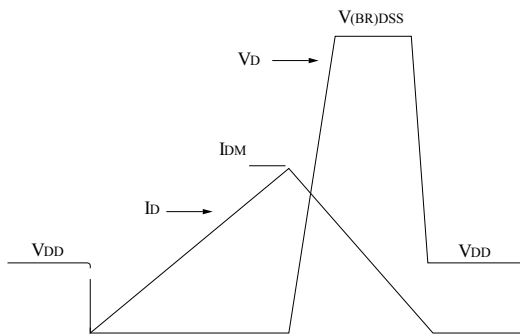
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**Figure 14. Test circuit for inductive load switching and diode recovery times**


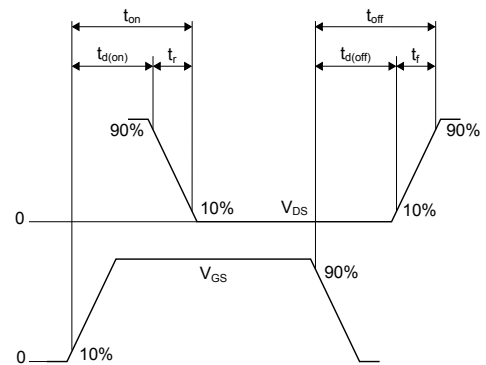
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**Figure 15. Unclamped inductive load test circuit**


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**Figure 16. Unclamped inductive waveform**


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**Figure 17. Switching time waveform**


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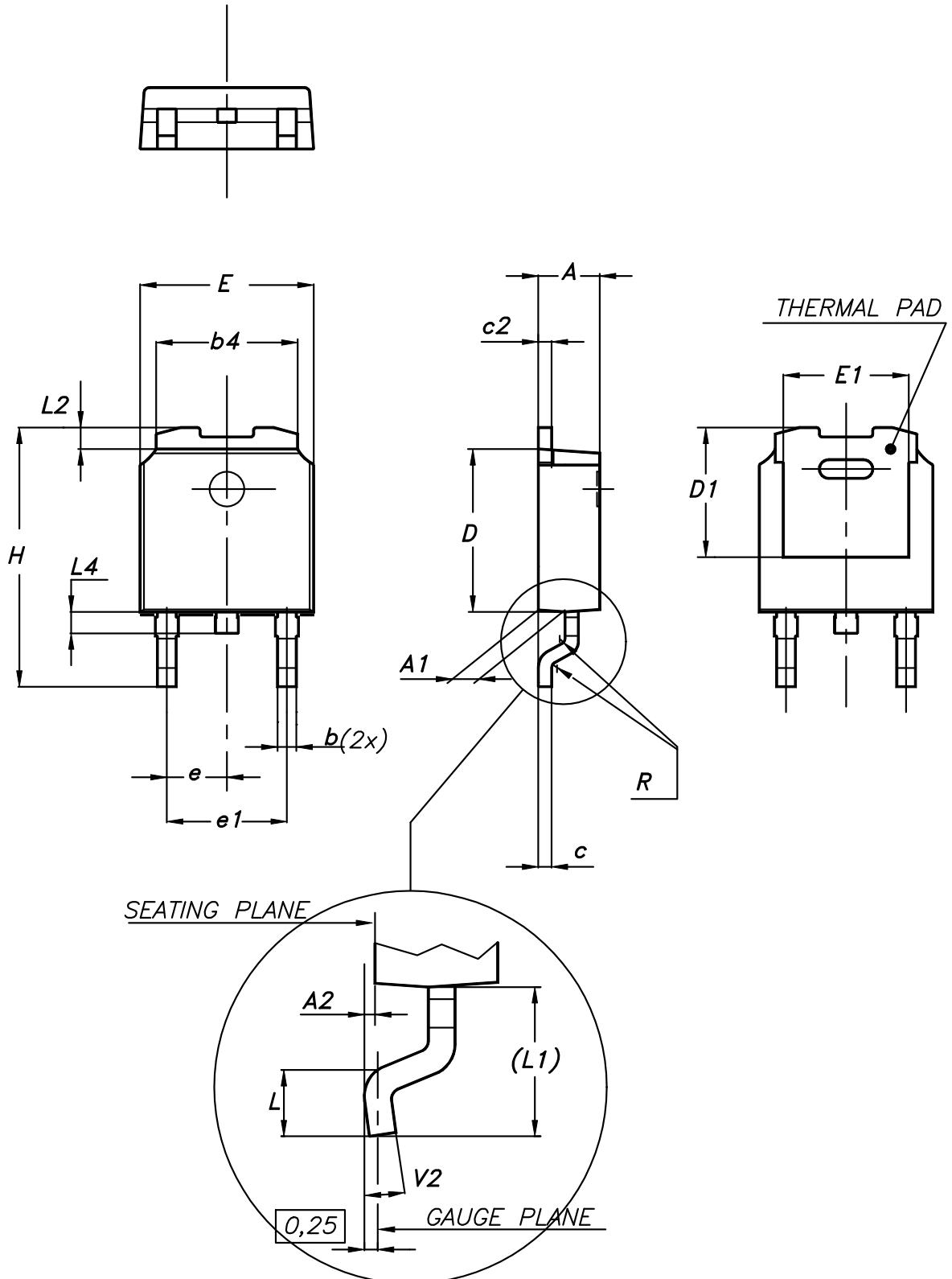
## 4 Package information

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In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 DPAK (TO-252) type A2 package information

Figure 18. DPAK (TO-252) type A2 package outline



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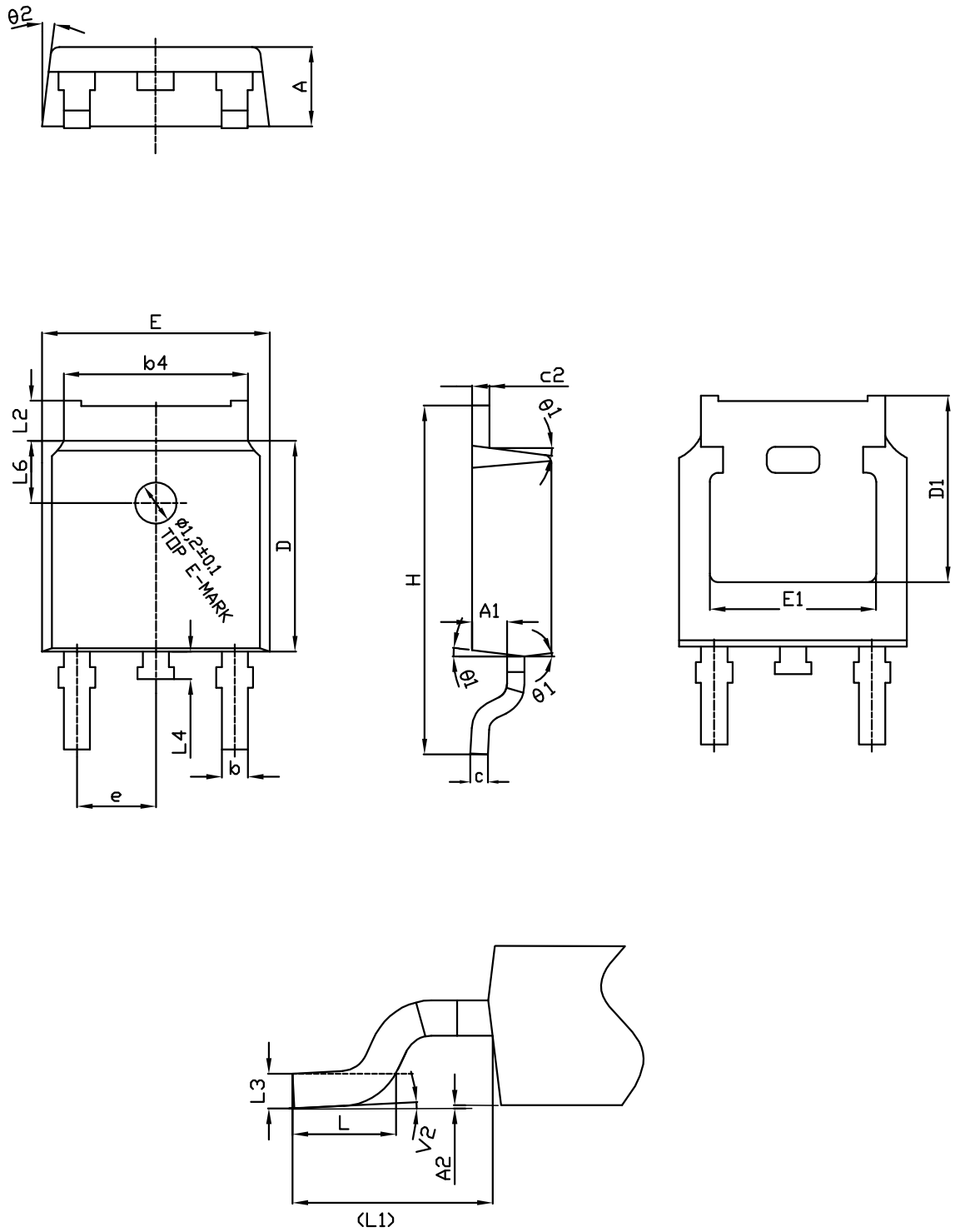


**Table 7. DPAK (TO-252) type A2 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

## 4.2 DPAK (TO-252) type C2 package information

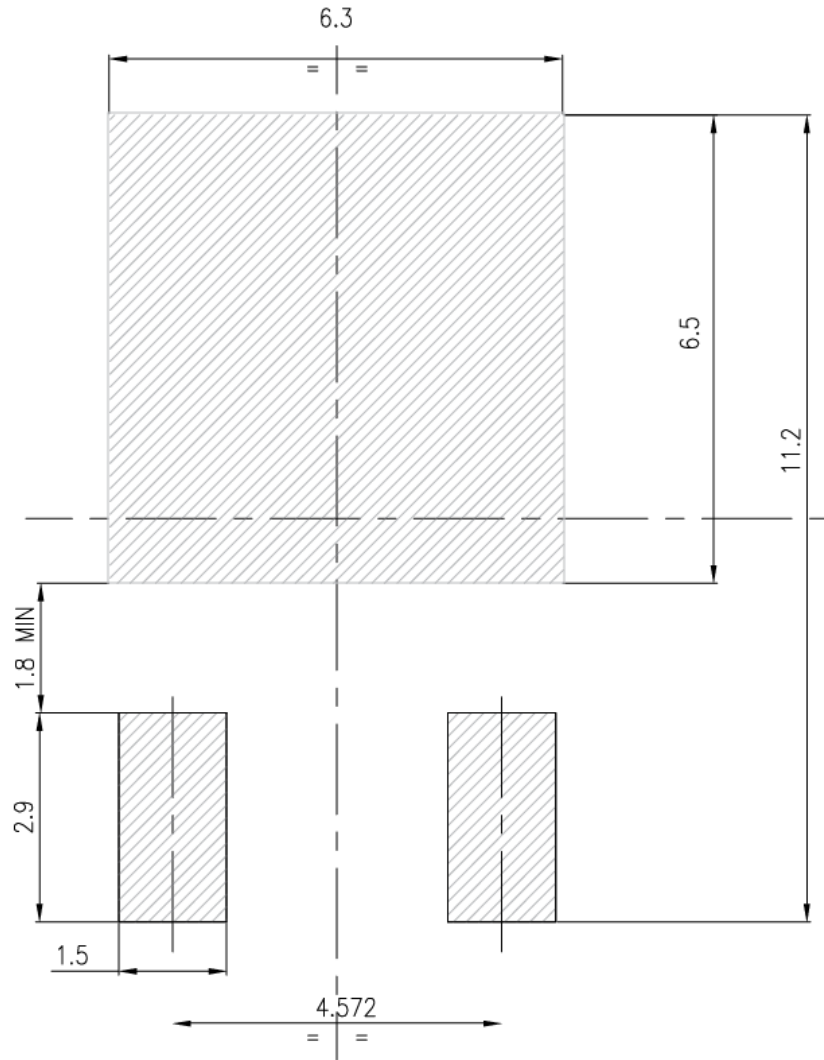
Figure 19. DPAK (TO-252) type C2 package outline



**Table 8. DPAK (TO-252) type C2 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.10		5.60
E	6.50	6.60	6.70
E1	5.20		5.50
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.90		1.25
L3	0.51 BSC		
L4	0.60	0.80	1.00
L6	1.80 BSC		
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

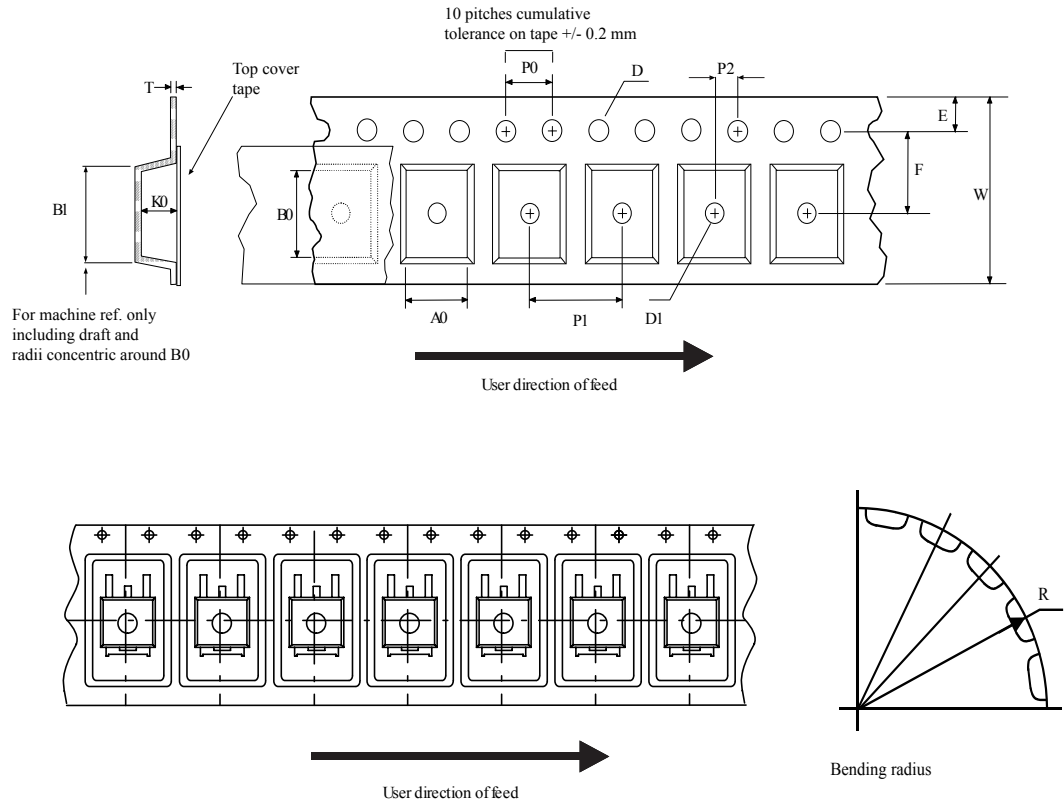
Figure 20. DPAK (TO-252) recommended footprint (dimensions are in mm)



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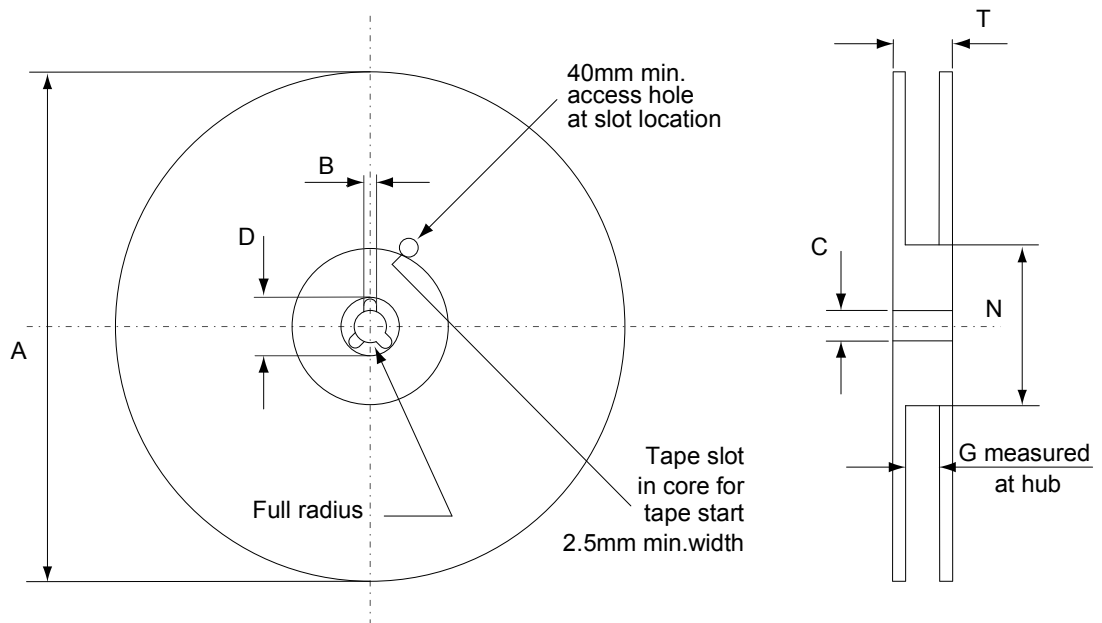
### 4.3 DPAK (TO-252) packing information

Figure 21. DPAK (TO-252) tape outline



AM08852v1

**Figure 22. DPAK (TO-252) reel outline**



AM06038v1

**Table 9. DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1		Base qty.	2500
P1	7.9	8.1		Bulk qty.	2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

## Revision history

**Table 10. Document revision history**

Date	Revision	Changes
21-Dec-2015	1	First release.
11-Apr-2016	2	Datasheet promoted from preliminary data to production data. Minor text changes.
10-Apr-2019	3	Added <a href="#">Section 4.2 DPAK (TO-252) type C2 package information</a> . Minor text changes.

## Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>2</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>3</b>
<b>2.1</b>	Characteristics curves .....	<b>4</b>
<b>3</b>	<b>Test circuits</b> .....	<b>6</b>
<b>4</b>	<b>Package information</b> .....	<b>7</b>
<b>4.1</b>	DPAK package information .....	<b>7</b>
<b>4.2</b>	Packing information .....	<b>9</b>
<b>4.3</b>	DPAK (TO-252) packing information .....	<b>12</b>
	<b>Revision history</b> .....	<b>15</b>



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