

### **STD16NF06**

## N-Channel 60V - 0.060Ω - 16A - DPAK STripFET™ II Power MOSFET

#### **General features**

| Туре      | V <sub>DSS</sub> | R <sub>DS(on)</sub> | I <sub>D</sub> |
|-----------|------------------|---------------------|----------------|
| STD16NF06 | 60V              | <0.070Ω             | 16A            |

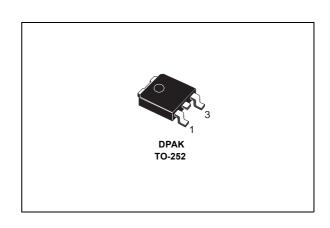
- Typical  $R_{DS(on)} = 0.060\Omega$
- Exceptional dv/dt Capability
- 100% Avalanche Tested
- Application Oriented Characterization

### **Description**

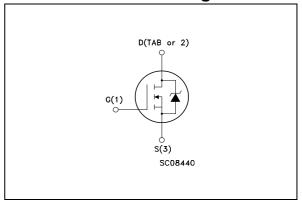
This Power MOSFET is the latest development of STMicroelectronis unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility

## **Applications**

- Audio Amplifiers
- Power Tools
- Automotive Environment



### Internal schematic diagram



#### **Order codes**

| Part Number | Part Number Marking |        | Packaging   |  |
|-------------|---------------------|--------|-------------|--|
| STD16NF06T4 | D16NF06             | TO-252 | TAPE & REEL |  |

Rev 1 January 2006 1/11 1 Electrical ratings STD16NF06

# 1 Electrical ratings

Table 1. Absolute maximum ratings

| Symbol                             | Parameter   | Value      | Unit |
|------------------------------------|---|------------|------|
| V <sub>DS</sub>                    | Drain-source Voltage (V <sub>GS</sub> = 0V)           | 60         | V    |
| V <sub>DGR</sub>                   | Drain-gate Voltage (R <sub>GS</sub> = 20 k $\Omega$ ) | 60         | V    |
| V <sub>GS</sub>                    | Gate-Source Voltage                                   | ± 20       | V    |
| I <sub>D</sub>                     | Drain Current (continuous) at T <sub>C</sub> = 25°C   | 16         | Α    |
| I <sub>D</sub>                     | Drain Current (continuous) at T <sub>C</sub> = 100°C  | 11         | Α    |
| I <sub>DM</sub> Note 4             | Drain Current (pulsed)                                | 64         | Α    |
| P <sub>TOT</sub>                   | Total Dissipation at T <sub>C</sub> = 25°C            | 40         | W    |
|                                    | Derating Factor                                       | 0.27       | W/°C |
| dv/dt                              | Peak Diode Recovery voltage slope                     | 10.5       | V/ns |
| EAS                                | Single Pulse Avalanche Energy                         | 178        | mJ   |
| T <sub>J</sub><br>T <sub>stg</sub> | Operating Junction Temperature Storage Temperature    | -55 to 175 | °C   |

Table 2. Thermal data

| R <sub>thJC</sub> | Thermal Resistance Junction-case Max           | 3.75 | °C/W |
|-------------------|--|------|------|
| R <sub>thJA</sub> | Thermal Resistance Junction-amb Max            | 100  | °C/W |
| T <sub>I</sub>    | Maximum Lead Temperature For Soldering Purpose | 275  | °C   |

STD16NF06 2 Electrical characteristics

## 2 Electrical characteristics

(  $T_{CASE}$  = 25 °C unless otherwise specified )

Table 3. On/off states

| Symbol               | Parameter  | Test Conditions                             |                     | Min. | Тур.  | Max.    | Unit     |
|----------------------|--|---|---------------------|------|-------|---------|----------|
| V <sub>(BR)DSS</sub> | Drain-Source Breakdown<br>Voltage                        | I <sub>D</sub> = 250μA                      | V <sub>GS</sub> = 0 | 60   |       |         | V        |
| I <sub>DSS</sub>     | Zero Gate Voltage Drain<br>Current (V <sub>GS</sub> = 0) | $V_{DS}$ = Max Rating $V_{DS}$ = Max Rating |                     |      |       | 1<br>10 | μA<br>μA |
| I <sub>GSS</sub>     | Gate Body Leakage Current (V <sub>DS</sub> = 0)          | V <sub>GS</sub> = ±20V                      |                     |      |       | ±100    | μA       |
| V <sub>GS(th)</sub>  | Gate Threshold Voltage                                   | $V_{DS} = V_{GS}$                           | $I_{D} = 250 \mu A$ | 2    |       |         | V        |
| R <sub>DS(on)</sub>  | Static Drain-Source On<br>Resistance                     | V <sub>GS</sub> = 10V                       | I <sub>D</sub> = 8A |      | 0.060 | 0.070   | Ω        |

#### Table 4. Dynamic

| Symbol   | Parameter   | Test Conditions  | Min. | Тур.               | Max. | Unit           |
|--|---|--|------|--------------------|------|----------------|
| g <sub>fs</sub> Note 5                                   | Forward Transconductance  | V <sub>DS</sub> = 25V I <sub>D</sub> = 8A                      |      | 6                  |      | S              |
| C <sub>iss</sub><br>C <sub>oss</sub><br>C <sub>rss</sub> | Input Capacitance Output Capacitance Reverse Transfer Capacitance | V <sub>DS</sub> = 15V, f = 1MHz, V <sub>GS</sub> = 0           |      | 400<br>103<br>41.5 |      | pF<br>pF<br>pF |
| Q <sub>g</sub><br>Q <sub>gs</sub><br>Q <sub>gd</sub>     | Total Gate Charge<br>Gate-Source Charge<br>Gate-Drain Charge      | $V_{DD}$ = 30 $I_{D}$ = 16A $V_{GS}$ = 10V Figure 14 on page 7 |      | 14.1<br>2.8<br>5.4 |      | nC<br>nC<br>nC |

Table 5. Switching times

| Symbol                               | Parameter                         | Test Conditions   | Min. | Тур.      | Max. | Unit     |
|--------------------------------------|-----------------------------------|---|------|-----------|------|----------|
| t <sub>d(on)</sub><br>t <sub>r</sub> | Turn-on Delay Time<br>Rise Time   | $V_{DD}$ = 30V, $I_D$ = 8A,<br>$R_G$ = 4.7 $\Omega$ , $V_{GS}$ = 10V<br>Figure 13 on page 7     |      | 4<br>15   |      | ns<br>ns |
| t <sub>d(off)</sub>                  | Off voltage Rise Time<br>FallTime | $V_{DD}$ = 30V, $I_{D}$ = 8A,<br>$R_{G}$ = 4.7 $\Omega$ , $V_{GS}$ = 10V<br>Figure 15 on page 7 |      | 16<br>5.5 |      | ns<br>ns |

**577** 

2 Electrical characteristics STD16NF06

Table 6. Source drain diode

| Symbol   | Parameter  | Test Conditions   | Min. | Тур.            | Max.     | Unit          |
|--|--|---|------|-----------------|----------|---------------|
| I <sub>SD</sub><br>I <sub>SDM</sub> Note 4             | Source-drain Current<br>Source-drain Current (pulsed)                        |   |      |                 | 16<br>64 | A<br>A        |
| V <sub>SD</sub> Note 5                                 | Forward on Voltage   | $I_{SD} = 8A$ $V_{GS} = 0$  |      |                 | 1.5      | V             |
| t <sub>rr</sub><br>Q <sub>rr</sub><br>I <sub>RRM</sub> | Reverse Recovery Time<br>Reverse Recovery Charge<br>Reverse Recovery Current | $I_{SD}$ = 16A, di/dt = 100A/µs,<br>$V_{DD}$ = 20V, $T_{J}$ =150°C<br>Figure 15 on page 7 |      | 49<br>78<br>3.2 |          | ns<br>μC<br>A |

Note: 1 Value limited by wire bonding

2 Garanted when external Rg=4.7  $\Omega$  and  $t_{\text{f}}$  <  $t_{\text{fmax}}.$ 

- 3 Starting  $T_J = 25$ °C,  $I_D = 19A$ ,  $V_{DD} = 18V$
- 4 Pulse width limited by safe operating area
- 5 Pulsed: pulse duration = 300µs, duty cycle 1.5%

STD16NF06 2 Electrical characteristics

### 2.1 Electrical chraracteristics (curves)

Figure 1. Safe Operating Area

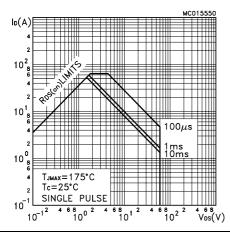


Figure 2. Thermal Impedance

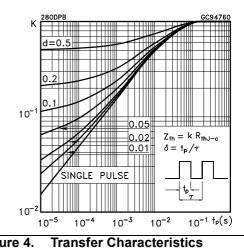
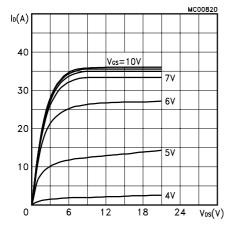


Figure 3. Output Characteristics

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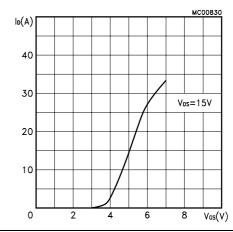
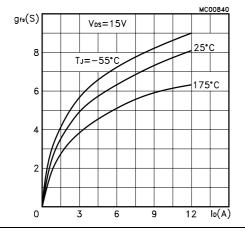
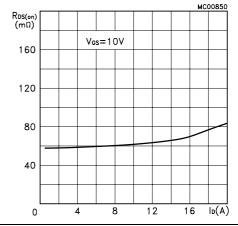


Figure 5. Transconductance

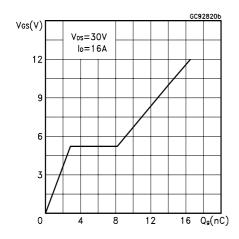
Figure 6. Static Drain-Source on Resistance





2 Electrical characteristics STD16NF06

Figure 7. Gate Charge vs Gate-Source Voltage Figure 8. Capacitance Variations



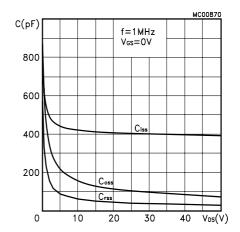
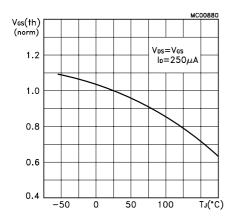


Figure 9. Normalized Gate Threshold Voltage Figure 10. Normalized on Resistance vs vs Temperature Temperature



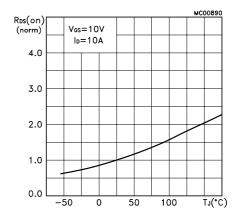
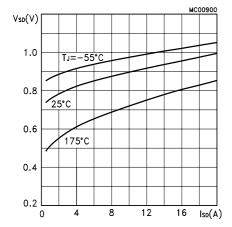
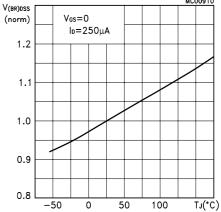


Figure 11. Source-drain Diode Forward Characteristics

Figure 12. Normalized Breakdown Voltage vs Temperature



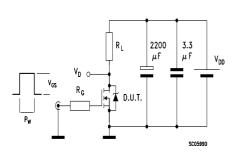


STD16NF06 3 Test circuits

### 3 Test circuits

Figure 13. Switching Times Test Circuit For Resistive Load

Figure 14. Gate Charge Test Circuit



V<sub>1</sub> = 20V = V<sub>GMAX</sub>

V<sub>1</sub> = 20V = V<sub>GMAX</sub>

1<sub>G</sub> = CONST

100 Ω

V<sub>G</sub>

1KΩ

V<sub>G</sub>

1KΩ

V<sub>G</sub>

1KΩ

V<sub>G</sub>

1KΩ

V<sub>G</sub>

1KΩ

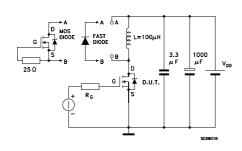
V<sub>G</sub>

100 Ω

1

Figure 15. Test Circuit For Inductive Load Switching and Diode Recovery Times

Figure 17. Unclamped Inductive Load Test Circuit



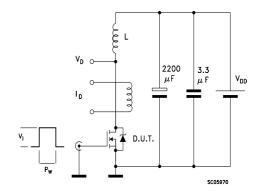
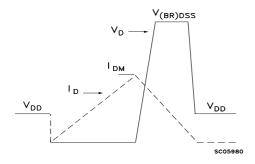


Figure 16. Unclamped Inductive Waveform

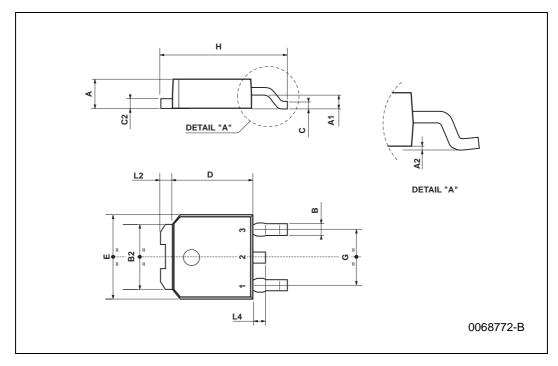


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: <a href="https://www.st.com">www.st.com</a>

### **TO-252 (DPAK) MECHANICAL DATA**

| DIM.   |      | mm   |      |       | inch  |       |
|--------|------|------|------|-------|-------|-------|
| Dilli. | MIN. | TYP. | MAX. | MIN.  | TYP.  | MAX.  |
| Α      | 2.2  |      | 2.4  | 0.086 |       | 0.094 |
| A1     | 0.9  |      | 1.1  | 0.035 |       | 0.043 |
| A2     | 0.03 |      | 0.23 | 0.001 |       | 0.009 |
| В      | 0.64 |      | 0.9  | 0.025 |       | 0.035 |
| B2     | 5.2  |      | 5.4  | 0.204 |       | 0.212 |
| С      | 0.45 | _    | 0.6  | 0.017 |       | 0.023 |
| C2     | 0.48 |      | 0.6  | 0.019 |       | 0.023 |
| D      | 6    |      | 6.2  | 0.236 |       | 0.244 |
| Е      | 6.4  |      | 6.6  | 0.252 |       | 0.260 |
| G      | 4.4  |      | 4.6  | 0.173 |       | 0.181 |
| Н      | 9.35 |      | 10.1 | 0.368 |       | 0.397 |
| L2     |      | 0.8  |      |       | 0.031 |       |
| L4     | 0.6  |      | 1    | 0.023 |       | 0.039 |



**5**//

5 Revision History STD16NF06

# 5 Revision History

| Date        | Revision | Description of changes |
|-------------|----------|------------------------|
| 10-Jan-2006 | 1        | First release          |

**STD16NF06** 5 Revision History

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