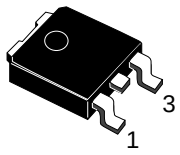
STD1703L

N-CHANNEL 30V - 0.038Ω - 17A - DPAK
STripFET™ II MOSFET

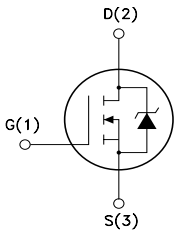
TYPE	V_{DSS}	$R_{DS(on)}$	I_D
STD1703L	30 V	<0.05 Ω	17 A

- TYPICAL $R_{DS}(on)$ = 0.038 Ω
- APPLICATION ORIENTED CHARACTERIZATION



DPAK

INTERNAL SCHEMATIC DIAGRAM



DESCRIPTION

This MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalance characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

APPLICATIONS

- DC-DC CONVERTERS
- LINEAR POST REGULATION

ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STD1703LT4	D1703L	DPAK	TAPE & REEL

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source Voltage (V_{GS} = 0)	30	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20 kΩ)	30	V
V_{GS}	Gate- source Voltage	± 20	V
I_D	Drain Current (continuous) at T_C = 25°C	17	A
I_D	Drain Current (continuous) at T_C = 100°C	12	A
I_{DM} (●)	Drain Current (pulsed)	68	A
P_{TOT}	Total Dissipation at T_C = 25°C	20	W
	Derating Factor	0.13	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	6	V/ns
E_{AS} (2)	Single Pulse Avalanche Energy	200	mJ
T_{stg}	Storage Temperature	–65 to 175	°C
T_j	Max. Operating Junction Temperature	175	°C

(●) Pulse width limited by safe operating area
(1) I_{SD} ≤17A, di/dt ≤300A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_j ≤ $T_{JMAX.}$
(2) Starting T_j=25°C, I_D=11A, V_{DD}=15V

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case Max	7.5	°C/W
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5	°C/W
T_l	Maximum Lead Temperature For Soldering Purpose	275	°C

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	I_D= 250 µA, V_{GS}= 0	30			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS}= Max Rating			1	µA
		V_{DS}= Max Rating, T_C= 125°C			10	µA
I_{GSS}	Gate-body Leakage Current (V_{DS} = 0)	V_{GS} = ± 15V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250µA	1			V
$R_{DS(on)}$	Static Drain-source On Resistance	V_{GS} = 10V, I_D = 8.5 A		0.038	0.05	Ω
		V_{GS} = 5 V, I_D = 8.5 A		0.045	0.06	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$, I_D =11A		7		S
C_{iss}	Input Capacitance	V_{DS}= 25V, f= 1 MHz, V_{GS}= 0		330		pF
C_{oss}	Output Capacitance			90		pF
C_{rss}	Reverse Transfer Capacitance			40		pF

ELECTRICAL CHARACTERISTICS (CONTINUED)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	V_{DD} = 15V, I_D = 8.5A		11		ns
t_r	Rise Time	R_G = 4.7Ω V_{GS} = 4.5V (see test circuit, Figure 3)		100		ns
Q_g	Total Gate Charge	V_{DD} = 24V, I_D = 17A, V_{GS} = 10V		6.5	9	nC
Q_{gs}	Gate-Source Charge			3.6		nC
Q_{gd}	Gate-Drain Charge			2		nC

SWITCHING OFF

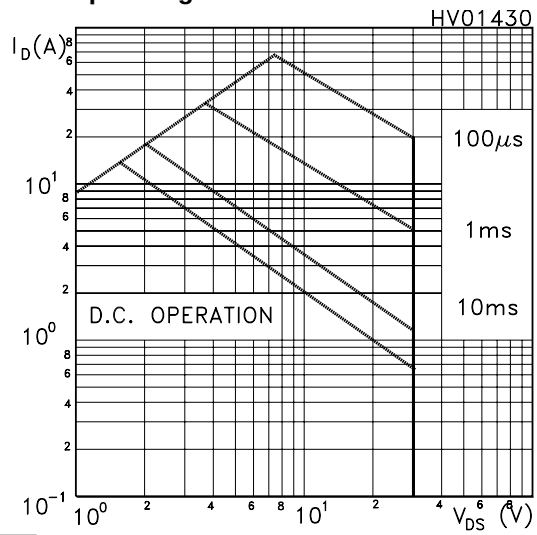
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off-Delay Time	V_{DD} = 15V, I_D = 8.5A,		25		ns
t_f	Fall Time	R_G = 4.7Ω, V_{GS} = 4.5V (see test circuit, Figure 3)		22		ns
$t_{r(off)}$	Off-voltage Rise Time	Vclamp =24V, I_D =17A		22		ns
t_f	Fall Time	R_G = 4.7Ω, V_{GS} = 4.5V		55		ns
t_c	Cross-over Time	(see test circuit, Figure 5)		75		ns

SOURCE DRAIN DIODE

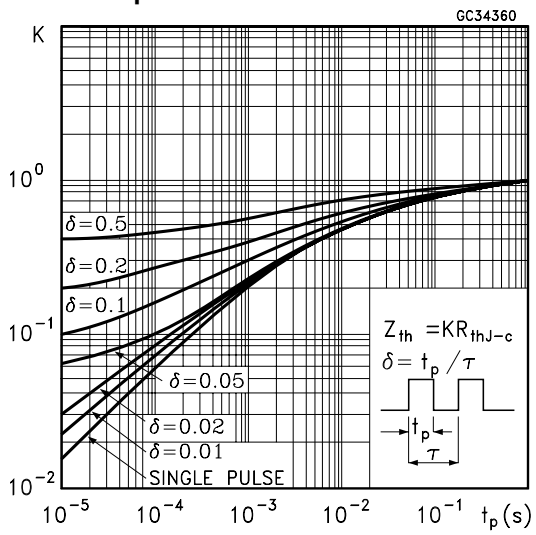
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				17	A
I_{SDM} (1)	Source-drain Current (pulsed)				68	A
V_{SD} (2)	Forward On Voltage	I_{SD} = 17A, V_{GS} = 0			1.5	V
t_{rr}	Reverse Recovery Time	I_{SD} = 17A, di/dt = 100A/µs,		30		ns
Q_{rr}	Reverse Recovery Charge	V_{DD} = 15V, T_j = 150°C		18		nC
I_{RRM}	Reverse Recovery Current	(see test circuit, Figure 5)		1.2		A

Note: 1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

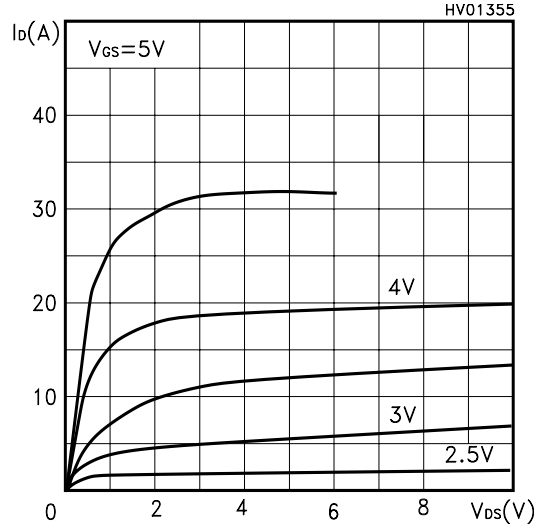
Safe Operating Area



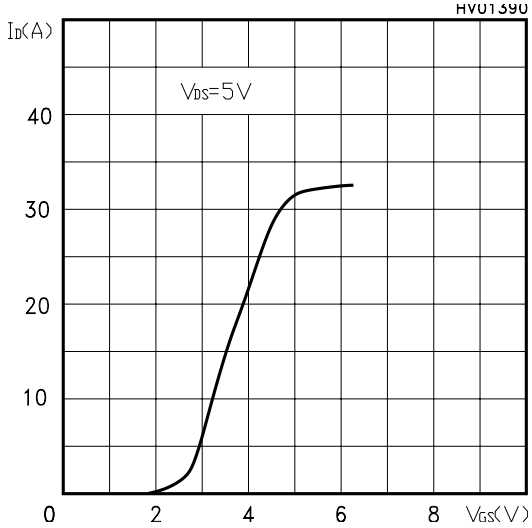
Thermal Impedence



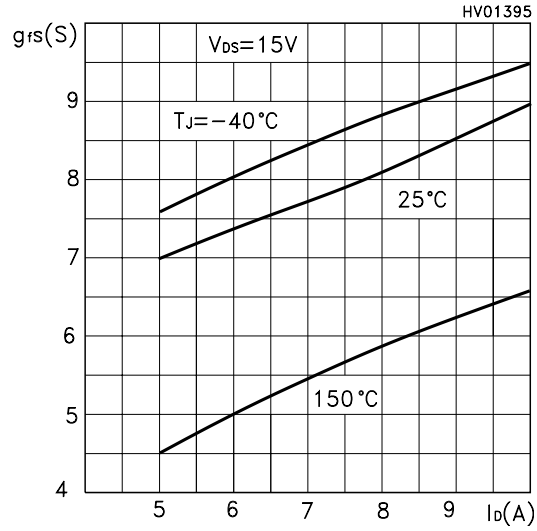
Output Characteristics



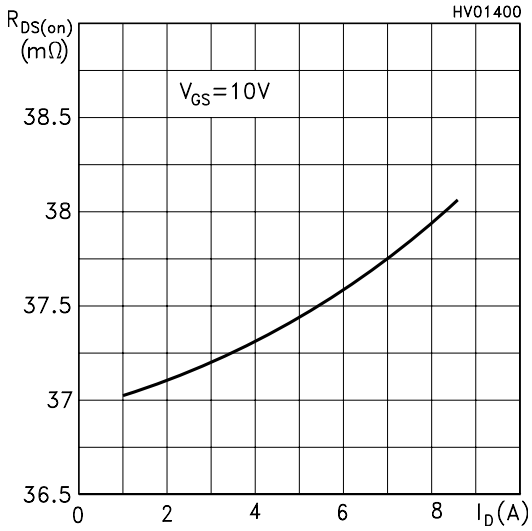
Transfer Characteristics



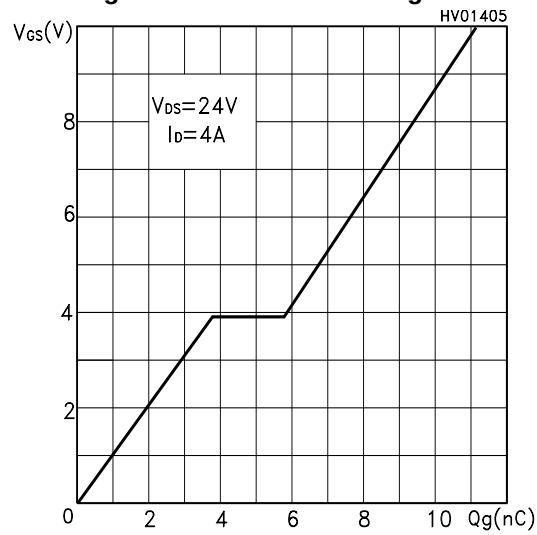
Transconductance



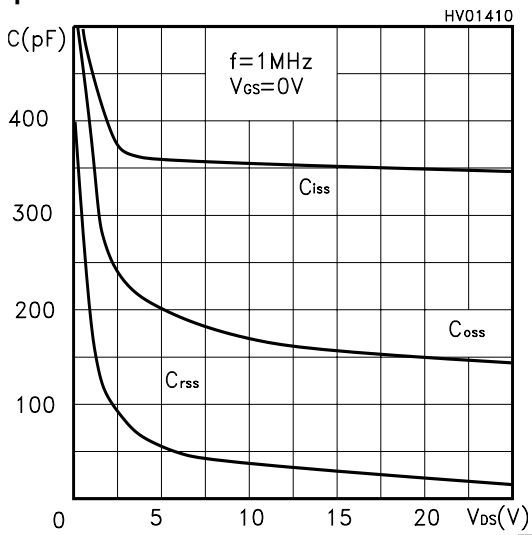
Static Drain-source On Resistance



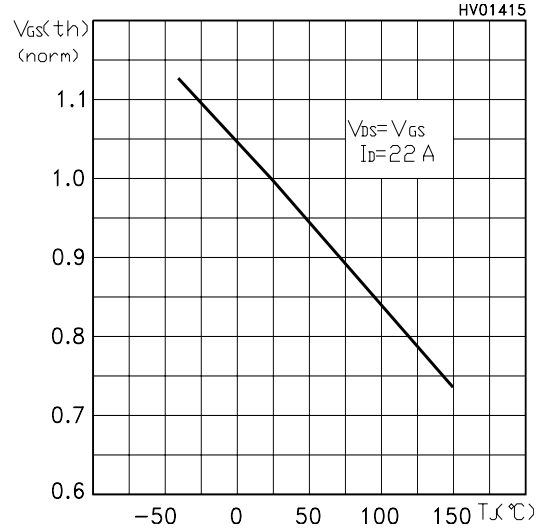
Gate Charge vs Gate-source Voltage



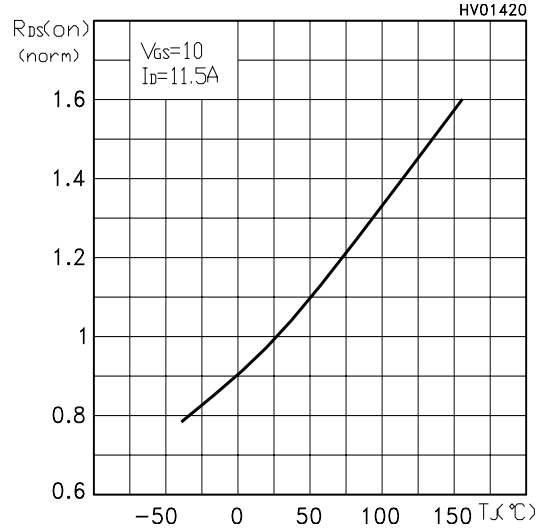
Capacitance Variations



Normalized Gate Thereshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

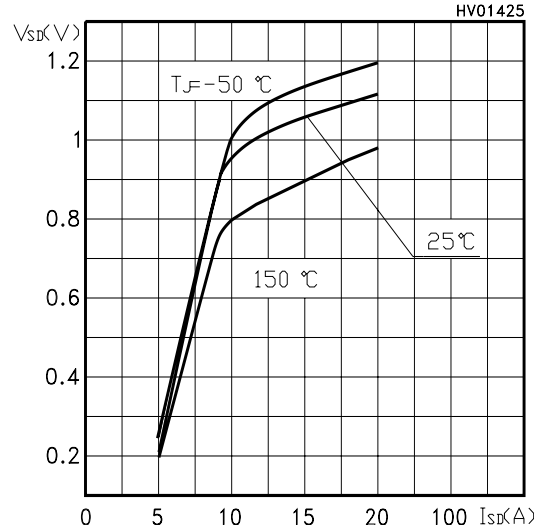


Fig. 1: Unclamped Inductive Load Test Circuit

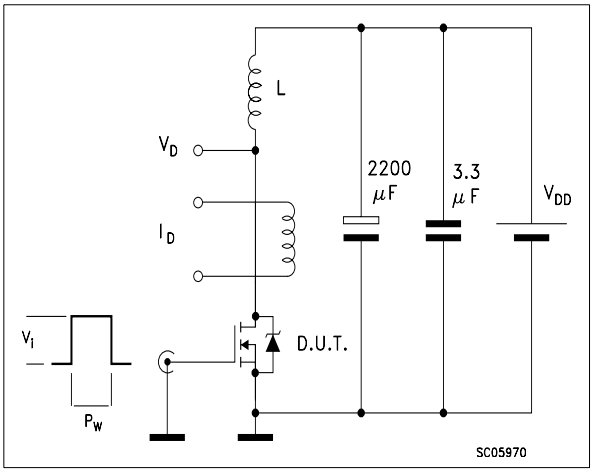


Fig. 2: Unclamped Inductive Waveform

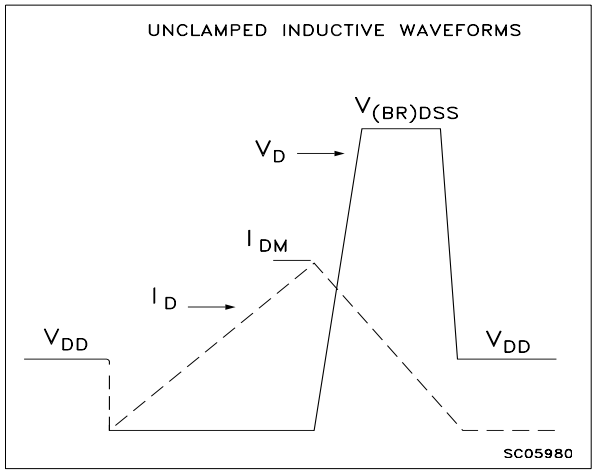


Fig. 3: Switching Times Test Circuit For Resistive Load

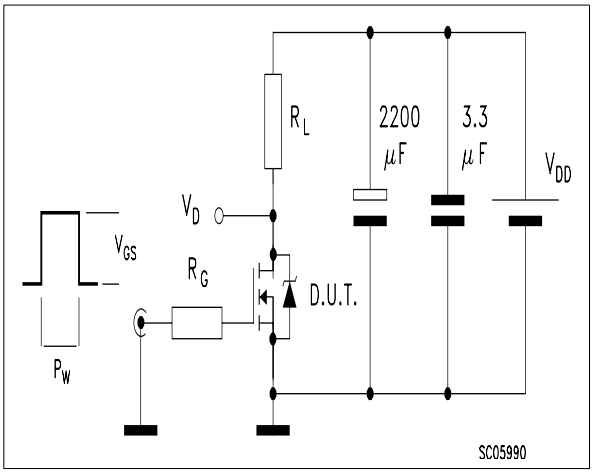


Fig. 4: Gate Charge test Circuit

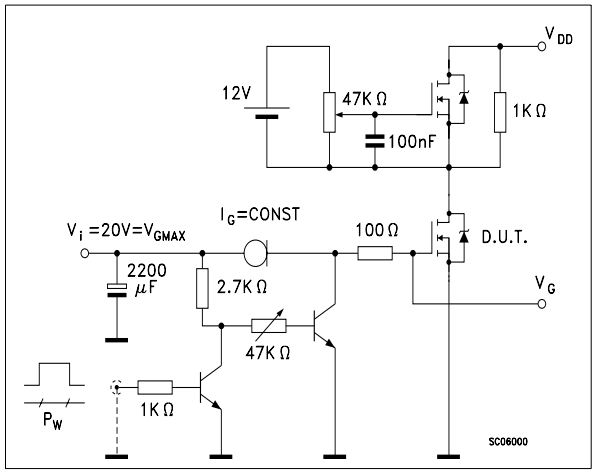
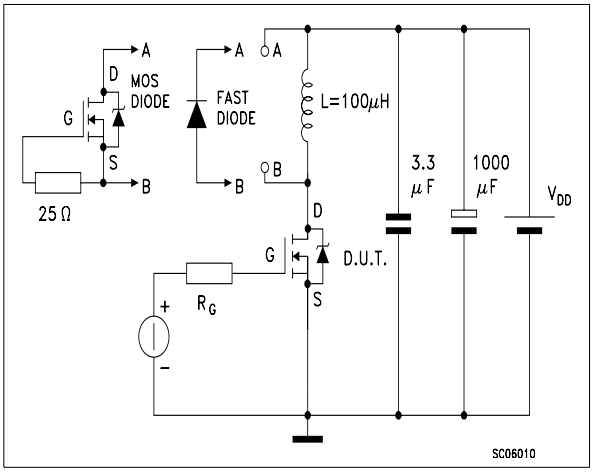
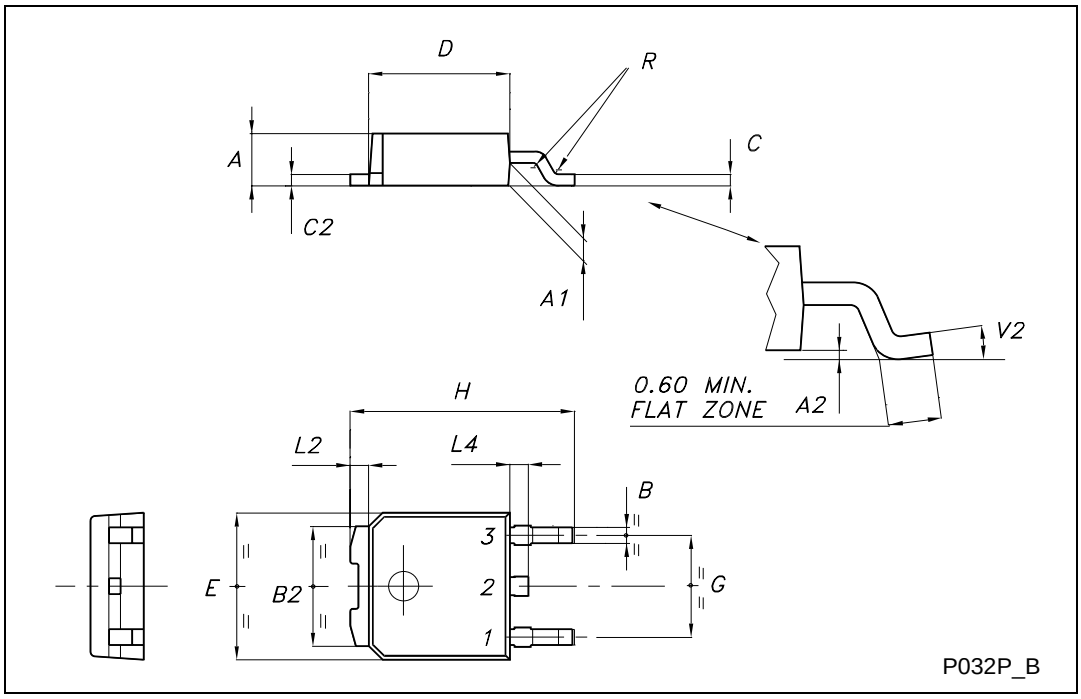


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



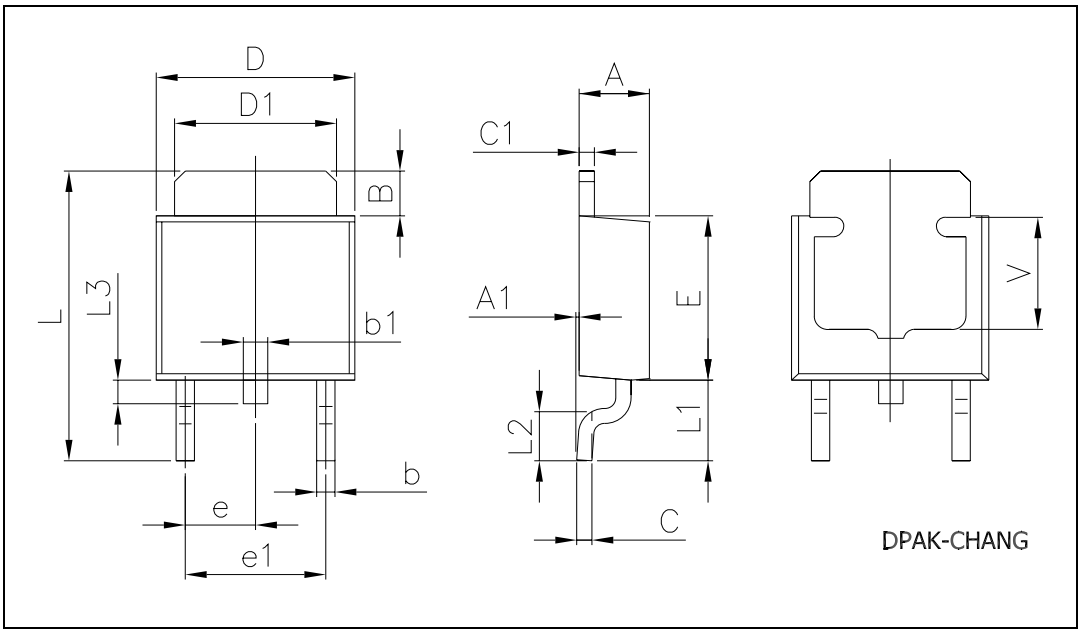
TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0^o		8^o	0^o		0^o



TO-252 (DPAK) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.00		0.127	0.00		0.005
B	1.350		1.650	0.053		0.065
b	0.50		0.70	0.020		0.028
b1	0.70		0.90	0.028		0.035
c	0.430		0.580	0.017		0.023
c1	0.430		0.580	0.017		0.023
D	6.350		6.650	0.250		0.262
D1	5.20		5.40	0.205		0.213
E	5.40		5.70	0.213		0.224
e		2.30			0.091	
e1	4.50		4.70	0.177		0.185
L	9.50		9.90	0.374		0.390
L1	2.550		2.900	0.10		0.114
L2	1.40		1.780	0.055		0.070
L3	0.35		0.65	0.014		0.026
V	3.80 REF			0.150 REF		



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