

Automotive-grade P-channel -30 V, 33 mΩ typ., -20 A STripFET™ F6 Power MOSFET in a DPAK package

Datasheet - production data

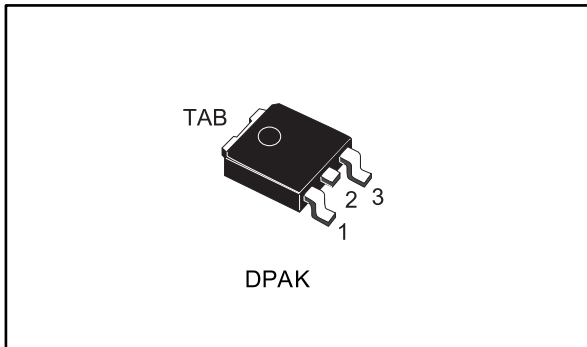
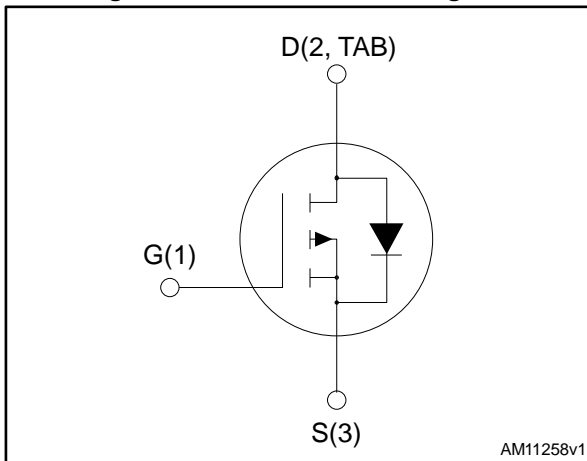


Figure 1: Internal schematic diagram



Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STD20P3H6AG	-30 V	50 mΩ	-20 A

- Designed for automotive applications and AEC-Q101 qualified
- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the STripFET™ F6 technology, with a new trench gate structure. The resulting Power MOSFET exhibits very low R_{DS(on)} in all packages.

Table 1: Device summary

Order code	Marking	Package	Packing
STD20P3H6AG	20P3H6	DPAK	Tape and reel

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	-30	V
V_{GS}	Gate-source voltage	± 20 V	V
I_D	Drain current (continuous) at $T_{case} = 25\text{ °C}$	-20	A
	Drain current (continuous) at $T_{case} = 100\text{ °C}$	-14	
$I_{DM}^{(1)}$	Drain current (pulsed)	-80	A
P_{TOT}	Total dissipation at $T_{case} = 25\text{ °C}$	40	W
$E_{AS}^{(2)}$	Single pulse avalanche energy	250	mJ
T_{stg}	Storage temperature	-55 to 175	°C
T_j	Operating junction temperature		

Notes:

⁽¹⁾ Pulse width is limited by safe operating area.

⁽²⁾ starting $T_j = 25\text{ °C}$, $R_G = 47\ \Omega$, $I_{D(min)} = -20\text{ A}$.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	3.75	°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	50	

Notes:

⁽¹⁾ When mounted on a 1-inch² FR-4, 2 Oz copper board

2 Electrical characteristics

($T_{\text{case}} = 25\text{ °C}$ unless otherwise specified)

Table 4: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = -250\text{ }\mu\text{A}$	-30			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = -30\text{ V}$			-1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = -30\text{ V}$, $T_{\text{case}} = 125\text{ °C}$			-10	
I_{GSS}	Gate-body leakage current	$V_{DS} = 0\text{ V}$, $V_{GS} = -20\text{ V}$			-100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = -250\text{ }\mu\text{A}$	-2		-4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = -10\text{ V}$, $I_D = -10\text{ A}$		33	50	m Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = -25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	635	-	μF
C_{oss}	Output capacitance		-	155	-	
C_{rss}	Reverse transfer capacitance		-	100	-	
Q_g	Total gate charge	$V_{DD} = -15\text{ V}$, $I_D = -20\text{ A}$, $V_{GS} = -10\text{ V}$ (see Figure 14: "Gate charge test circuit")	-	12.8	-	nC
Q_{gs}	Gate-source charge		-	4.4	-	
Q_{gd}	Gate-drain charge		-	3.4	-	

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = -15\text{ V}$, $I_D = -10\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = -10\text{ V}$ (see Figure 13: "Switching times test circuit for resistive load")	-	9.4	-	ns
t_r	Rise time		-	28.2	-	
$t_{d(off)}$	Turn-off delay time		-	15.8	-	
t_f	Fall time		-	6.25	-	

Table 7: Source-drain diode

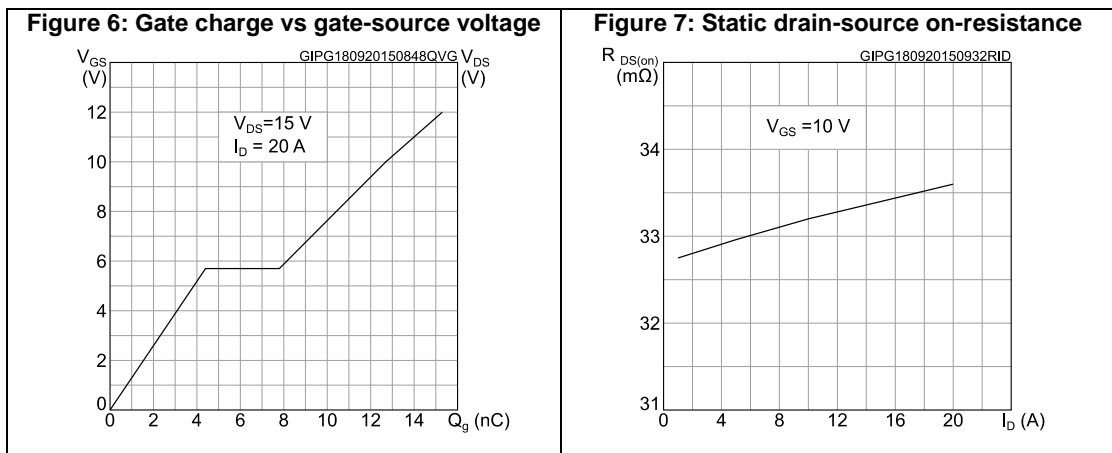
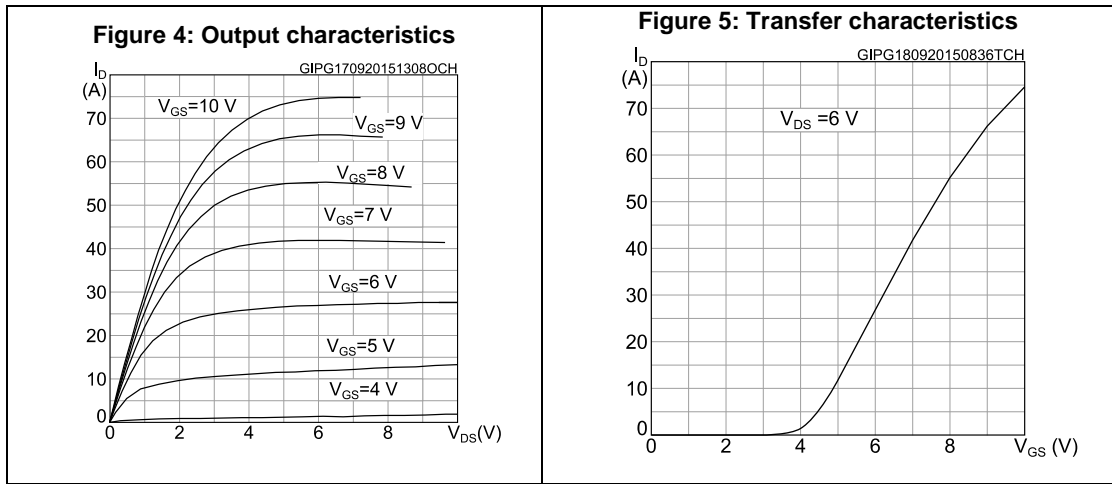
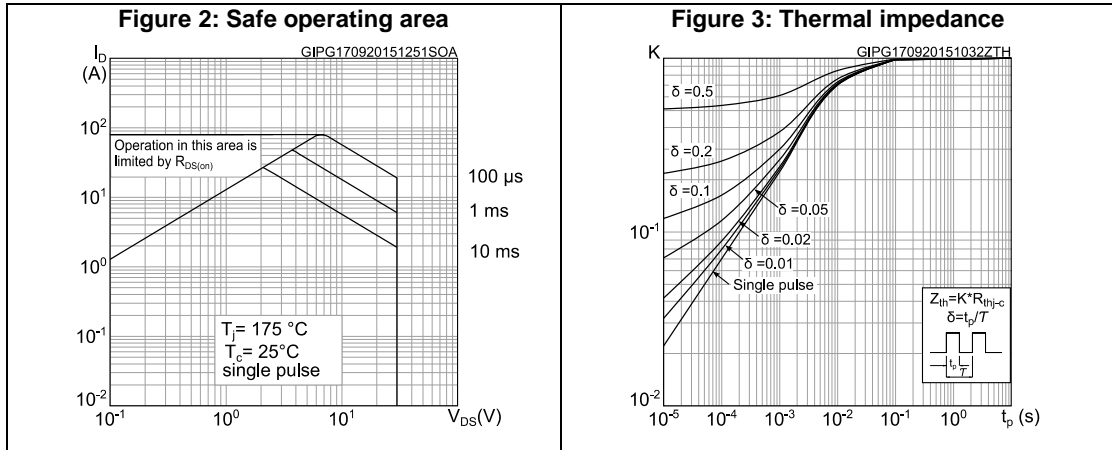
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		-20	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		-80	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = -20\text{ A}$	-		-1.3	V
t_{rr}	Reverse recovery time	$I_{SD} = -20\text{ A}$, $di/dt = -100\text{ A}/\mu\text{s}$, $V_{DD} = -24\text{ V}$ (see Figure 15: "Test circuit for inductive load switching and diode recovery times")	-	18.4		ns
Q_{rr}	Reverse recovery charge		-	11.2		nC
I_{RRM}	Reverse recovery current		-	-1.2		A

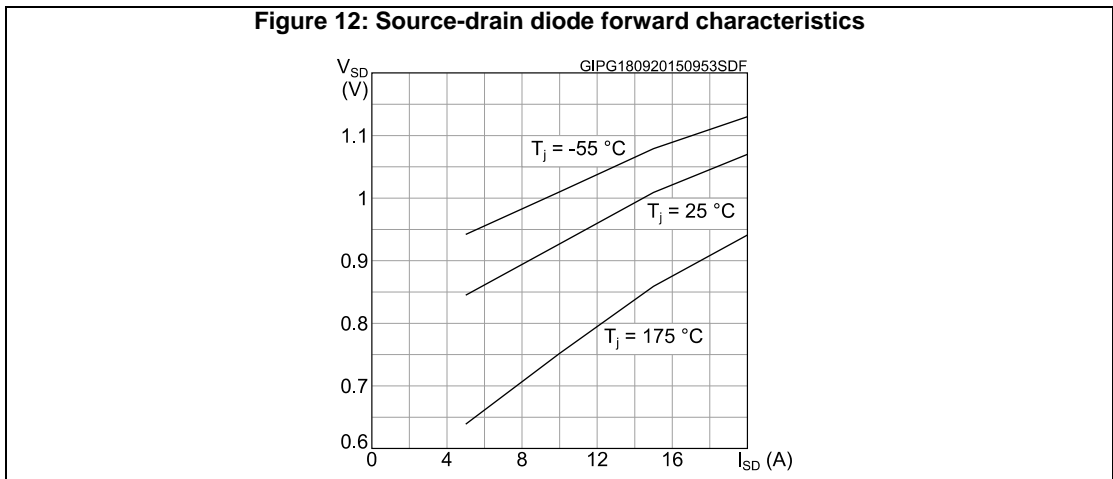
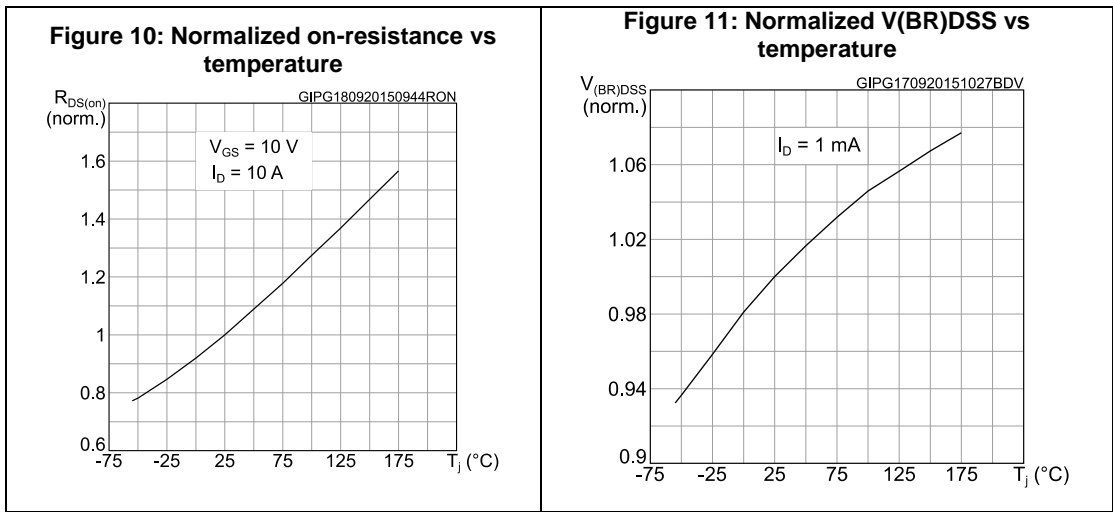
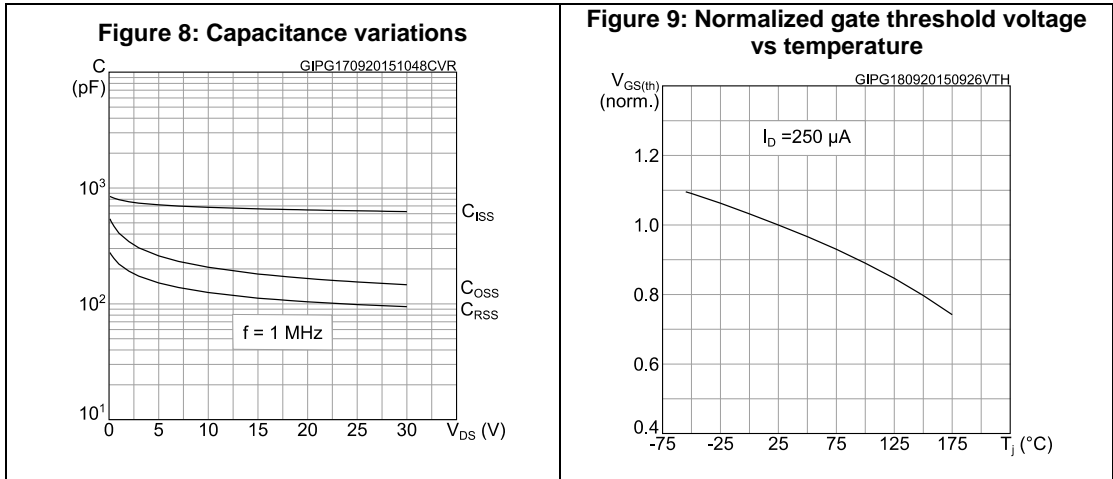
Notes:

(1) Pulse width is limited by safe operating area.

(2) Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.2 Electrical characteristics (curves)





For the P-channel Power MOSFET, current and voltage polarities are reversed.

3 Test circuits

Figure 13: Switching times test circuit for resistive load

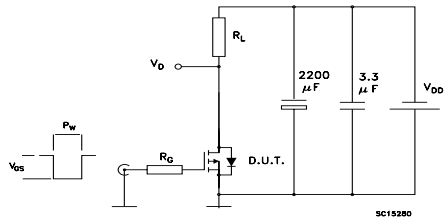


Figure 14: Gate charge test circuit

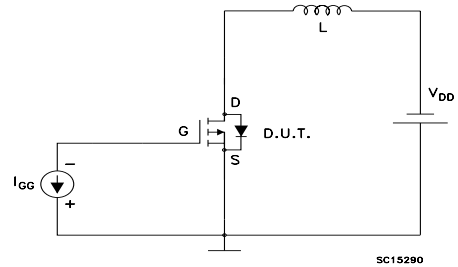
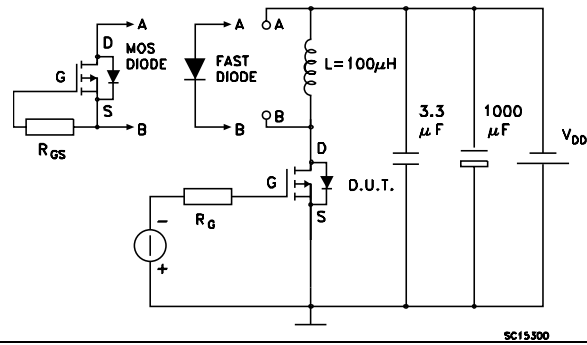


Figure 15: Test circuit for inductive load switching and diode recovery times



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A package information

Figure 16: DPAK (TO-252) type A package outline

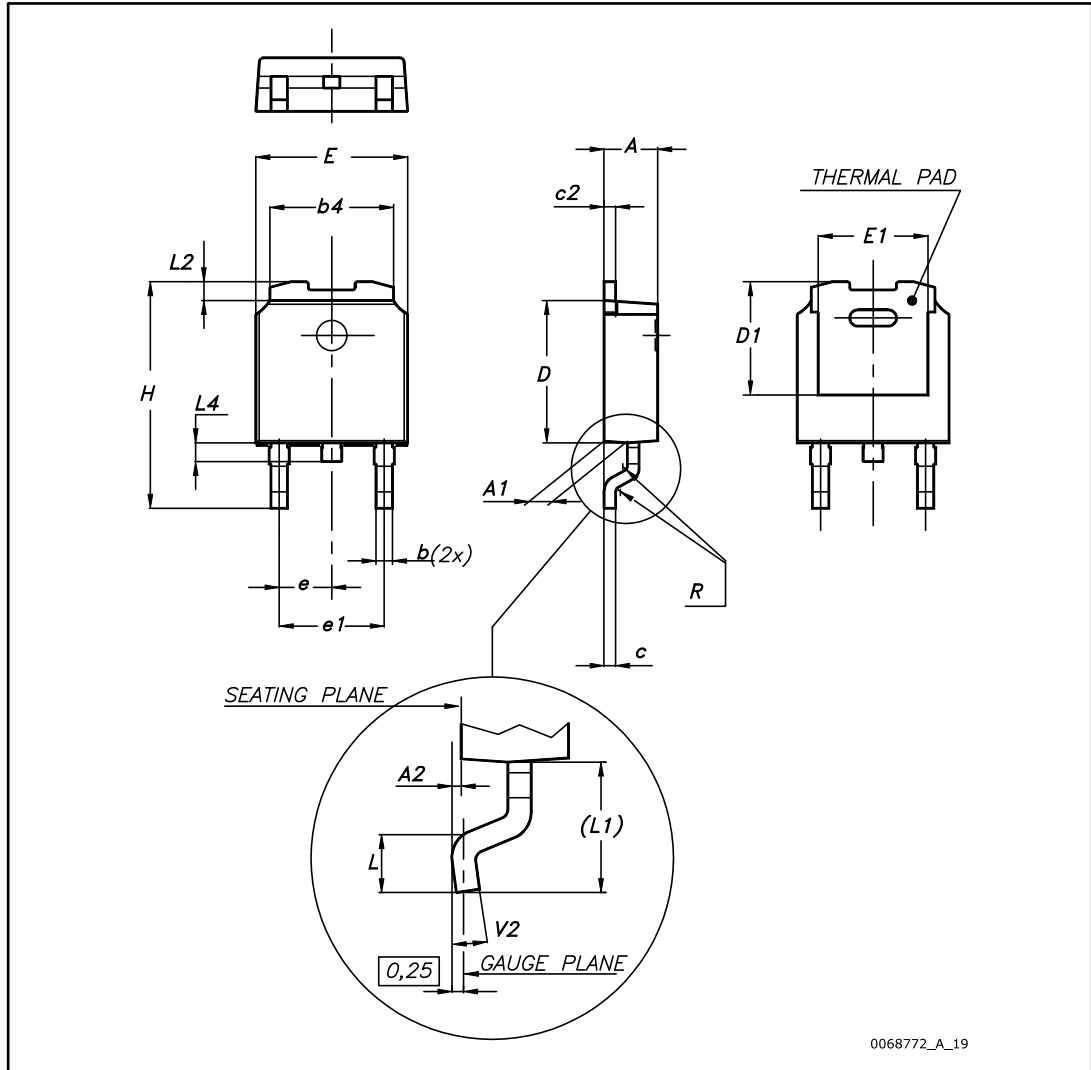
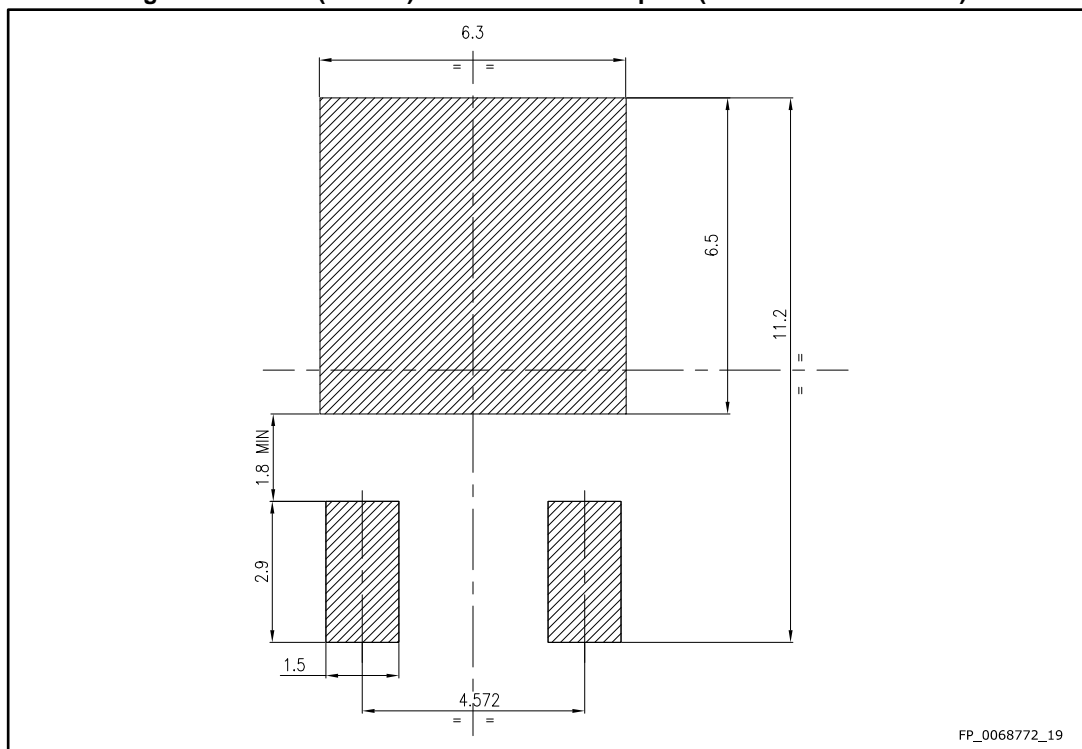


Table 8: DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 17: DPAK (TO-252) recommended footprint (dimensions are in mm)



4.2 DPAK (TO-252) packing information

Figure 18: DPAK (TO-252) tape outline

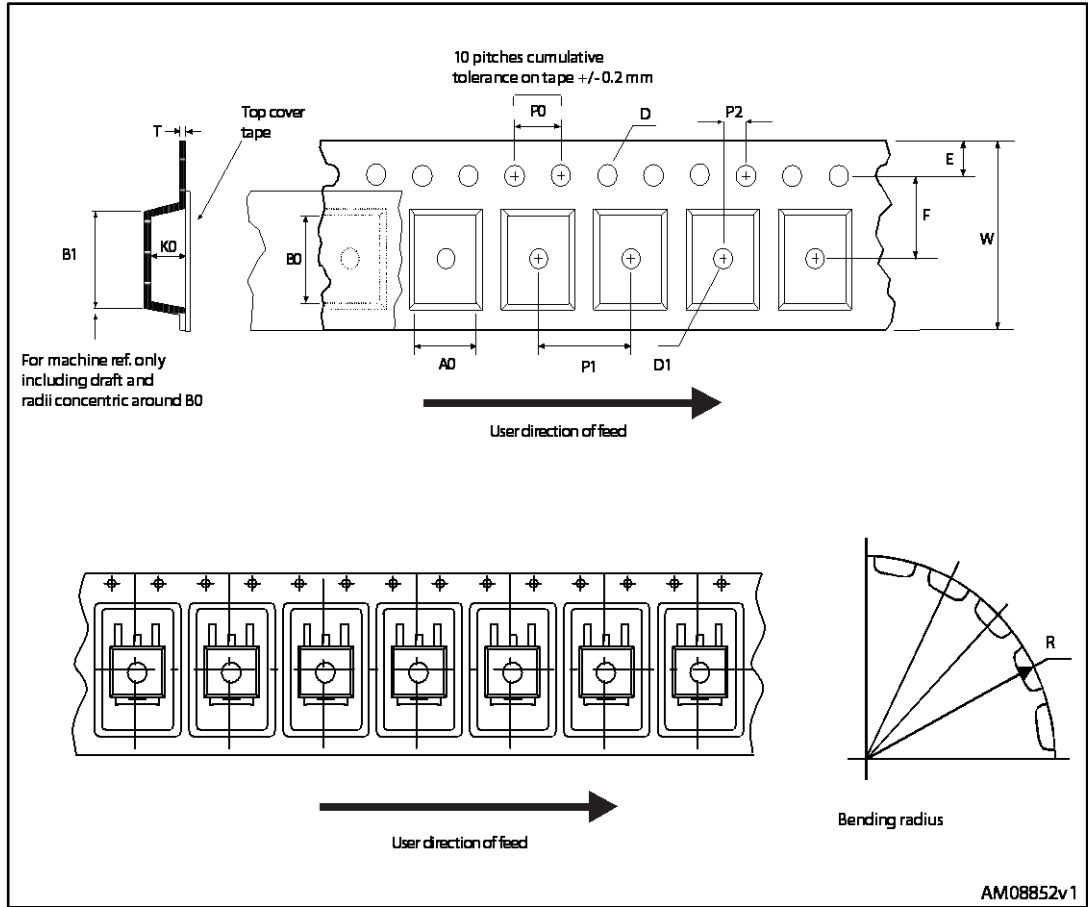


Figure 19: DPAK (TO-252) reel outline

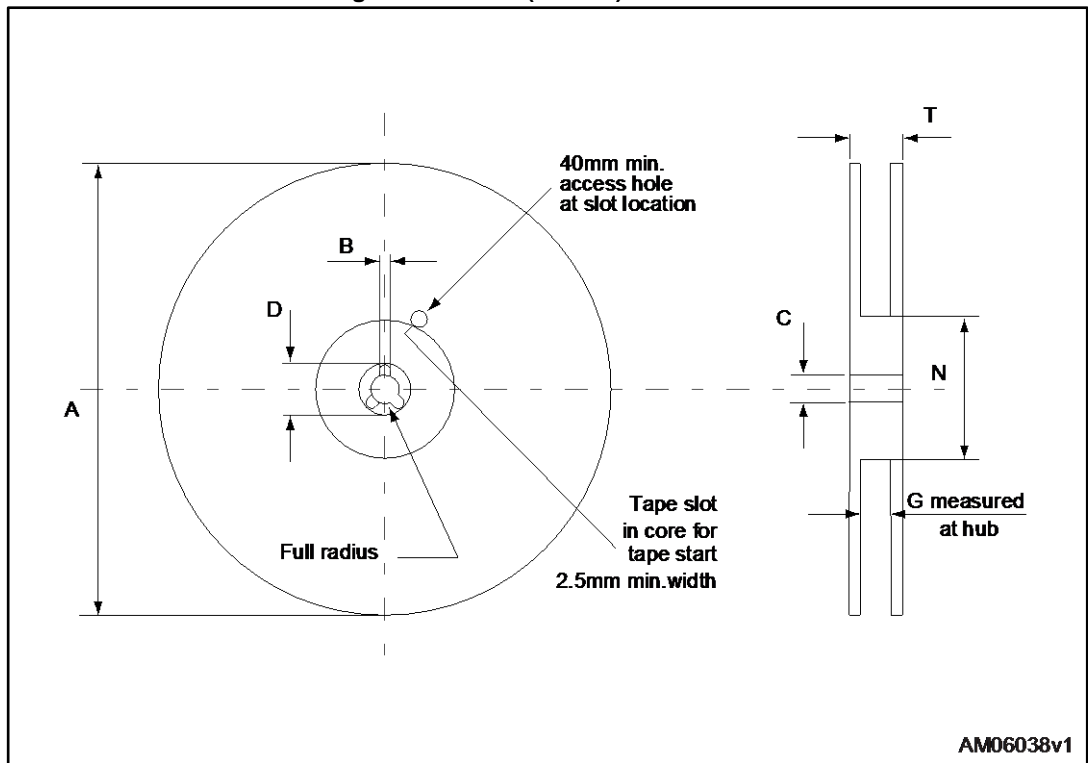


Table 9: DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
18-Sep-2015	1	First release.

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