STD22NF06AG

Automotive-grade N-channel 60 V, 32 mΩ typ., 24 A STripFET™ II Power MOSFET in a DPAK package

Datasheet - production data

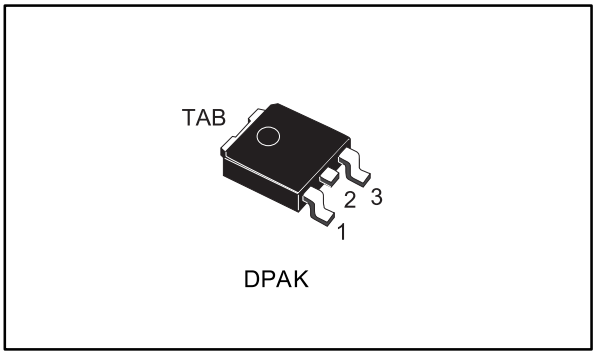
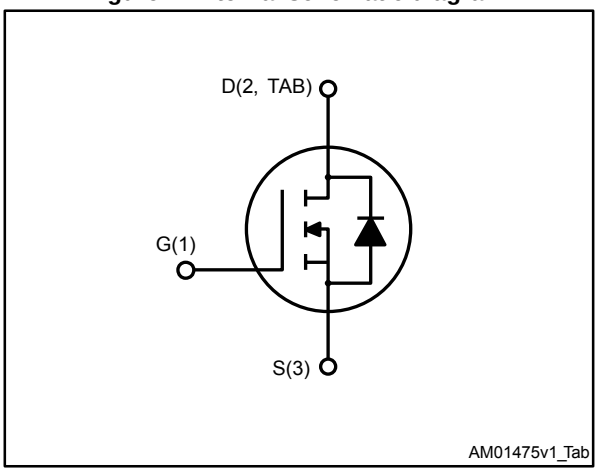


Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STD22NF06AG	60 V	40 mΩ	24 A

- AEC-Q101 qualified
- Exceptional dv/dt capability
- 100% avalanche tested
- Low gate charge

Applications

- Switching applications

Description

This Power MOSFET has been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

Table 1: Device summary

Order code	Marking	Package	Packing
STD22NF06AG	D22NF06	DPAK	Tape and reel

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 kΩ)	60	V
V_{GS}	Gate- source voltage	±20	V
I_D	Drain current (continuous) at T_C = 25°C	24	A
I_D	Drain current (continuous) at T_C=100°C	17	A
I_{DM} (1)	Drain current (pulsed)	96	A
P_{TOT}	Total dissipation at T_C = 25°C	60	W
dv/dt(2)	Peak diode recovery voltage slope	10	V/ns
E_{AS} (3)	Single pulse avalanche energy	300	mJ
T_j	Operating junction temperature range	- 55 to 175	°C
T_{stg}	Storage temperature range		

Notes:

(1)Pulse width limited by safe operating area.

(2)I_{SD} ≤ 24A, di/dt ≤100A/µs, V_{DD} =$V_{(BR)DSS}$, Tj ≤ T_{JMAX}

(3)Starting Tj = 25 °C, I_D = 10 A, V_{DD} = 45 V.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	2.5	°C/W
$R_{thj\text{-}pcb}$ (1)	Thermal resistance junction-pcb	50	°C/W

Notes:

(1)When mounted on a 1-inch² FR-4 board, 2oz Cu.

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4: On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0, I_D = 250 µA	60			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 60 V, V_{GS} = 0			1	µA
		V_{DS} = 60 V, V_{GS} = 0 T_C = 125°C(1)			10	µA
I_{GSS}	Gate body leakage current(V_{DS} = 0)	V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D= 12 A		32	40	mΩ

Notes:

(1)Defined by design,not subject to production test

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs}(1)	Forward transconductance	V_{DS} = 25 V, I_D = 12 A	-	15	-	S
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	690		pF
C_{oss}	Output capacitance		-	170	-	pF
C_{rss}	Reverse transfer capacitance		-	68	-	pF
$t_{d(on)}$	Turn-on delay time	V_{DD} = 30 V, I_D = 10 A R_G = 4.7 Ω V_{GS} = 10 V (see *Figure 14: "Test circuit for resistive load switching times"*)	-	10		ns
t_r	Rise time		-	30		ns
$t_{d(off)}$	Turn-off delay time		-	30		ns
t_f	Fall time		-	8		ns
Q_g	Total gate charge	V_{DD} = 30 V, I_D = 20 A, V_{GS} = 10 V, R_G= 4.7 Ω (see *Figure 15: "Test circuit for gate charge behavior"*)	-	23	31	nC
Q_{gs}	Gate-source charge		-	5	-	nC
Q_{gd}	Gate-drain charge		-	7.5	-	nC

Notes:

(1)Pulsed: Pulse duration = 300 µs, duty cycle 1.5%.

Table 6: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		24	A
I_{SDM}(1)	Source-drain current (pulsed)				96	A
V_{SD}(2)	Forward on voltage	I_{SD} = 24 A, V_{GS} = 0 V			1.5	V
t_r	Reverse recovery time	I_{SD} = 20 A, di/dt = 100 A/µs V_{DD} = 30 V, T_j = 150 °C (see *Figure 16: "Test circuit for inductive load switching and diode recovery times"*)	-	65	-	ns
$t_{d(off)}$	Reverse recovery charge		-	150	-	nC
t_f	Reverse recovery current		-	4.6	-	A

Notes:

(1)Pulse width limited by safe operating area.

(2)Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

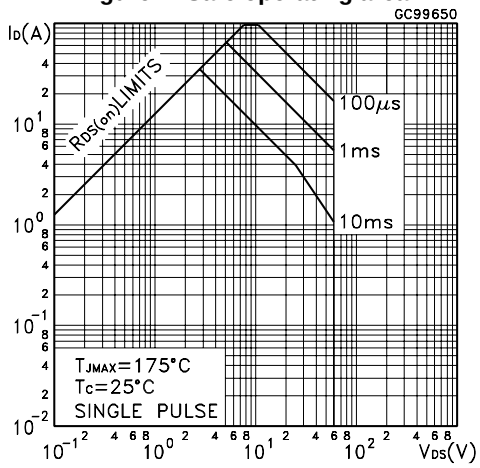


Figure 3: Thermal impedance

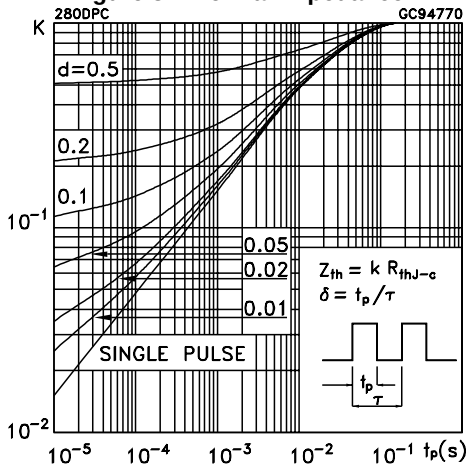


Figure 4: Output characteristics

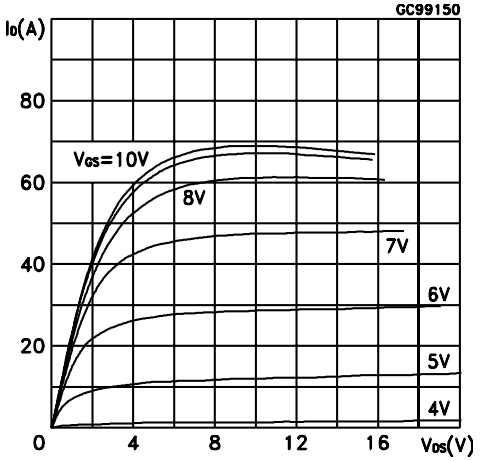


Figure 5: Transfer characteristics

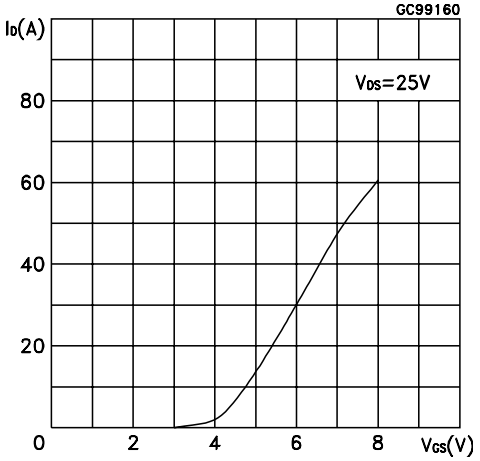


Figure 6: Transconductance

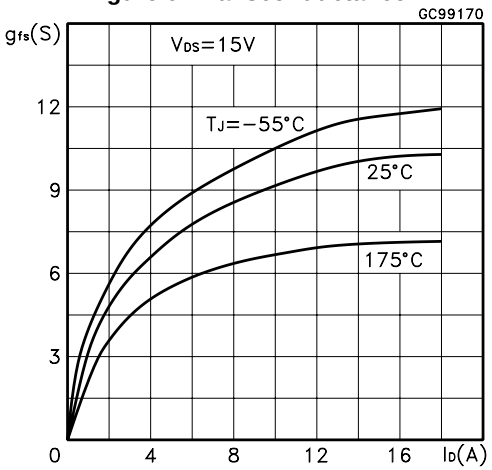


Figure 7: Static drain-source on-resistance

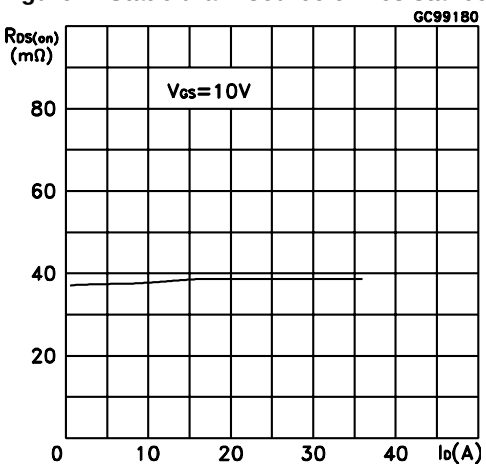


Figure 8: Gate charge vs. gate-source voltage

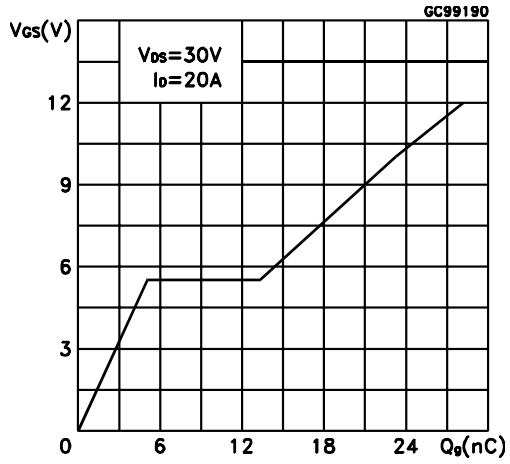


Figure 9: Capacitance variations

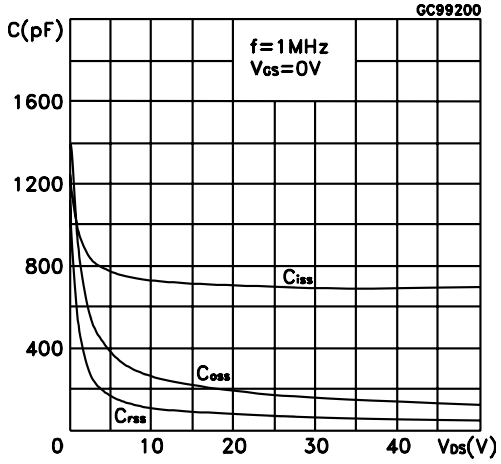


Figure 10: Normalized gate threshold voltage vs. temperature

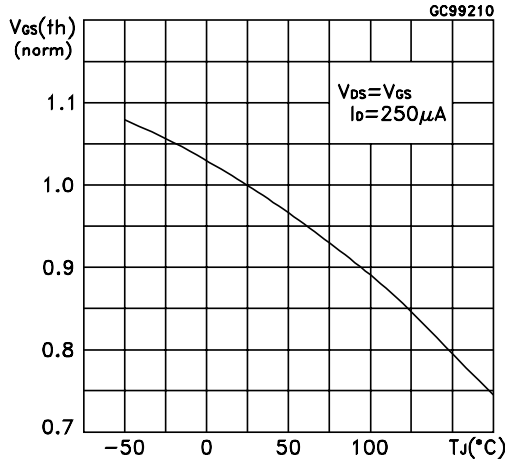


Figure 11: Normalized on-resistance vs. temperature

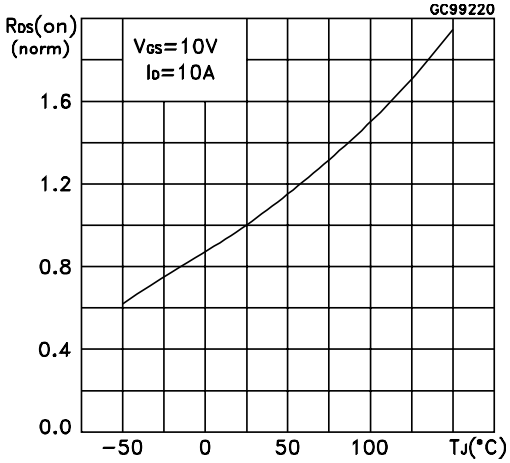


Figure 12: Source-drain diode forward characteristics

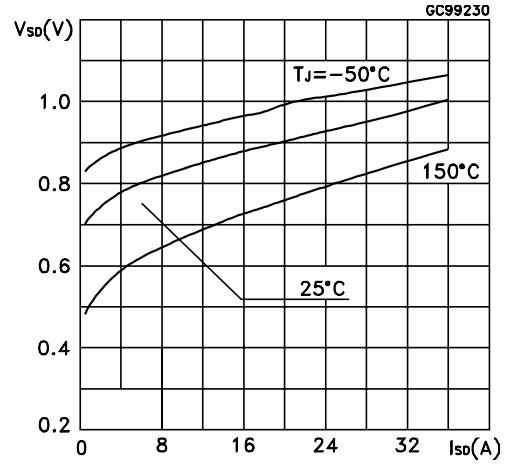
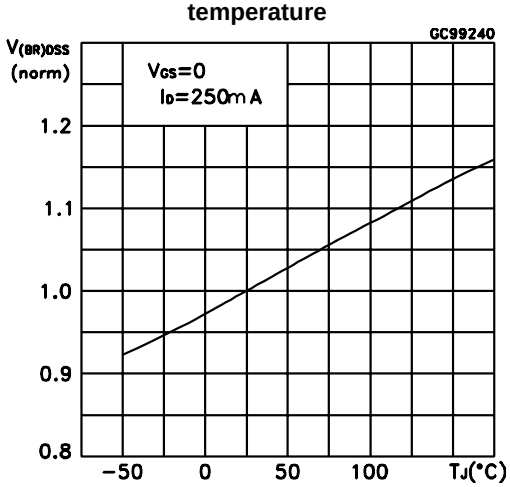


Figure 13: Normalized breakdown voltage vs. temperature



3 Test circuits

Figure 14: Test circuit for resistive load switching times

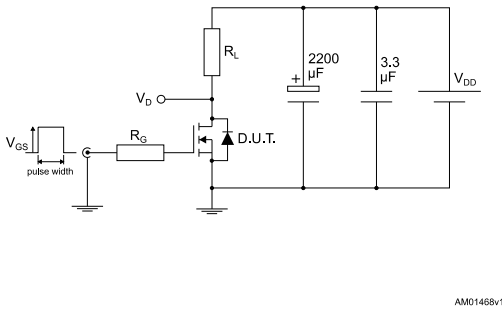


Figure 15: Test circuit for gate charge behavior

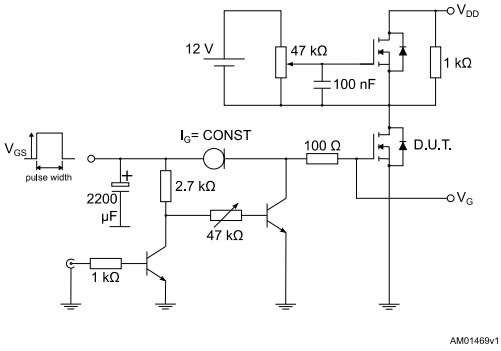


Figure 16: Test circuit for inductive load switching and diode recovery times

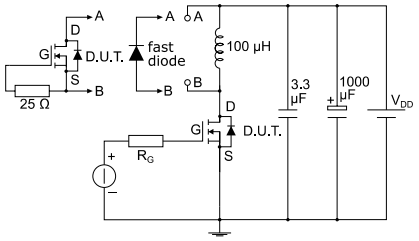


Figure 17: Unclamped inductive load test circuit

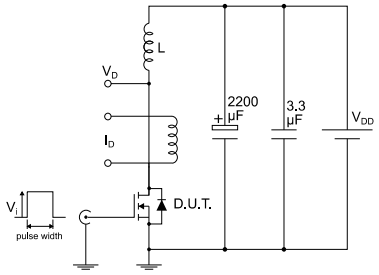


Figure 18: Unclamped inductive waveform

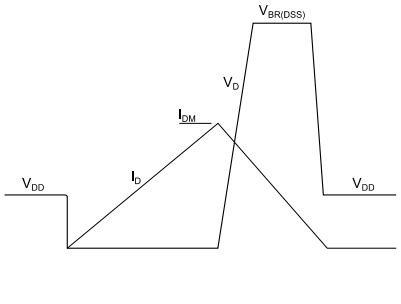
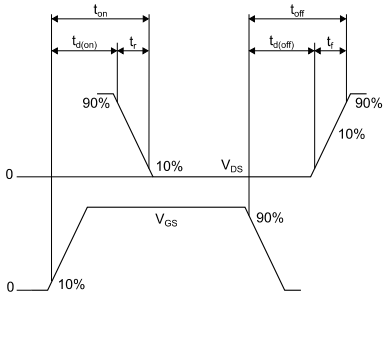


Figure 19: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A2 package information

Figure 20: DPAK (TO-252) type A2 package outline

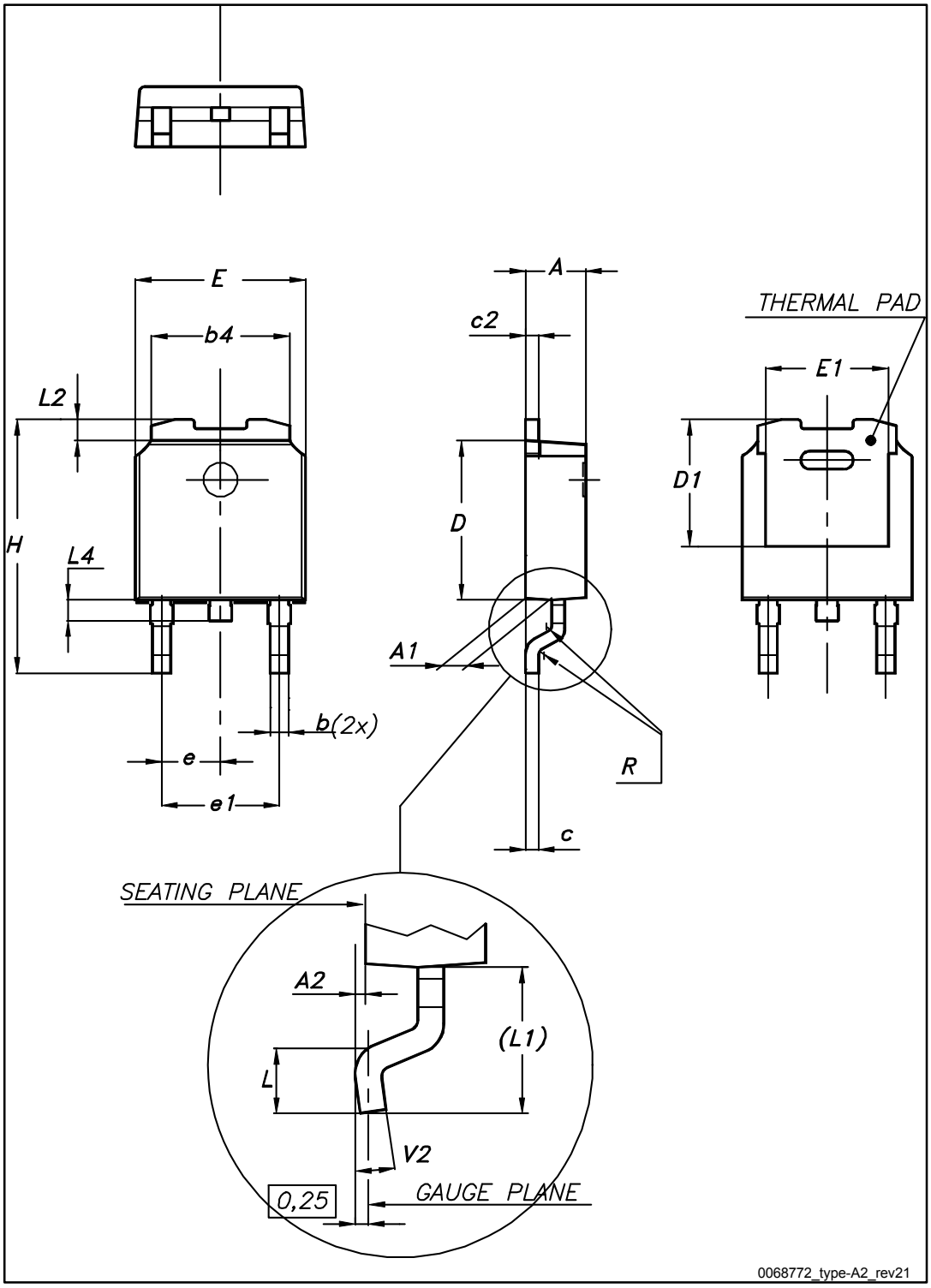
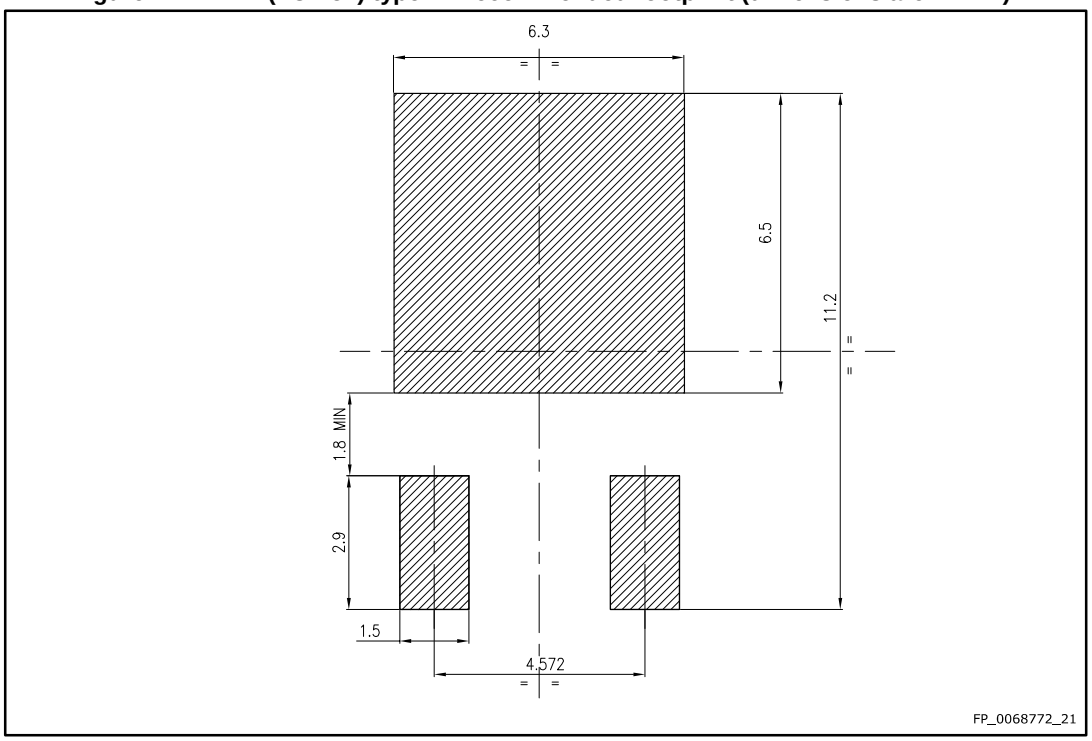


Table 7: DPAK (TO-252) type A2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 21: DPAK (TO-252) type A2 recommended footprint (dimensions are in mm)



4.2 DPAK packing information

Figure 22: DPAK (TO-252) tape outline

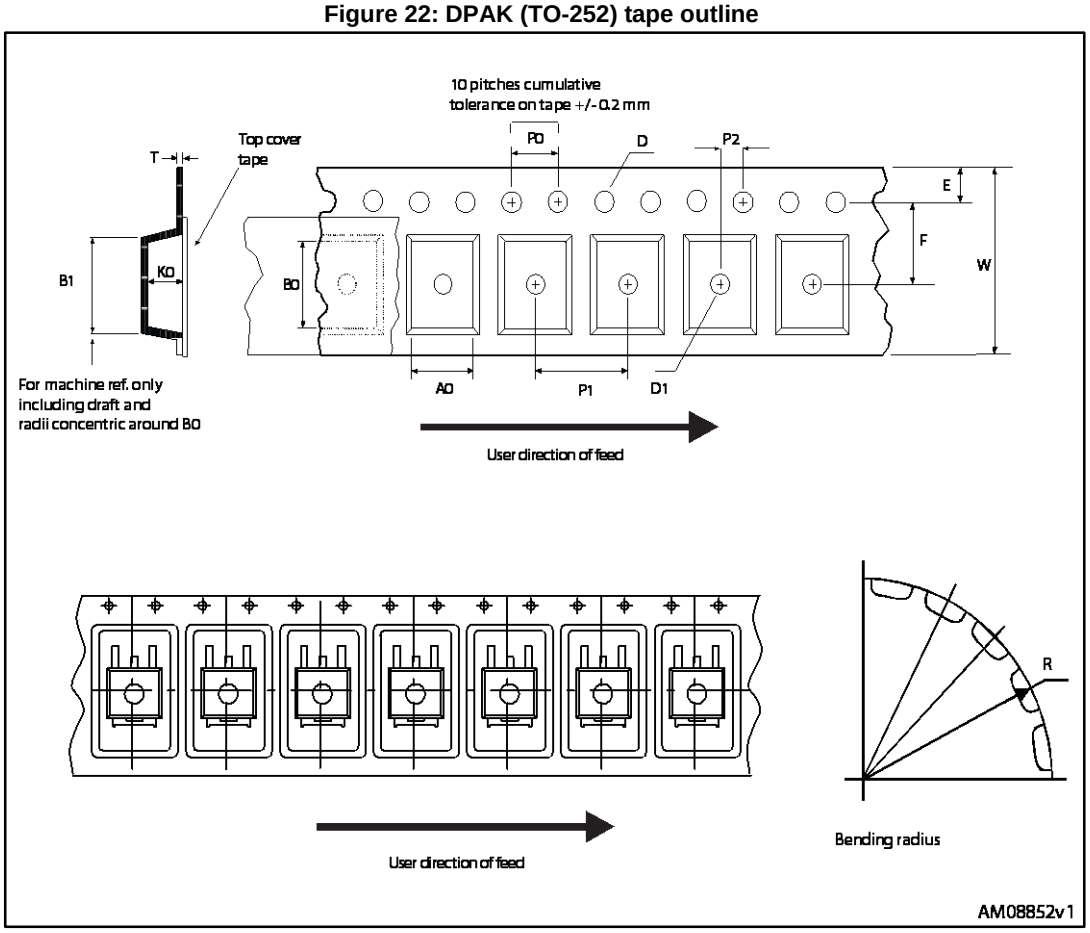


Figure 23: DPAK (TO-252) reel outline

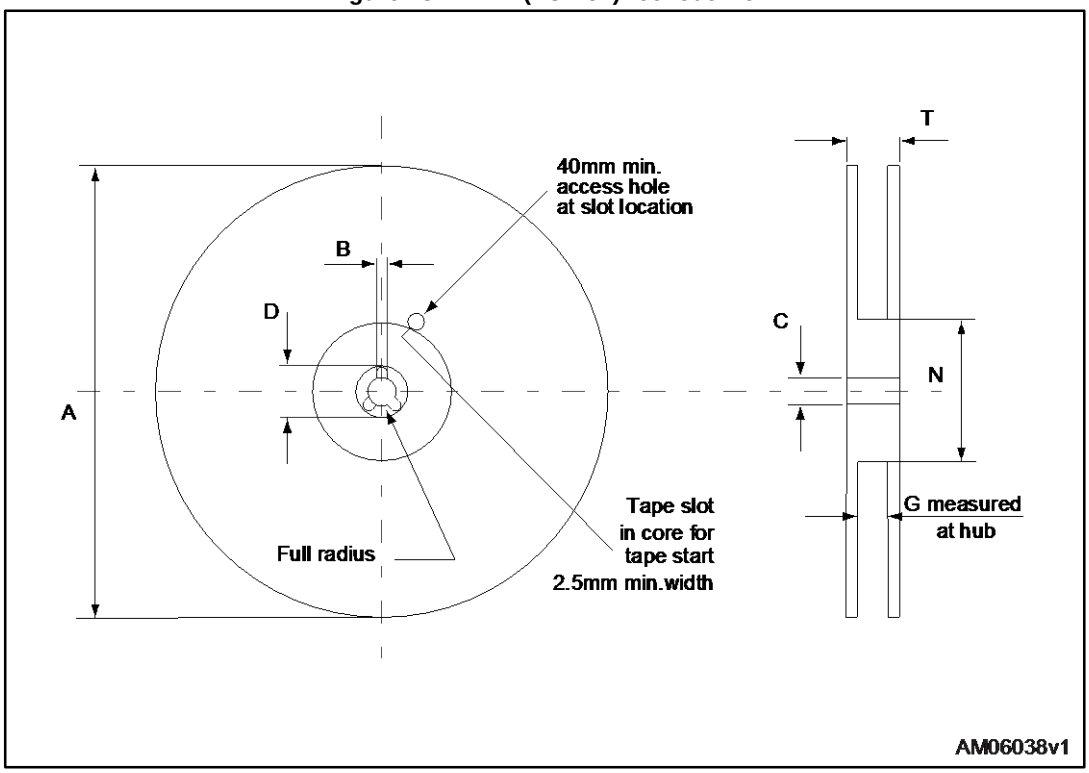


Table 8: DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
25-Oct-2016	1	First version.

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