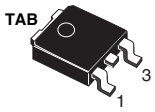
STD25NF10LA

N-channel 100 V, 0.030 Ω, 25 A DPAK STripFET™ II Power MOSFET

Features

Order code	V_{DSS}	$R_{DS(on)}$ max	I_D
STD25NF10LA	100 V	< 0.035 Ω	25 A

- Exceptional dv/dt capability
- 100% avalanche tested
- Logic level device



DPAK

Applications

- Switching application
- Automotive

Description

This Power MOSFET has been developed using STMicroelectronics' unique STripFET process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

Figure 1. Internal schematic diagram

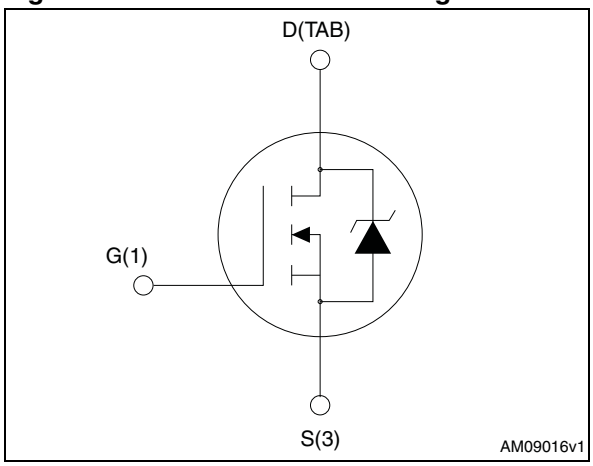


Table 1. Device summary

Order code	Marking	Package	Packaging
STD25NF10LA	D25NF10LA	DPAK	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate- source voltage	± 16	V
I_D (1)	Drain current (continuous) at T_C = 25 °C	25	A
I_D	Drain current (continuous) at T_C = 100 °C	21	A
I_{DM} (2)	Drain current (pulsed)	100	A
P_{tot}	Total dissipation at T_C = 25 °C	100	W
	Derating Factor	0.67	W/°C
dv/dt (3)	Peak diode recovery avalanche energy	20	V/ns
E_{AS} (4)	Single pulse avalanche energy	450	mJ
T_{stg}	Storage temperature	-55 to 175	°C
T_j	Max. operating junction temperature		

1. Current limited by package
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 25$ A, di/dt ≤ 300 A/µs, $V_{DD} = V_{(BR)DSS}$, $T_J \leq T_{JMAX}$
4. Starting T_j = 25 °C, I_D = 12.5 A V_{DD} = 50 V

Table 3. Thermal data

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case max	1.5	°C/W
Rthj-pcb	Thermal resistance junction-pcb max (1)	50	°C/W

1. When Mounted on 1 inch2 FR-4 board, 2 oz. of Cu.

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS} =0	100			V
I_{DSS}	Zero gate voltage drain current	V_{DS}= 100 V V_{DS}= 100 V, T_C = 125 °C V_{GS} =0			1 10	µA µA
I_{GSS}	Gate-body leakage current	V_{GS} = ± 16 V, V_{DS} = 0			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1		2.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 12.5 A V_{GS} = 4.5 V, I_D = 12.5 A		0.030 0.035	0.035 0.040	Ω Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	1710 250 110		pF pF pF
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off delay time Fall time	V_{DD} = 50 V, I_D = 12.5 A R_G = 4.7 Ω V_{GS} = 5 V (see *Figure 13*)	-	20 40 58 20		ns ns ns ns
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 80 V, I_D = 25 A, V_{GS} = 5 V, R_G = 4.7 Ω (see *Figure 14*)	-	38 8.5 21	52	nC nC nC

Table 6. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		25 100	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 25 A, V_{GS} = 0	-		1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 25 A, di/dt = 100 A/µs, V_{DD} = 50 V, T_j = 150 °C (see *Figure 15*)	-	88 317 7.2		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

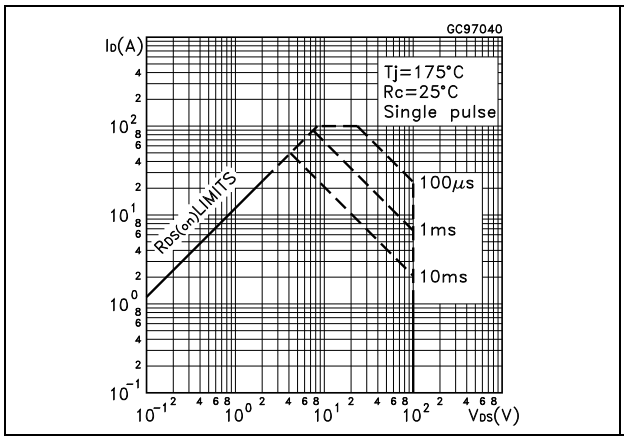


Figure 3. Thermal impedance

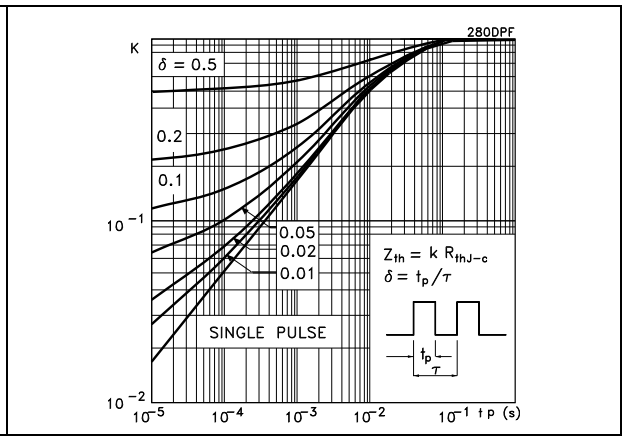


Figure 4. Output characteristics

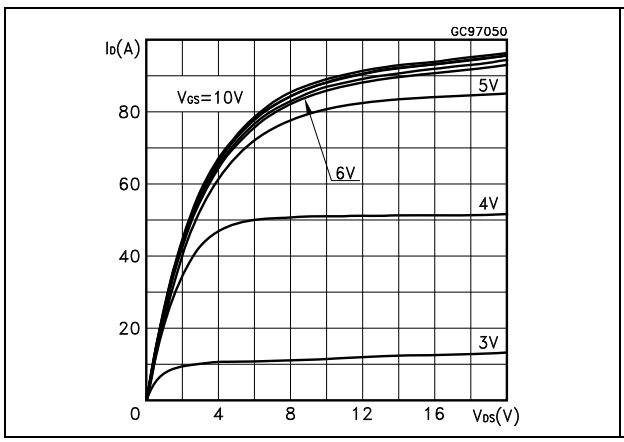


Figure 5. Transfer characteristics

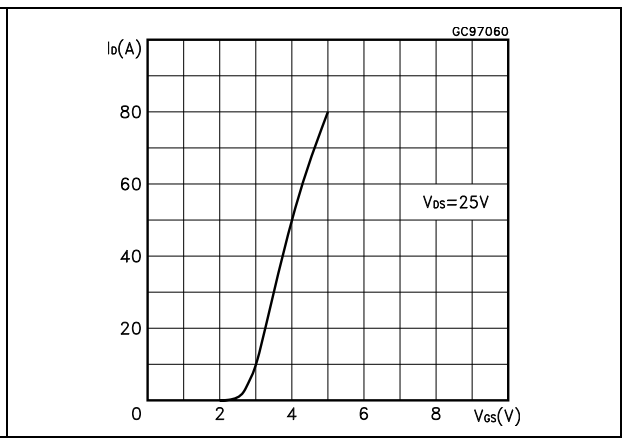


Figure 6. Normalized breakdown voltage vs. temperature

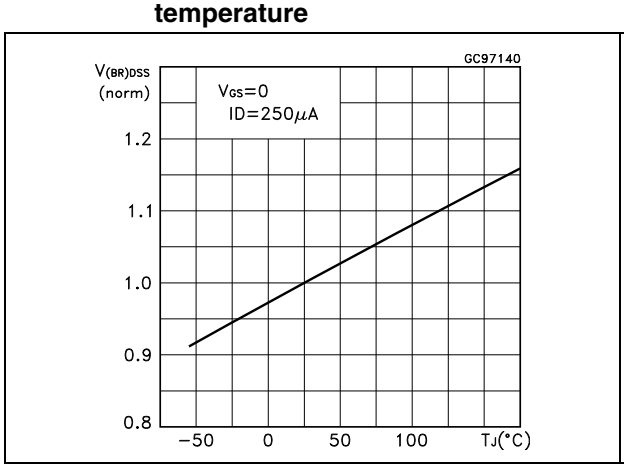


Figure 7. Static drain-source on resistance

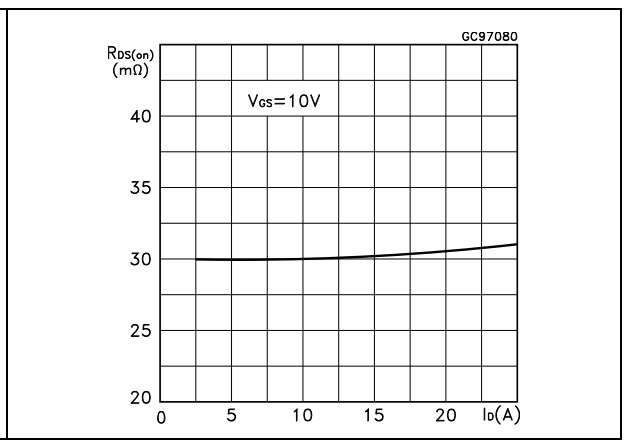


Figure 8. Gate charge vs. gate-source voltage

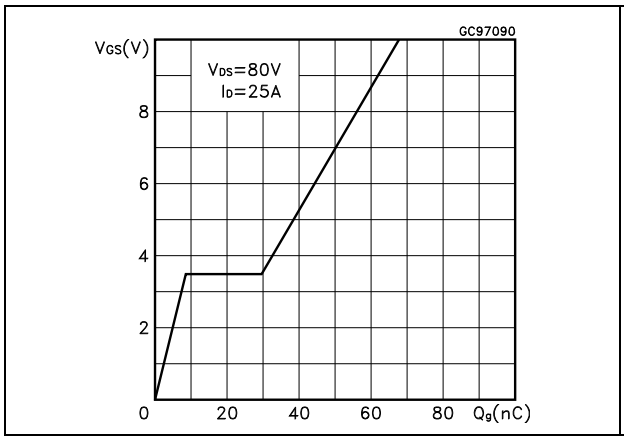


Figure 9. Capacitance variations

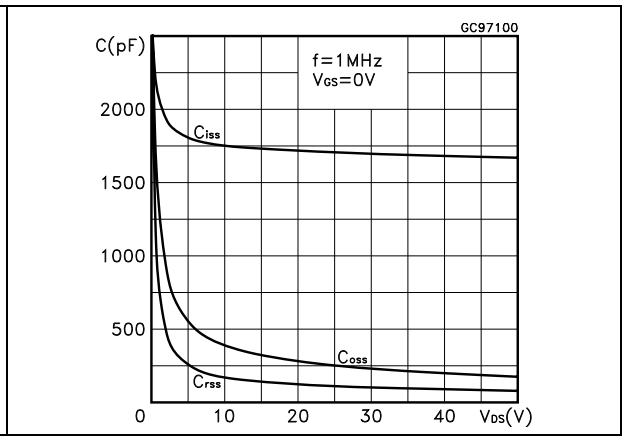


Figure 10. Normalized gate threshold voltage vs. temperature

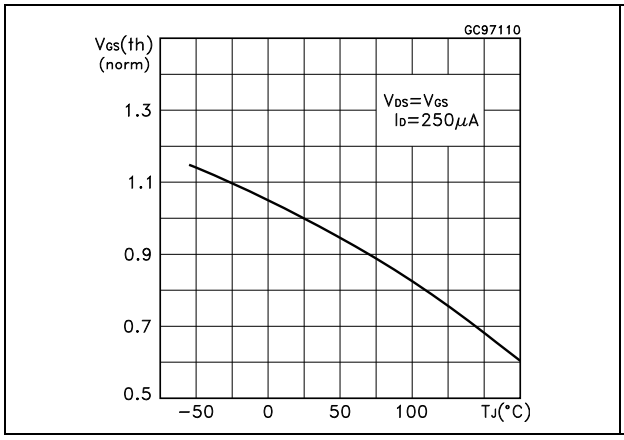


Figure 11. Normalized on resistance vs. temperature

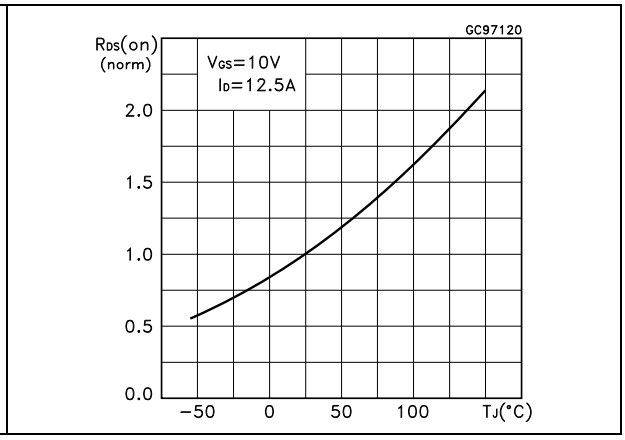
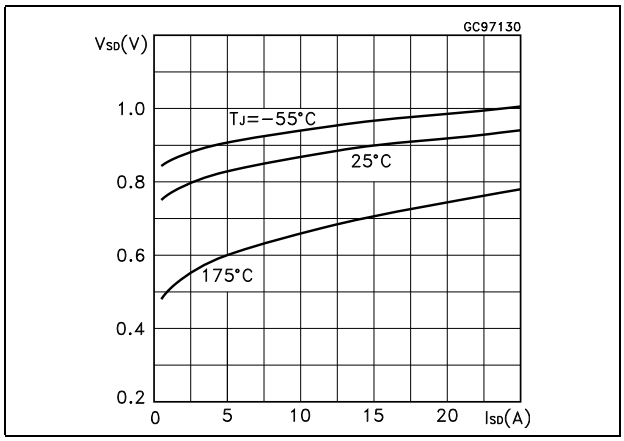


Figure 12. Source-drain diode forward characteristics



3 Test circuit

Figure 13. Switching times test circuit for resistive load

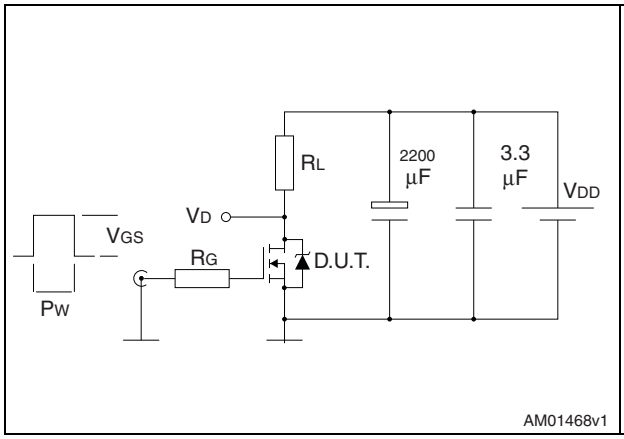


Figure 14. Gate charge test circuit

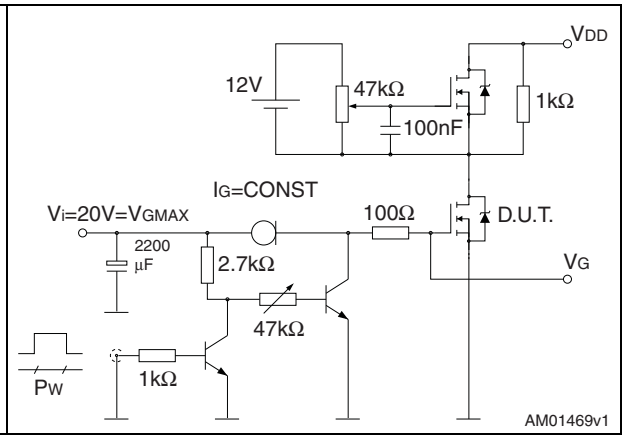


Figure 15. Test circuit for inductive load switching and diode recovery times

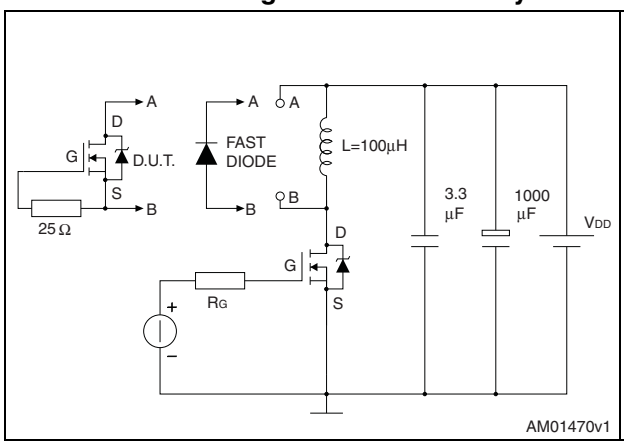


Figure 16. Unclamped Inductive load test circuit

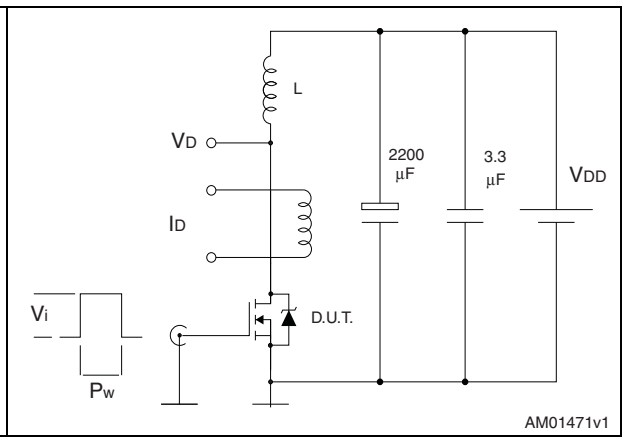


Figure 17. Unclamped inductive waveform

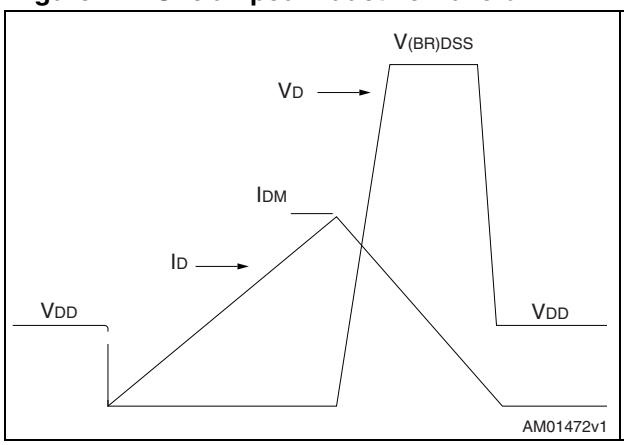
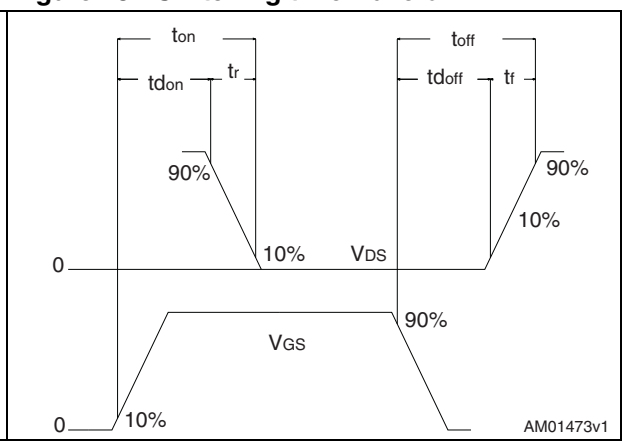


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 7. DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		1.50
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

Figure 19. DPAK (TO-252) drawing

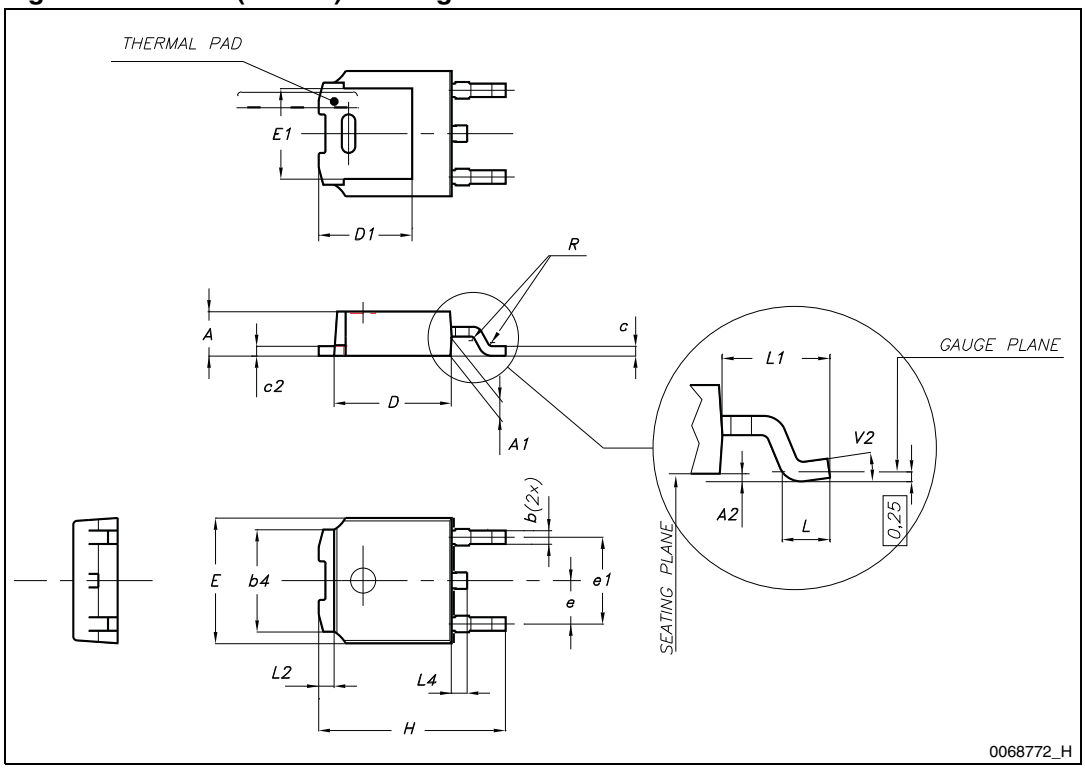
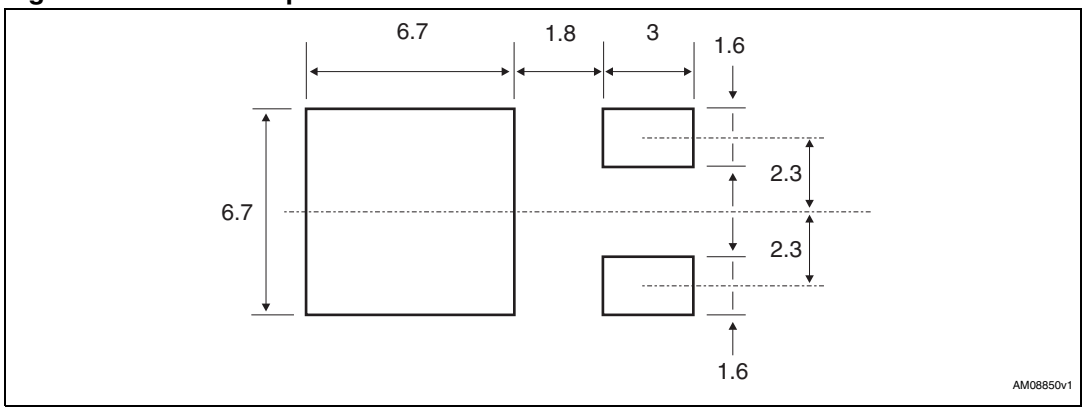


Figure 20. DPAK footprint[a]



a. All dimensions are in millimeters

5 Packing mechanical data

Table 8. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 21. Tape for DPAK (TO-252)

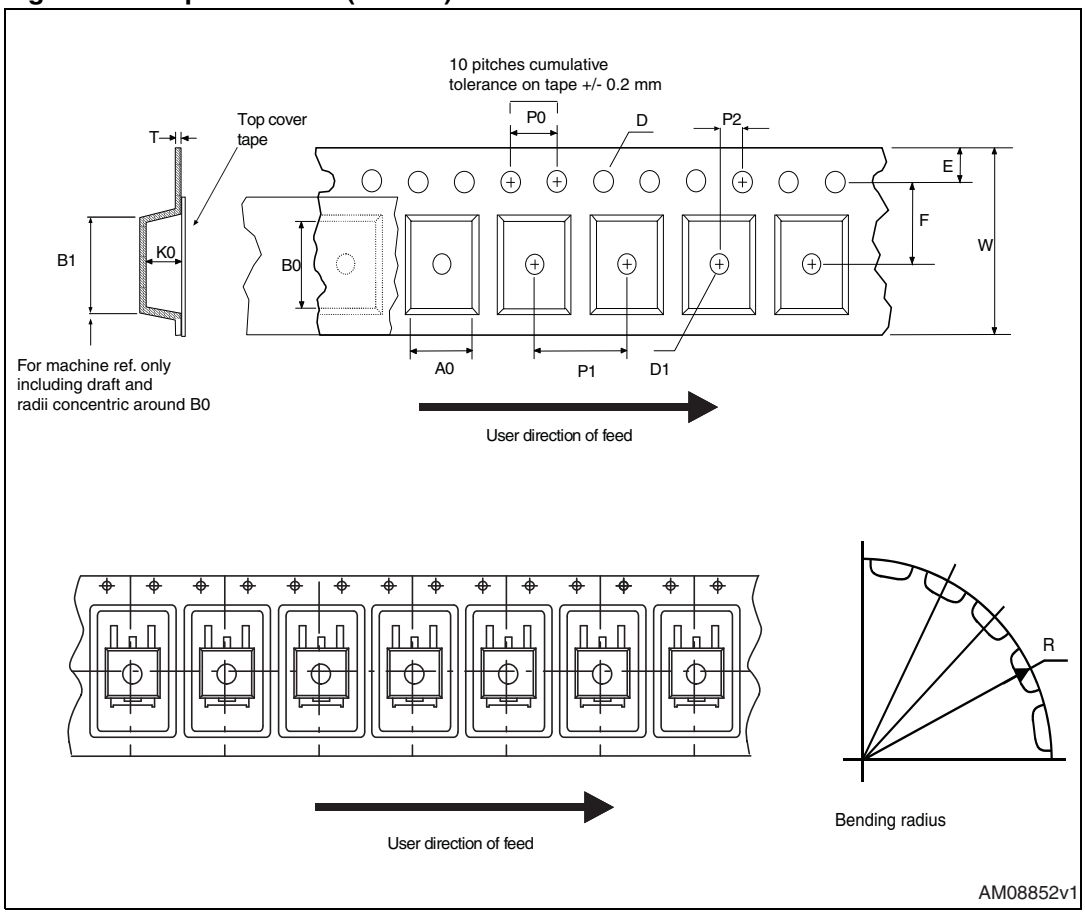
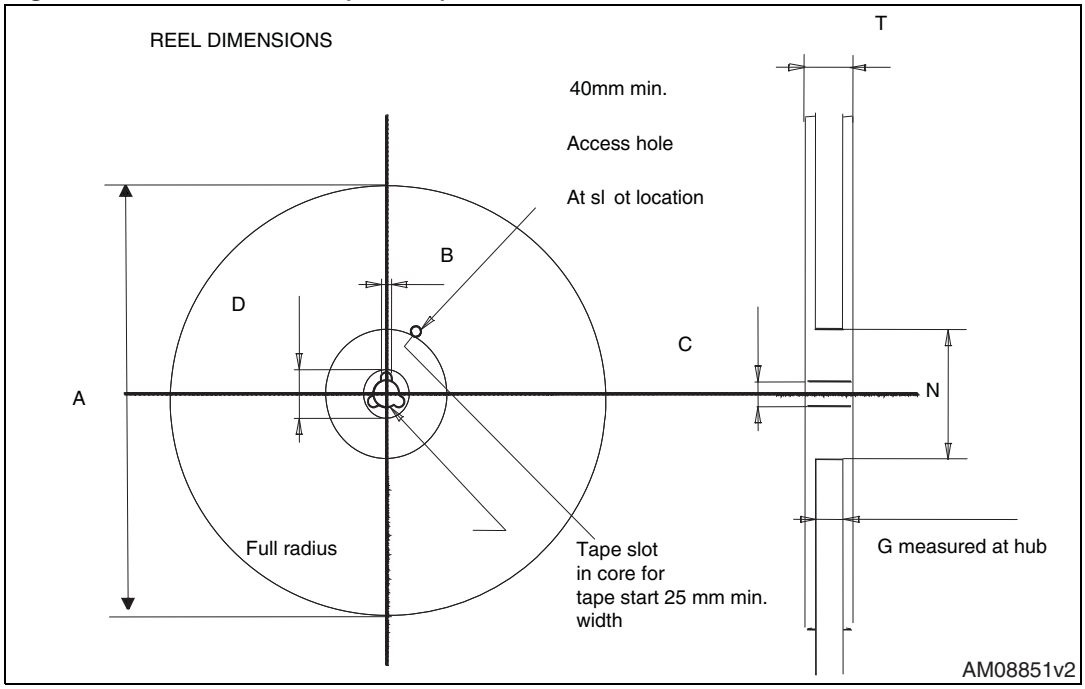


Figure 22. Reel for DPAK (TO-252)



6 Revision history

Table 9. Revision history

Date	Revision	Changes
05-Oct-2011	1	First release.

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