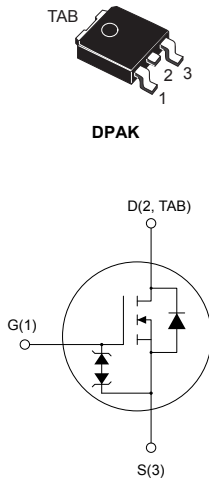


N-channel 1000 V, 6.25 Ω typ., 1.85 A SuperMESH Power MOSFET in a DPAK package



AM01476v1_tab



Features

| Order code | V_{DS} | $R_{DS(on)}$ max. | I_D |
|------------|----------|-------------------|--------|
| STD2NK100Z | 1000 V | 8.5 Ω | 1.85 A |

- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance
- Zener-protected

Applications

- Switching applications

Description

This high-voltage device is a Zener-protected N-channel Power MOSFET developed using the SuperMESH technology by STMicroelectronics, an optimization of the well-established PowerMESH. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

Product status link

[STD2NK100Z](#)

Product summary

| | |
|-------------------|---------------|
| Order code | STD2NK100Z |
| Marking | 2NK100Z |
| Package | DPAK |
| Packing | Tape and reel |

1 Electrical ratings

Table 1. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|----------------|--|------------|------------------|
| V_{DS} | Drain-source voltage | 1000 | V |
| V_{GS} | Gate-source voltage | ± 30 | V |
| I_D | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$ | 1.85 | A |
| | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$ | 1.6 | |
| $I_{DM}^{(1)}$ | Drain current (pulsed) | 7.4 | A |
| P_{TOT} | Total power dissipation at $T_C = 25\text{ }^\circ\text{C}$ | 70 | W |
| ESD | Gate-source, human body model ($R = 1.5\text{ k}\Omega$, $C = 100\text{ pF}$) | 3 | kV |
| $dv/dt^{(2)}$ | Peak diode recovery voltage slope | 2.5 | V/ns |
| T_{stg} | Storage temperature range | -55 to 150 | $^\circ\text{C}$ |
| T_J | Operating junction temperature range | | $^\circ\text{C}$ |

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 1.85\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} = 80\% V_{(BR)DSS}$.

Table 2. Thermal data

| Symbol | Parameter | Value | Unit |
|------------------|---|-------|---------------------------|
| R_{thJC} | Thermal resistance, junction-to-case | 1.79 | $^\circ\text{C}/\text{W}$ |
| $R_{thJA}^{(1)}$ | Thermal resistance, junction-to-ambient | 50 | $^\circ\text{C}/\text{W}$ |

1. When mounted on an 1-inch² FR-4, 2 Oz copper board.

Table 3. Avalanche characteristics

| Symbol | Parameter | Value | Unit |
|----------|--|-------|------|
| I_{AR} | Avalanche current, repetitive or not repetitive (pulse width is limited by T_J max.) | 1.85 | A |
| E_{AS} | Single pulse avalanche energy (starting $T_J = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$) | 170 | mJ |

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified.

Table 4. On/off states

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|-----------------------------------|--|------|------|----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS} = 0\text{ V}$, $I_D = 1\text{ mA}$ | 1000 | | | V |
| I_{DSS} | Zero gate voltage drain current | $V_{GS} = 0\text{ V}$, $V_{DS} = 1000\text{ V}$ | | | 1 | μA |
| | | $V_{GS} = 0\text{ V}$, $V_{DS} = 1000\text{ V}$, $T_C = 125\text{ °C}^{(1)}$ | | | 50 | μA |
| I_{GSS} | Gate-body leakage current | $V_{DS} = 0\text{ V}$, $V_{GS} = \pm 30\text{ V}$ | | | ± 10 | μA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = V_{GS}$, $I_D = 50\text{ }\mu\text{A}$ | 3 | 3.75 | 4.5 | V |
| $R_{DS(on)}$ | Static drain-source on resistance | $V_{GS} = 10\text{ V}$, $I_D = 0.9\text{ A}$ | | 6.25 | 8.5 | Ω |

1. Specified by design, not tested in production.

Table 5. Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|----------------------------|-------------------------------|---|------|------|------|----------|
| C_{iss} | Input capacitance | $V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$ | - | 499 | - | pF |
| C_{oss} | Output capacitance | | - | 53 | - | pF |
| C_{rss} | Reverse transfer capacitance | | - | 9 | - | pF |
| $C_{oss\text{ eq.}}^{(1)}$ | Equivalent output capacitance | $V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ V to } 800\text{ V}$ | - | 28 | - | pF |
| R_G | Gate input resistance | $f = 1\text{ MHz}$, open drain | - | 6.6 | - | Ω |
| Q_g | Total gate charge | $V_{DD} = 800\text{ V}$, $I_D = 1.85\text{ A}$, $V_{GS} = 0\text{ to } 10\text{ V}$ (see Figure 14. Test circuit for gate charge behavior) | - | 16 | - | nC |
| Q_{gs} | Gate-source charge | | - | 3 | - | nC |
| Q_{gd} | Gate-drain charge | | - | 9 | - | nC |

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------|---------------------|---|------|------|------|------|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD} = 500\text{ V}$, $I_D = 0.9\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ | - | 7.2 | - | ns |
| t_r | Rise time | | - | 6.5 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | (see Figure 13. Test circuit for resistive load switching times and Figure 18. Switching time waveform) | - | 41.5 | - | ns |
| t_f | Fall time | | - | 32.5 | - | ns |

Table 7. Source-drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|---|------|------|------|---------------|
| I_{SD} | Source-drain current | | - | | 1.85 | A |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | - | | 7.4 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $I_{SD} = 1.85 \text{ A}$, $V_{GS} = 0 \text{ V}$ | - | | 1.6 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = 1.85 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ | - | 476 | | ns |
| Q_{rr} | Reverse recovery charge | $V_{DD} = 60 \text{ V}$ | - | 1.6 | | μC |
| I_{RRM} | Reverse recovery current | (see Figure 15. Test circuit for inductive load switching and diode recovery times) | - | 6.9 | | A |
| t_{rr} | Reverse recovery time | $I_{SD} = 1.85 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ | - | 532 | | ns |
| Q_{rr} | Reverse recovery charge | $V_{DD} = 60 \text{ V}$, $T_J = 150 \text{ }^\circ\text{C}$ | - | 1.9 | | μC |
| I_{RRM} | Reverse recovery current | (see Figure 15. Test circuit for inductive load switching and diode recovery times) | - | 88 | | A |

1. Pulse width is limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

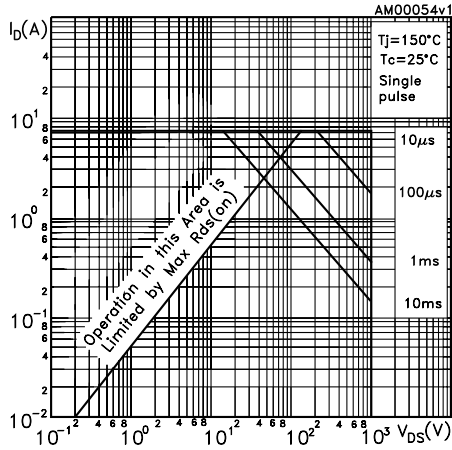


Figure 2. Thermal impedance

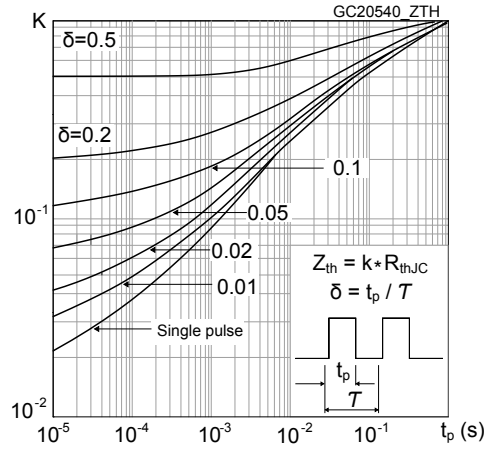


Figure 3. Output characteristics

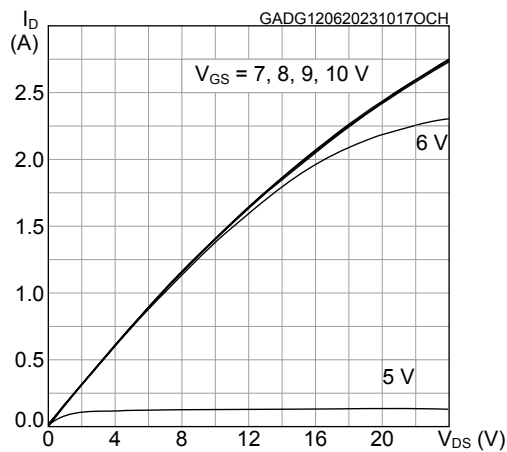


Figure 4. Transfer characteristics

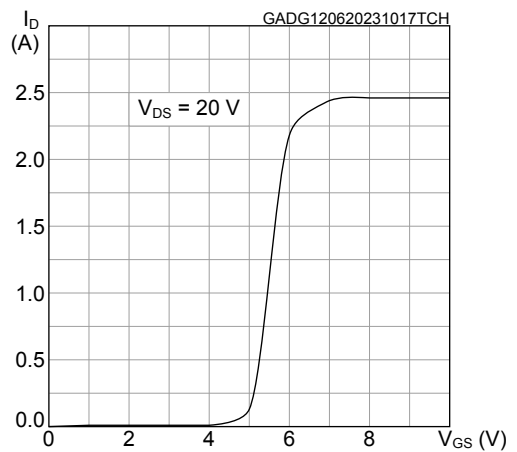


Figure 5. Normalized $V_{(BR)DSS}$ vs temperature

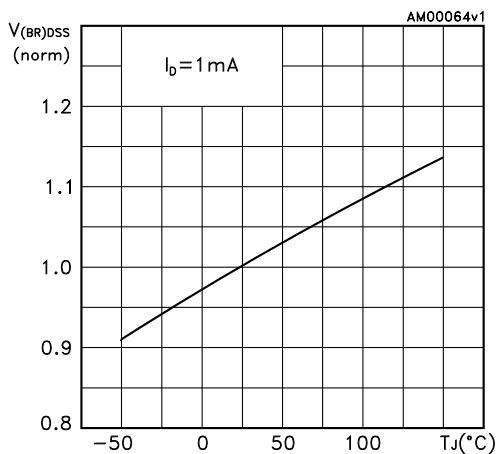


Figure 6. Static drain-source on resistance

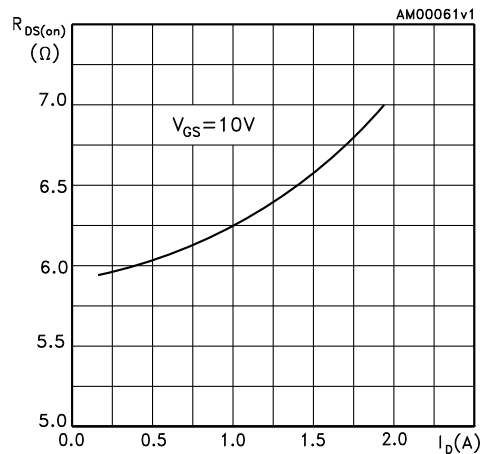


Figure 7. Gate charge vs gate-source voltage

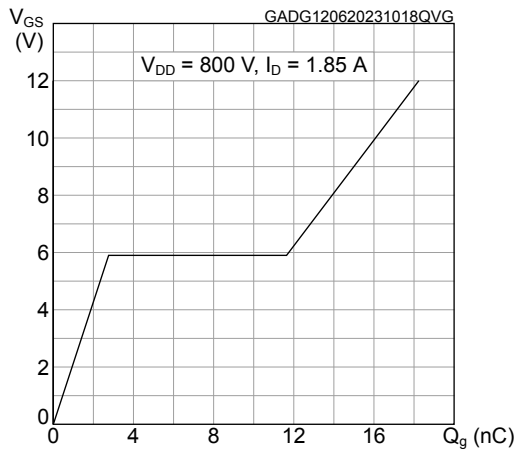


Figure 8. Capacitance variations

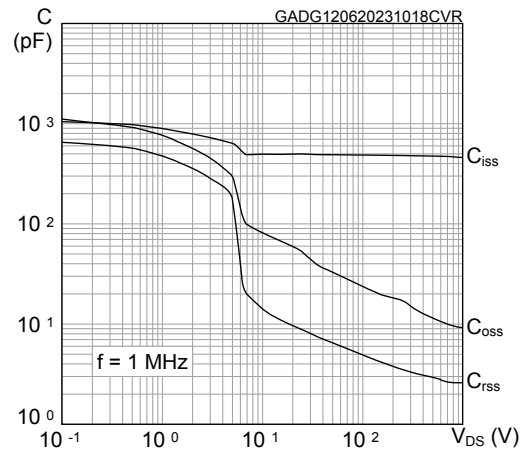


Figure 9. Normalized gate threshold voltage vs temperature

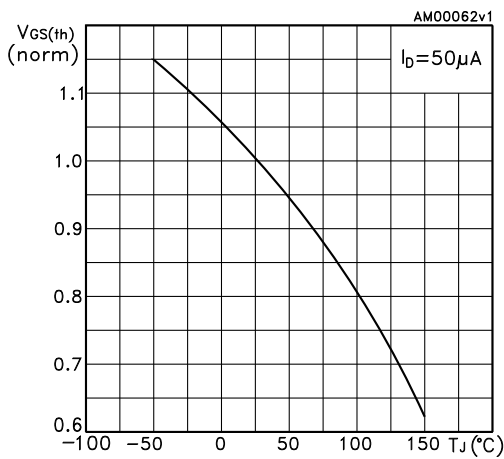


Figure 10. Normalized on resistance vs temperature

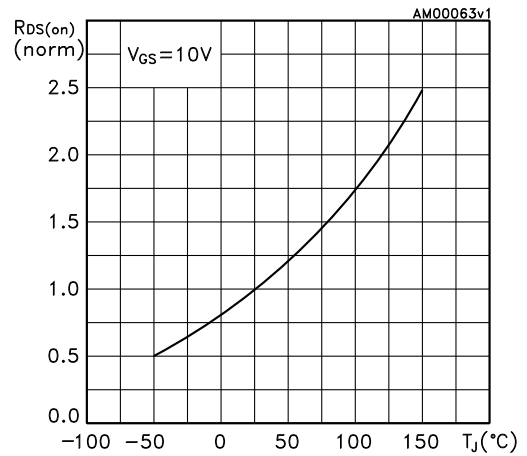


Figure 11. Source-drain diode forward characteristics

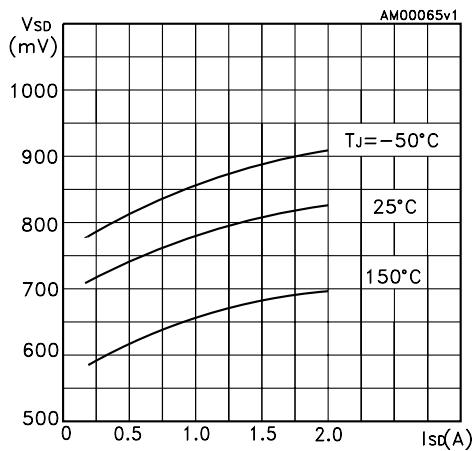
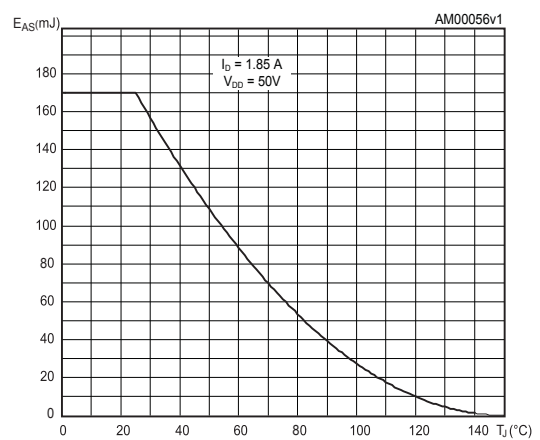
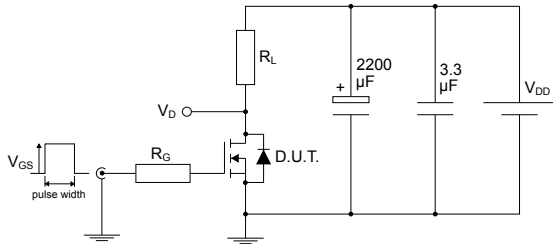


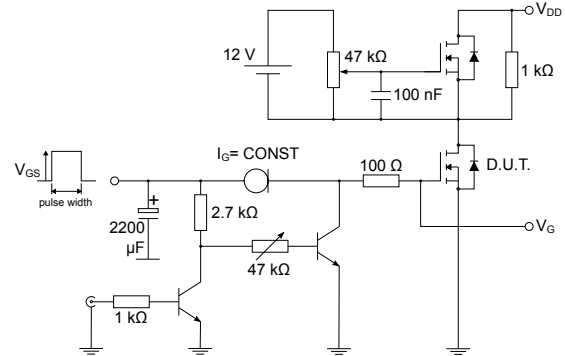
Figure 12. Maximum avalanche energy vs temperature



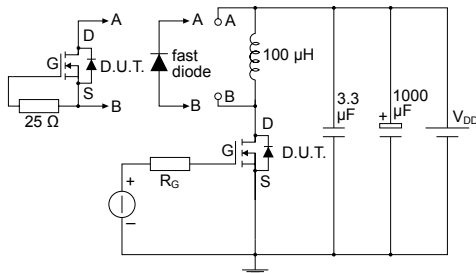
3 Test circuits

Figure 13. Test circuit for resistive load switching times


AM01468v1

Figure 14. Test circuit for gate charge behavior


AM01469v1

Figure 15. Test circuit for inductive load switching and diode recovery times


AM01470v1

Figure 16. Unclamped inductive load test circuit


AM01471v1

Figure 17. Unclamped inductive waveform


AM01472v1

Figure 18. Switching time waveform

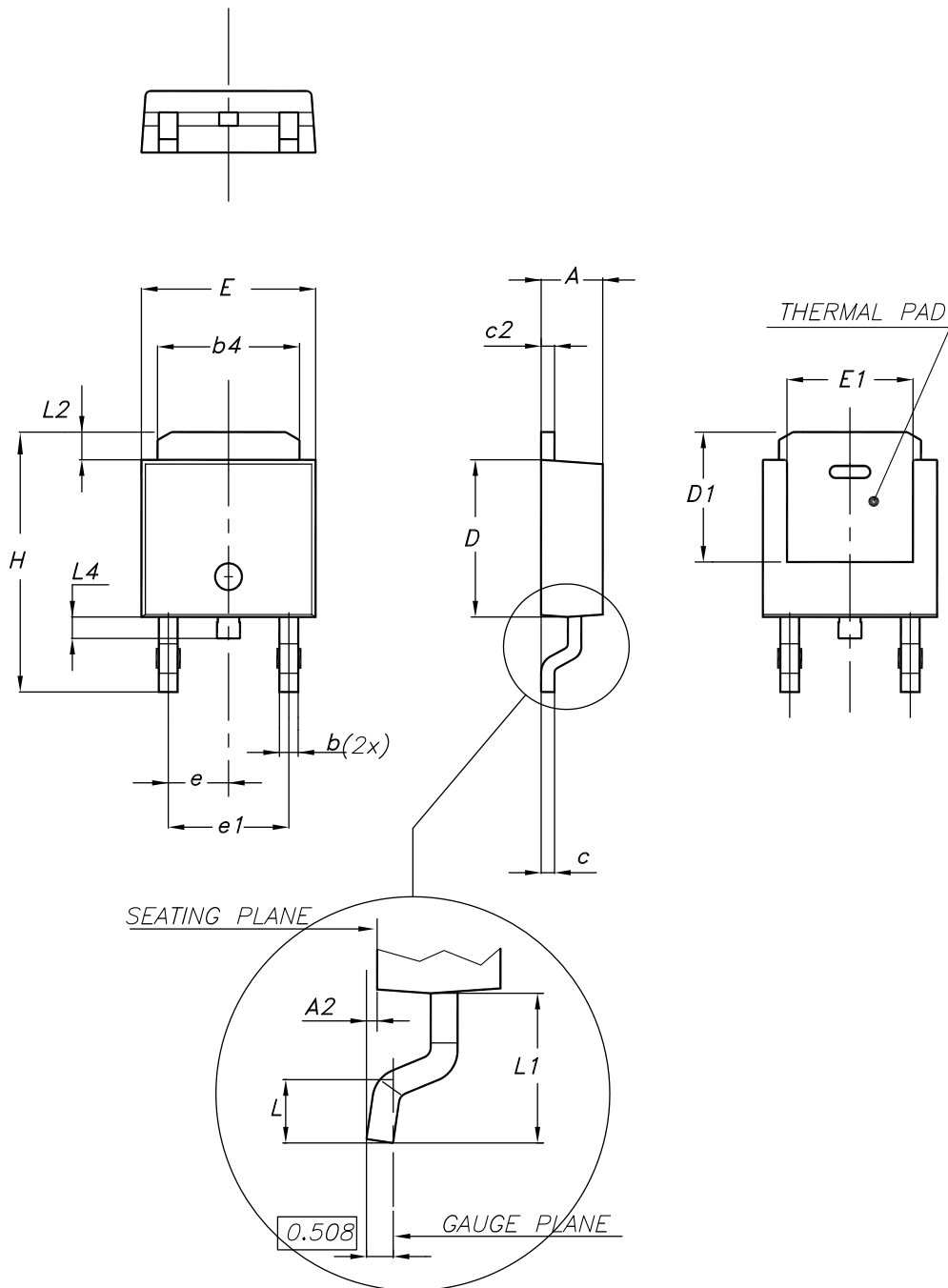

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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 DPAK (TO-252) type E package information

Figure 19. DPAK (TO-252) type E package outline

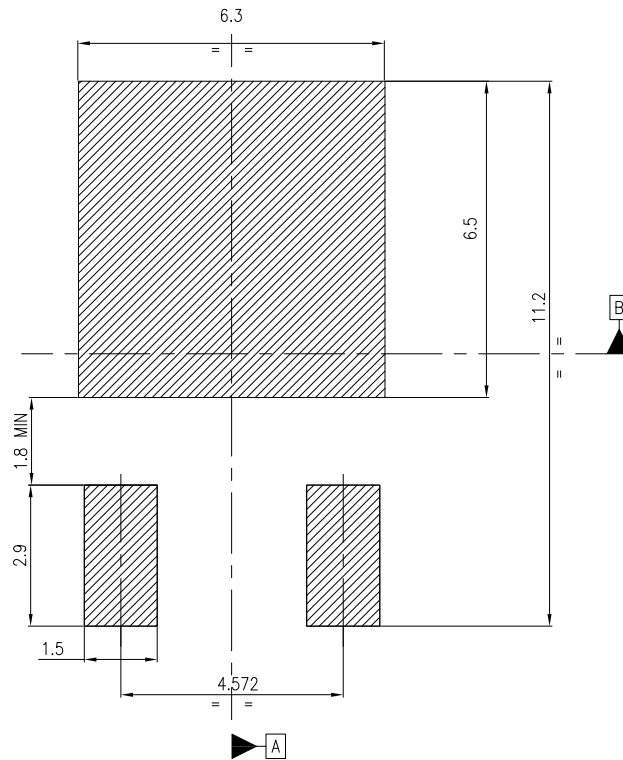


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Table 8. DPAK (TO-252) type E mechanical data

| Dim. | mm | | |
|------|------|-------|-------|
| | Min. | Typ. | Max. |
| A | 2.18 | | 2.39 |
| A2 | | | 0.13 |
| b | 0.65 | | 0.884 |
| b4 | 4.95 | | 5.46 |
| c | 0.46 | | 0.61 |
| c2 | 0.46 | | 0.60 |
| D | 5.97 | | 6.22 |
| D1 | 5.21 | | |
| E | 6.35 | | 6.73 |
| E1 | 4.32 | | |
| e | | 2.286 | |
| e1 | | 4.572 | |
| H | 9.94 | | 10.34 |
| L | 1.50 | | 1.78 |
| L1 | | 2.74 | |
| L2 | 0.89 | | 1.27 |
| L4 | | | 1.02 |

Figure 20. DPAK (TO-252) recommended footprint (dimensions are in mm)



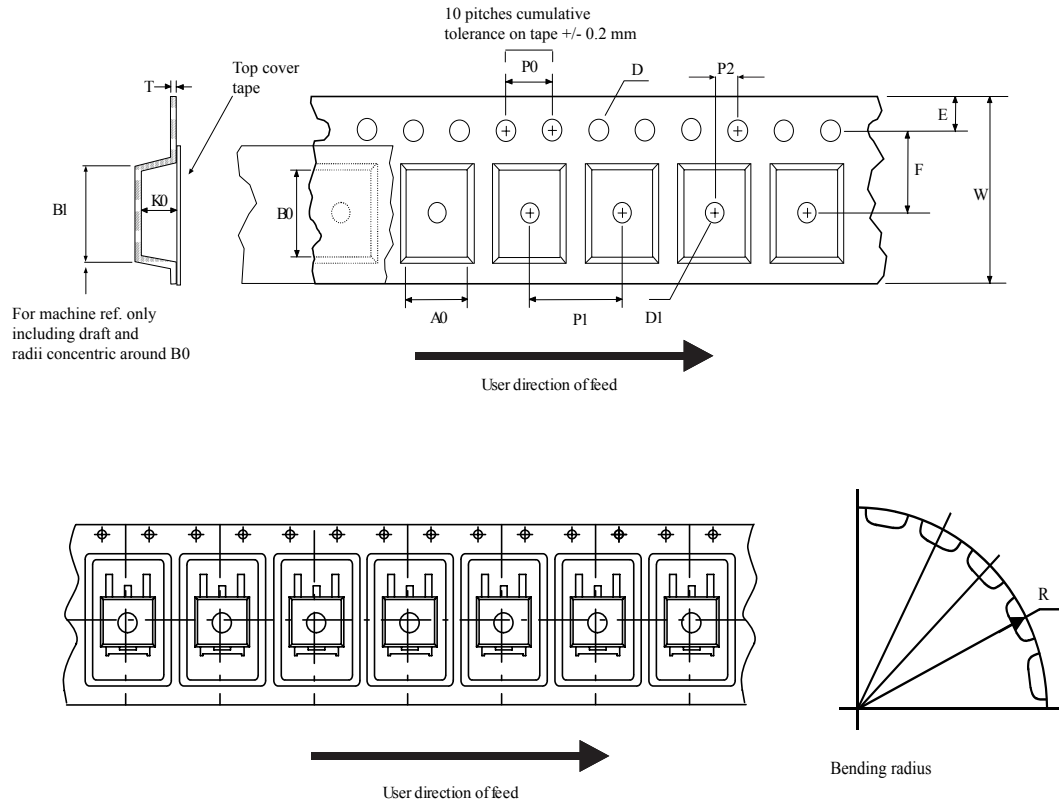
Notes:

- 1) This footprint is able to ensure insulation up to 630 Vrms (according to CEI IEC 664-1)
- 2) The device must be positioned within $\oplus 0.05$ A B

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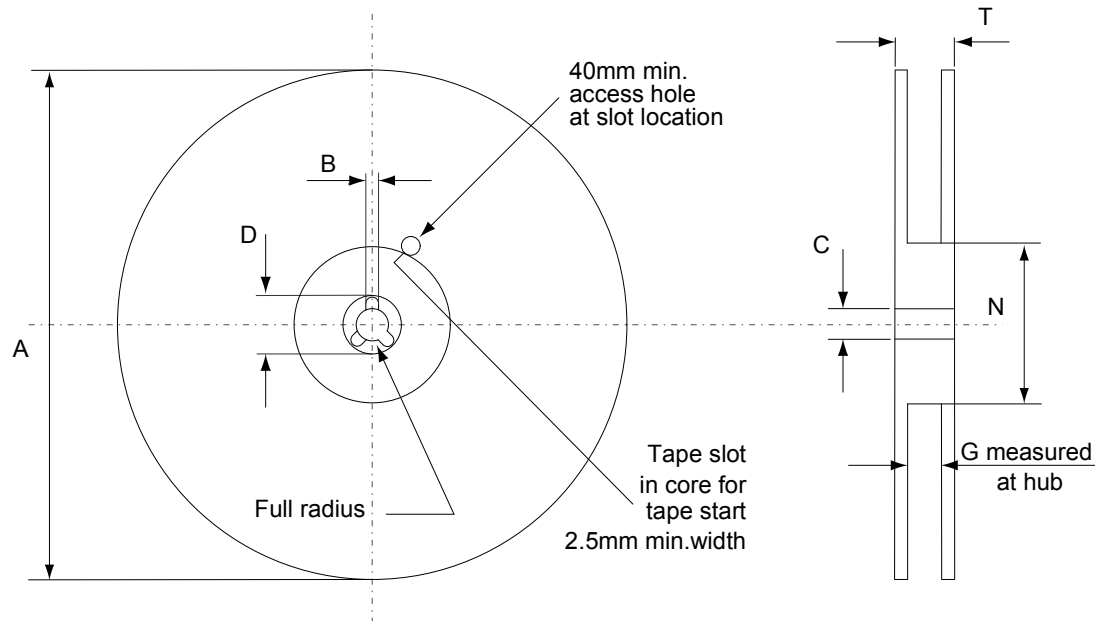
4.2 DPAK (TO-252) packing information

Figure 21. DPAK (TO-252) tape outline



AM08852v1

Figure 22. DPAK (TO-252) reel outline



AM06038v1

Table 9. DPAK (TO-252) tape and reel mechanical data

| Dim. | Tape | | Dim. | Reel | |
|------|------|------|-----------|------|------|
| | mm | | | mm | |
| | Min. | Max. | | Min. | Max. |
| A0 | 6.8 | 7 | A | | 330 |
| B0 | 10.4 | 10.6 | B | 1.5 | |
| B1 | | 12.1 | C | 12.8 | 13.2 |
| D | 1.5 | 1.6 | D | 20.2 | |
| D1 | 1.5 | | G | 16.4 | 18.4 |
| E | 1.65 | 1.85 | N | 50 | |
| F | 7.4 | 7.6 | T | | 22.4 |
| K0 | 2.55 | 2.75 | | | |
| P0 | 3.9 | 4.1 | Base qty. | | 2500 |
| P1 | 7.9 | 8.1 | Bulk qty. | | 2500 |
| P2 | 1.9 | 2.1 | | | |
| R | 40 | | | | |
| T | 0.25 | 0.35 | | | |
| W | 15.7 | 16.3 | | | |

Revision history

Table 10. Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 21-Jun-2023 | 1 | First release. The part number STD2NK100Z was previously inserted in the DS5280. |

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