



STD40NF02L

N-CHANNEL 20V - 0.01 Ω - 40A DPAK LOW GATE CHARGE STripFET™ POWER MOSFET

TARGET DATA

TYPE	V _{DSS}	R _{DS(on)}	I _D
STD40NF02L	20 V	< 0.013 Ω	40 A

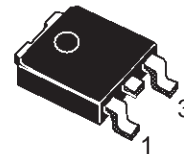
- TYPICAL R_{DS(on)} = 0.01 Ω
- TYPICAL Q_g = 35 nC @ 10V
- OPTIMAL R_{DS(on)} X Q_g TRADE-OFF
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED

DESCRIPTION

This application specific Power Mosfet is the third generation of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows the best trade-off between on-resistance and gate charge. When used as high and low side in buck regulators, it gives the best performance in terms of both conduction and switching losses. This is extremely important for motherboards where fast switching and high efficiency are of paramount importance.

APPLICATIONS

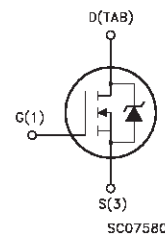
- SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY CPU CORE DC/DC CONVERTERS



**DPAK
TO-252
(Suffix "T4")**

ADD SUFFIX "T4" FOR ORDERING IN TAPE & REEL

INTERNAL SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	20	V
V _{DGR}	Drain- gate Voltage (R _{GS} = 20 k Ω)	20	V
V _{GS}	Gate-source Voltage	\pm 20	V
I _D (●)	Drain Current (continuous) at T _c = 25 °C	20	A
I _D (●)	Drain Current (continuous) at T _c = 100 °C	20	A
I _{DM} (●●)	Drain Current (pulsed)	80	A
P _{tot}	Total Dissipation at T _c = 25 °C	55	W
	Derating Factor	0.37	W/°C
T _{stg}	Storage Temperature	-65 to 175	°C
T _j	Max. Operating Junction Temperature	175	°C

(●) Current Limited By The Package

(●●) Pulse width limited by safe operating area

STD40NF02L

THERMAL DATA

$R_{thj-case}$	Thermal Resistance Junction-case	Max	2.73	$^{\circ}C/W$
$R_{thj-amb}$	Thermal Resistance Junction-ambient	Max	62.5	$^{\circ}C/W$
T_l	Maximum Lead Temperature For Soldering Purpose		300	$^{\circ}C$

ELECTRICAL CHARACTERISTICS ($T_{case} = 25^{\circ}C$ unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250 \mu A$ $V_{GS} = 0$	20			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$ $T_c = 125^{\circ}C$			1 10	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20 V$			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ $I_D = 250 \mu A$	1		2.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10V$ $I_D = 20 A$ $V_{GS} = 5V$ $I_D = 20 A$		0.01 0.015	0.013 0.019	Ω Ω
$I_{D(on)}$	On State Drain Current	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $V_{GS} = 10 V$	20			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (*)$	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}$ $I_D = 20 A$		40		S
C_{iss}	Input Capacitance	$V_{DS} = 25 V$ $f = 1 MHz$ $V_{GS} = 0$		1500		pF
C_{oss}	Output Capacitance			900		pF
C_{rss}	Reverse Transfer Capacitance			200		pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 15\text{ V}$ $I_D = 20\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$ (Resistive Load, see fig. 3)		20		ns
t_r	Rise Time			170		ns
Q_g	Total Gate Charge	$V_{DD} = 16\text{ V}$ $I_D = 20\text{ A}$ $V_{GS} = 10\text{ V}$		36	45	nC
Q_{gs}	Gate-Source Charge			5		nC
Q_{gd}	Gate-Drain Charge			10		nC

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SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$	Turn-off Delay Time	$V_{DD} = 15\text{ V}$ $I_D = 20\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 4.5\text{ V}$ (Resistive Load, see fig. 3)		40		ns
t_f	Fall Time			60		ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain Current				20	A
$I_{SDM}(\bullet)$	Source-drain Current (pulsed)				80	A
$V_{SD}(\ast)$	Forward On Voltage	$I_{SD} = 20\text{ A}$ $V_{GS} = 0$			1.2	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 20\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 15\text{ V}$ $T_j = 150\text{ }^\circ\text{C}$ (see test circuit, fig. 5)		T.B.D		ns
Q_{rr}	Reverse Recovery Charge					μC
I_{RRM}	Reverse Recovery Current					A

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

(•) Pulse width limited by safe operating area

Fig. 1: Unclamped Inductive Load Test Circuit

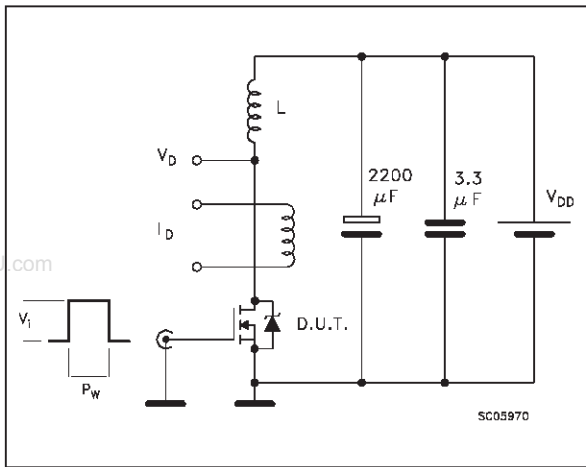


Fig. 2: Unclamped Inductive Waveform

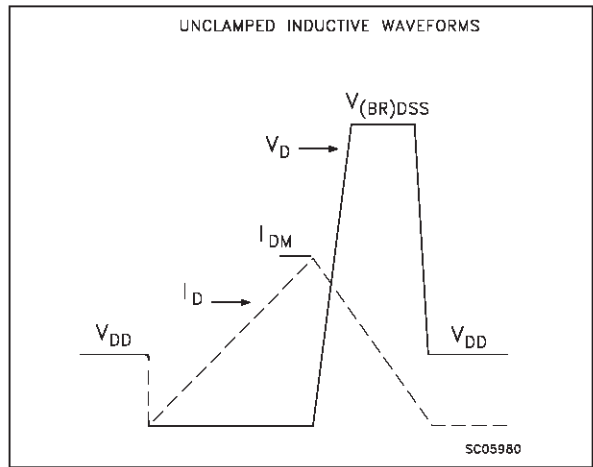


Fig. 3: Switching Times Test Circuits For Resistive Load



Fig. 4: Gate Charge test Circuit

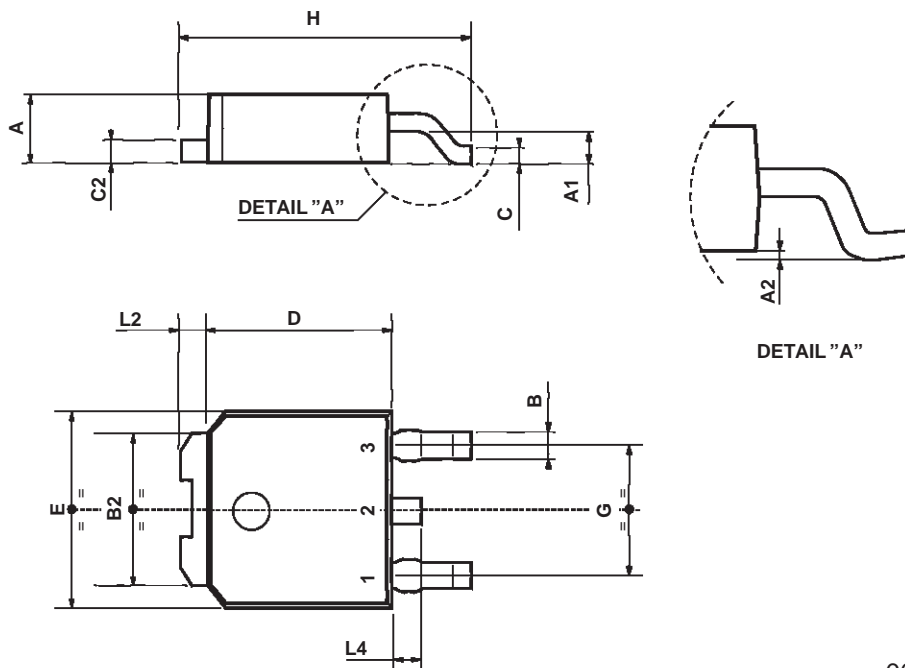


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
B2	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L2		0.8			0.031	
L4	0.6		1	0.023		0.039



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