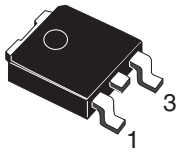
# STD40NF3LL

## N-channel 30V - 0.009Ω - 40A - DPAK
## Low gate charge STripFET™ II Power MOSFET

## General features

| Type | $V_{DSS}$ | $R_{DS(on)}$ | $I_D$ |
|---|---|---|---|
| STD40NF3LL | 30V | <0.011Ω | 40A |

- Logic level device
- Optimal $R_{DS(on)}$ x $Q_g$ trade-off
- Conduction losses reduced
- Switching losses reduced
- Low threshold drive

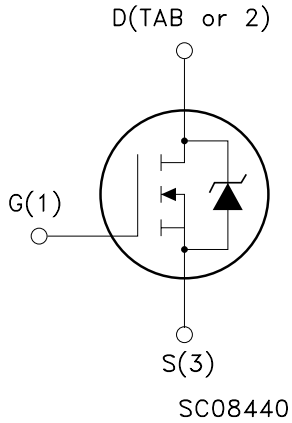



**DPAK**

## Description

This application specific Power MOSFET is the third generation of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows the best trade-off between on-resistance and gate charge. When used as high and low side in buck regulators, it gives the best performance in terms of both conduction and switching losses. This is extremely important for motherboards where fast switching and high efficiency are of paramount importance.

## Internal schematic diagram




## Applications

- Switching application

## Order codes

| Part number | Marking | Package | Packaging |
|---|---|---|---|
| STD40NF3LLT4 | D40NF3LL@ | DPAK | Tape & reel |

# Contents

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source voltage ($V_{GS}$ = 0) | 30 | V |
| $V_{DGR}$ | Drain-gate voltage ($R_{GS}$ = 20 kΩ) | 30 | V |
| $V_{GS}$ | Gate- source voltage | ± 16 | V |
| $I_D$ (1) | Drain current (continuous) at $T_C$ = 25°C | 40 | A |
| $I_D$ | Drain current (continuous) at $T_C$ = 100°C | 28 | A |
| $I_{DM}$ (2) | Drain current (pulsed) | 160 | A |
| $P_{tot}$ | Total dissipation at $T_C$ = 25°C | 80 | W |
| | Derating Factor | 0.53 | W/°C |
| dv/dt (3) | Peak diode recovery voltage slope | 5.5 | V/ns |
| $E_{AS}$ (4) | Single pulse avalanche energy | 850 | mJ |
| $T_{stg}$ | Storage temperature | -55 to 175 | °C |
| $T_j$ | Max. operating junction temperature | | |

1. Current limited by package
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 40A$, di/dt ≤350A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$
4. Starting $T_j$ = 25 °C, $I_D$ = 20A, $V_{DD}$ = 25V

**Table 2. Thermal data**

| | | | |
|---|---|---|---|
| Rthj-case | Thermal resistance junction-case max | 1.88 | °C/W |
| Rthj-amb | Thermal resistance junction-ambient max | 100 | °C/W |
| $T_J$ | Maximum lead temperature for soldering purpose | 300 | °C |

# 2 Electrical characteristics

($T_{CASE}$=25°C unless otherwise specified)

**Table 3. On/off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $I_D$ = 250µA, $V_{GS}$ =0 | 30 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current ($V_{GS}$ = 0) | $V_{DS}$ = max rating<br>$V_{DS}$ = max rating, $T_C$ = 125°C | | | 1<br>10 | µA<br>µA |
| $I_{GSS}$ | Gate-body leakage current ($V_{DS}$ = 0) | $V_{GS}$ = ±16V | | | ±100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250µA | 1 | | | V |
| $R_{DS(on)}$ | Static drain-source on resistance | $V_{GS}$ = 10V, $I_D$ = 20A<br>$V_{GS}$ = 4.5V, $I_D$ = 10A | | 0.0090<br>0.0115 | 0.0110<br>0.0135 | Ω<br>Ω |

**Table 4. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $g_{fs}$ (1) | Forward transconductance | $V_{DS}$ = 15V, $I_D$ = 20A | | 23 | | S |
| $C_{iss}$<br>$C_{oss}$<br>$C_{rss}$ | Input capacitance<br>Output capacitance<br>Reverse transfer capacitance | $V_{DS}$ = 25V, f = 1MHz, $V_{GS}$ = 0 | | 1650<br>540<br>130 | | pF<br>pF<br>pF |
| $t_{d(on)}$<br>$t_r$<br>$t_{d(off)}$<br>$t_f$ | Turn-on delay time<br>Rise time<br>Turn-off delay time<br>Fall time | $V_{DD}$ = 15V, $I_D$ = 20A<br>$R_G$ = 4.7Ω $V_{GS}$ =4.5V<br>(see *Figure 13*) | | 23<br>156<br>27<br>28 | | ns<br>ns<br>ns<br>ns |
| $Q_g$<br>$Q_{gs}$<br>$Q_{gd}$ | Total gate charge<br>Gate-source charge<br>Gate-drain charge | $V_{DD}$ = 15V, $I_D$ = 20A,<br>$V_{GS}$ = 4.5V, $R_G$ = 4.7Ω<br>(see *Figure 14*) | | 24<br>8.5<br>12 | 33 | nC<br>nC<br>nC |

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%.

**Table 5. Source drain diode**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$<br>$I_{SDM}$ (1) | Source-drain current<br>Source-drain current (pulsed) | | | | 40<br>160 | A<br>A |
| $V_{SD}$ (2) | Forward on voltage | $I_{SD}$ = 40A, $V_{GS}$ = 0 | | | 1.3 | V |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{RRM}$ | Reverse recovery time<br>Reverse recovery charge<br>Reverse recovery current | $I_{SD}$ = 40A, di/dt = 100A/µs,<br>$V_{DD}$ = 15V, $T_j$ = 150°C<br>(see *Figure 15*) | | 40<br>50<br>2.5 | | ns<br>nC<br>A |

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

**Figure 1. Safe operating area**

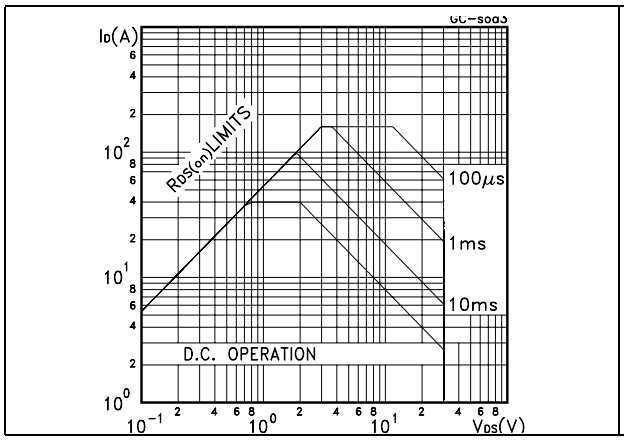



**Figure 2. Thermal impedance**

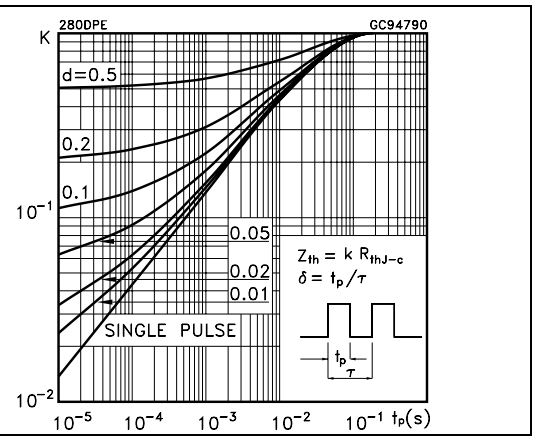



**Figure 3. Output characteristics**

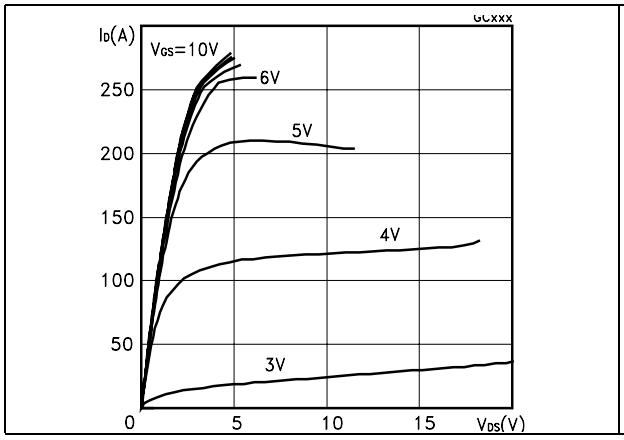



**Figure 4. Transfer characteristics**

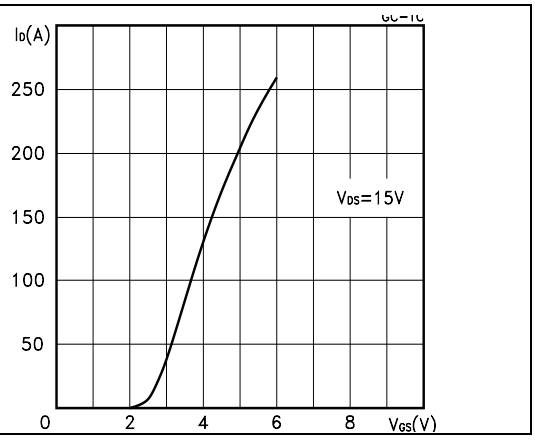



**Figure 5. Transconductance**

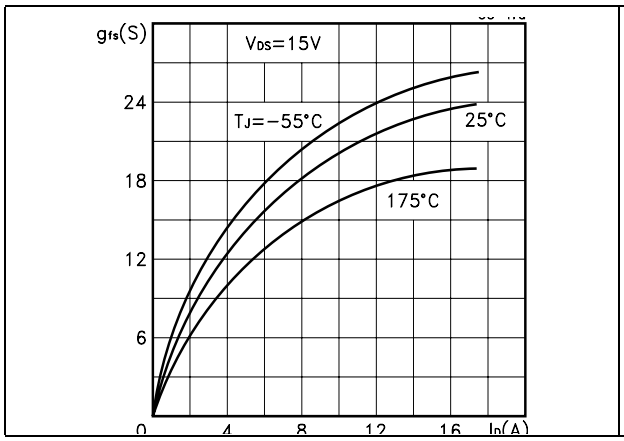



**Figure 6. Static drain-source on resistance**

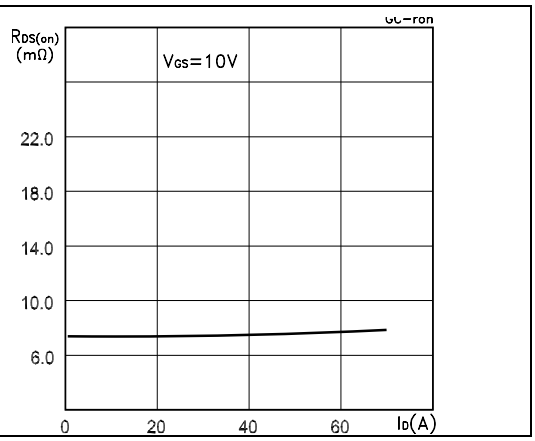


**Figure 7. Gate charge vs. gate-source voltage**

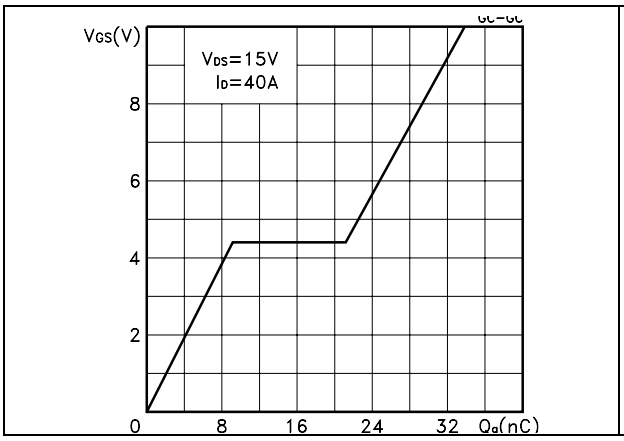



**Figure 8. Capacitance variations**

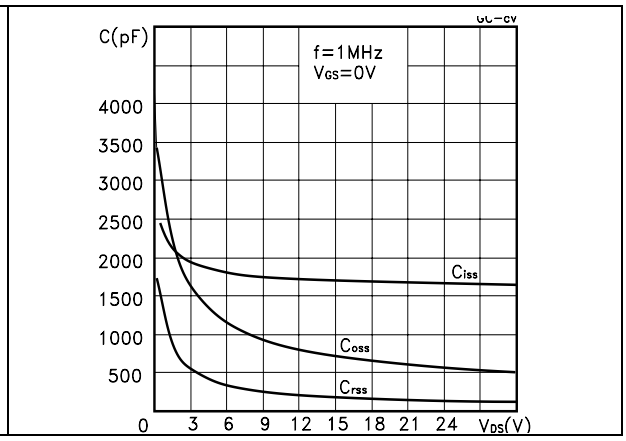



**Figure 9. Normalized gate threshold voltage vs. temperature**

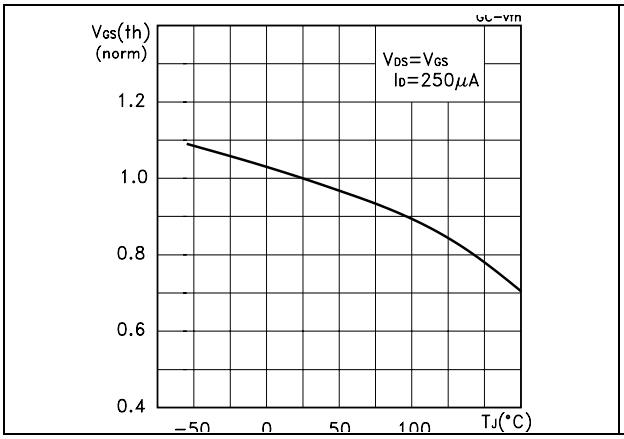



**Figure 10. Normalized on resistance vs. temperature**

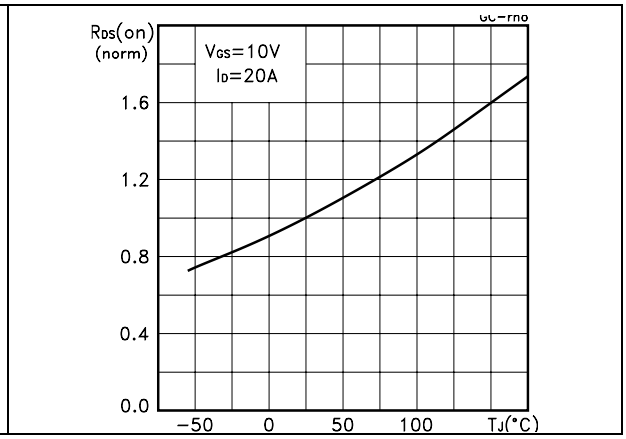



**Figure 11. Source-drain diode forward characteristics**

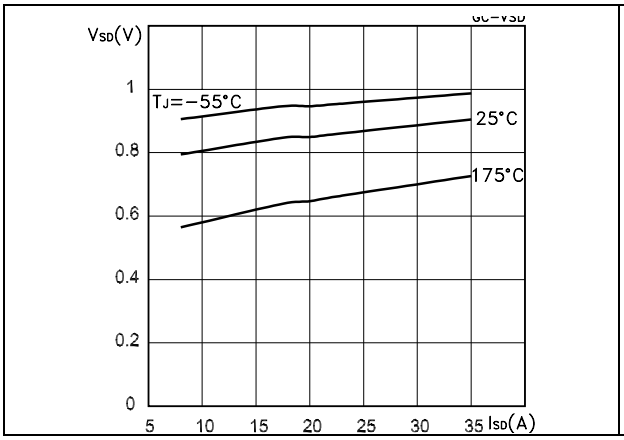
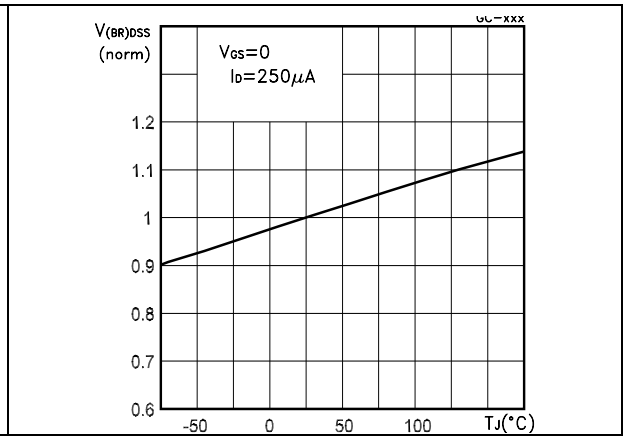



**Figure 12. Normalized breakdown voltage vs. temperature**



# 3 Test circuit

**Figure 13. Switching times test circuit for resistive load**

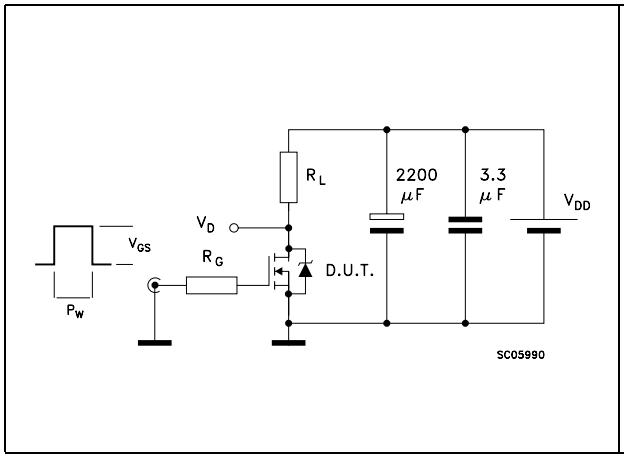



**Figure 14. Gate charge test circuit**

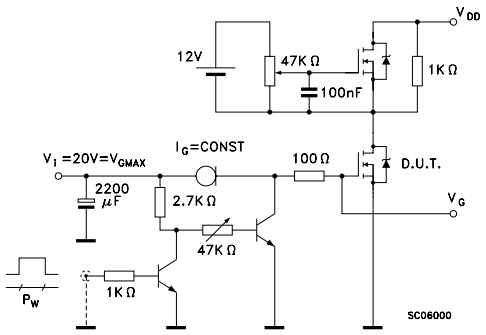



**Figure 15. Test circuit for inductive load switching and diode recovery times**

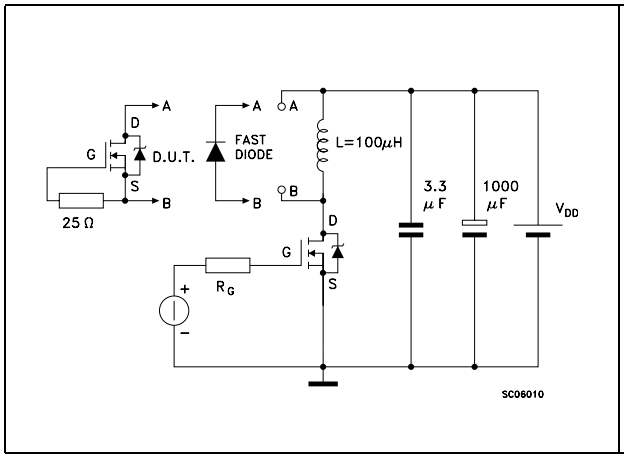



**Figure 16. Unclamped Inductive load test circuit**

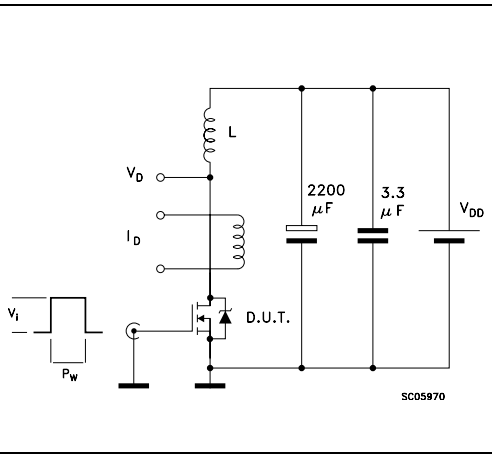



**Figure 17. Unclamped inductive waveform**

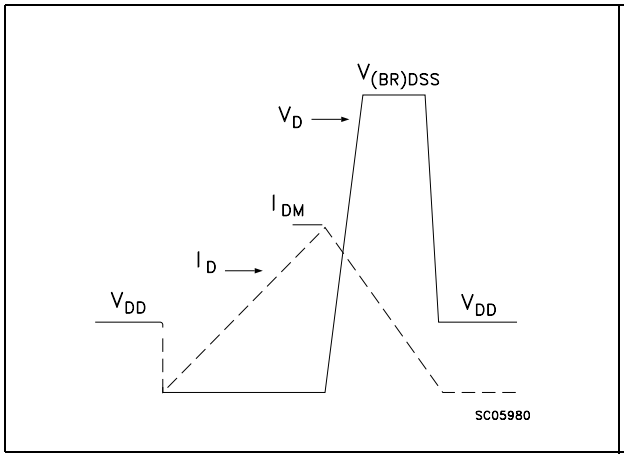
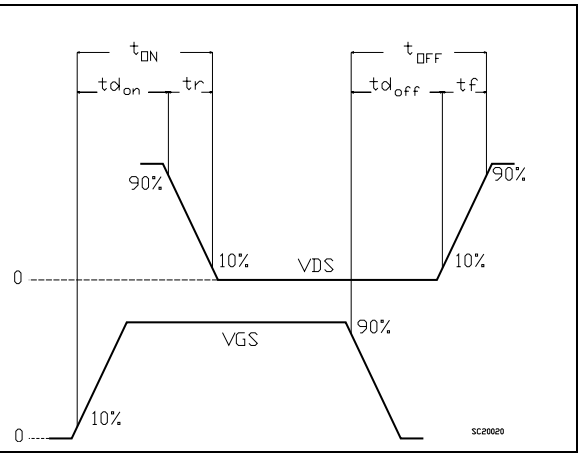



**Figure 18. Switching time waveform**

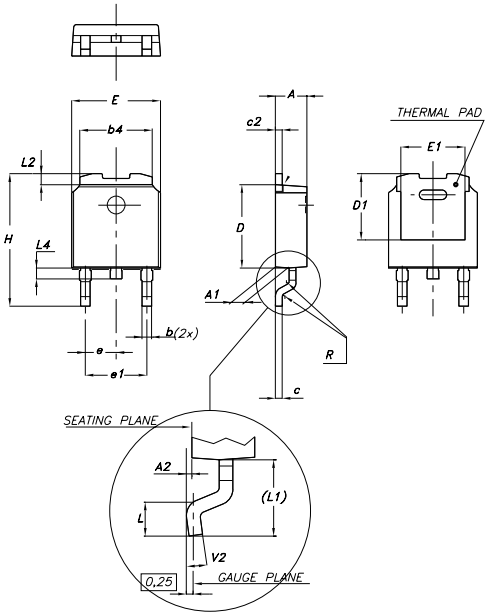


# 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

## DPAK MECHANICAL DATA

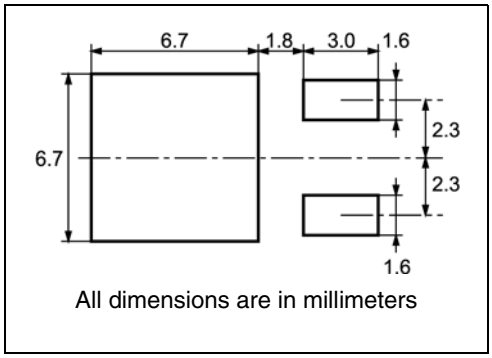
| DIM. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | 2.2 | | 2.4 | 0.086 | | 0.094 |
| A1 | 0.9 | | 1.1 | 0.035 | | 0.043 |
| A2 | 0.03 | | 0.23 | 0.001 | | 0.009 |
| B | 0.64 | | 0.9 | 0.025 | | 0.035 |
| b4 | 5.2 | | 5.4 | 0.204 | | 0.212 |
| C | 0.45 | | 0.6 | 0.017 | | 0.023 |
| C2 | 0.48 | | 0.6 | 0.019 | | 0.023 |
| D | 6 | | 6.2 | 0.236 | | 0.244 |
| D1 | | 5.1 | | | 0.200 | |
| E | 6.4 | | 6.6 | 0.252 | | 0.260 |
| E1 | | 4.7 | | | 0.185 | |
| e | | 2.28 | | | 0.090 | |
| e1 | 4.4 | | 4.6 | 0.173 | | 0.181 |
| H | 9.35 | | 10.1 | 0.368 | | 0.397 |
| L | 1 | | | 0.039 | | |
| (L1) | | 2.8 | | | 0.110 | |
| L2 | | 0.8 | | | 0.031 | |
| L4 | 0.6 | | 1 | 0.023 | | 0.039 |
| R | | 0.2 | | | 0.008 | |
| V2 | 0° | | 8° | 0° | | 8° |




0068772-F

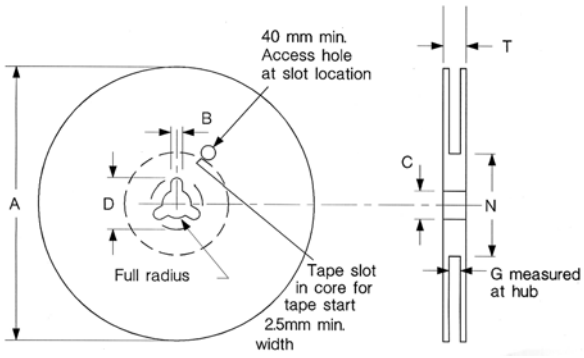
# 5 Packing mechanical data

### DPAK FOOTPRINT




All dimensions are in millimeters

### TAPE AND REEL SHIPMENT



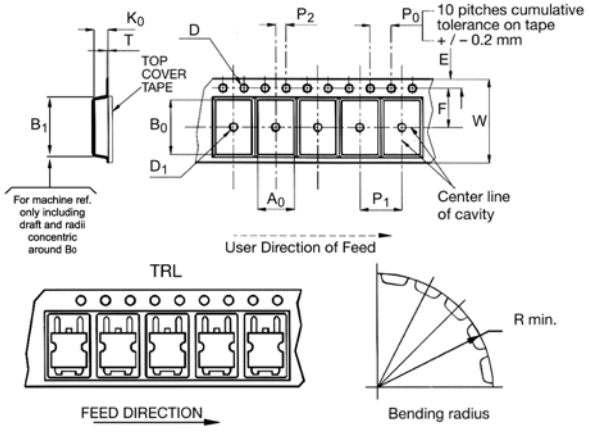

REEL MECHANICAL DATA

| DIM. | mm | | inch | |
|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. |
| A | | 330 | | 12.992 |
| B | 1.5 | | 0.059 | |
| C | 12.8 | 13.2 | 0.504 | 0.520 |
| D | 20.2 | | 0.795 | |
| G | 16.4 | 18.4 | 0.645 | 0.724 |
| N | 50 | | 1.968 | |
| T | | 22.4 | | 0.881 |

| BASE QTY | BULK QTY |
|---|---|
| 2500 | 2500 |

TAPE MECHANICAL DATA

| DIM. | mm | | inch | |
|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. |
| A0 | 6.8 | 7 | 0.267 | 0.275 |
| B0 | 10.4 | 10.6 | 0.409 | 0.417 |
| B1 | | 12.1 | | 0.476 |
| D | 1.5 | 1.6 | 0.059 | 0.063 |
| D1 | 1.5 | | 0.059 | |
| E | 1.65 | 1.85 | 0.065 | 0.073 |
| F | 7.4 | 7.6 | 0.291 | 0.299 |
| K0 | 2.55 | 2.75 | 0.100 | 0.108 |
| P0 | 3.9 | 4.1 | 0.153 | 0.161 |
| P1 | 7.9 | 8.1 | 0.311 | 0.319 |
| P2 | 1.9 | 2.1 | 0.075 | 0.082 |
| R | 40 | | 1.574 | |
| W | 15.7 | 16.3 | 0.618 | 0.641 |



# 6 Revision history

Table 6. Revision history

| Date | Revision | Changes |
|---|---|---|
| 21-Jun-2004 | 3 | New datasheet according to PCN DSG/CT/2C13<br>marking:D40NF3LL@ |
| 11-Jul-2006 | 4 | New template, no content change |
| 20-Feb-2007 | 5 | Typo mistake on page 1 |

**Please Read Carefully:**

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

**UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

**UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER’S OWN RISK.**

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.



STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

**www.st.com**