



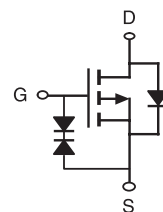
P-Channel Logic Level Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY

V _{DSS}	I _D	R _{DS(ON)} (mΩ) Max
-40V	-19A	48 @ V _{GS} =10V
		78 @ V _{GS} =4.5V

FEATURES

- Super high dense cell design for low R_{DS(ON)}.
- Rugged and reliable.
- Surface Mount Package.
- ESD Protected.



ABSOLUTE MAXIMUM RATINGS (T_A=25°C unless otherwise noted)

Symbol	Parameter		Limit	Units
V _{DS}	Drain-Source Voltage		-40	V
V _{GS}	Gate-Source Voltage		±20	V
I _D	Drain Current-Continuous ^a	T _C =25°C	-19	A
		T _C =70°C	-15	A
I _{DM}	-Pulsed ^b		-58	A
E _{AS}	Sigle Pulse Avalanche Energy ^d		16	mJ
P _D	Maximum Power Dissipation ^a	T _C =25°C	32	W
		T _C =70°C	20	W
T _J , T _{STG}	Operating Junction and Storage Temperature Range		-55 to 150	°C

THERMAL CHARACTERISTICS

R _{θJC}	Thermal Resistance, Junction-to-Case ^a	4	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient ^a	50	°C/W

STU/D413S

Ver 1.0

ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V , I _D =-250uA	-40			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-32V , V _{GS} =0V			1	uA
I _{GSS}	Gate-Body Leakage Current	V _{GS} = ±20V , V _{DS} =0V			±10	uA
ON CHARACTERISTICS						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250uA	-1	-1.8	-3	V
R _{DS(ON)}	Drain-Source On-State Resistance	V _{GS} =-10V , I _D =-9.5A		38	48	m ohm
		V _{GS} =-4.5V , I _D =-7.5A		58	78	m ohm
g _{FS}	Forward Transconductance	V _{DS} =-10V , I _D =-9.5A		10		S
DYNAMIC CHARACTERISTICS [°]						
C _{ISS}	Input Capacitance	V _{DS} =-20V,V _{GS} =0V f=1.0MHz		895		pF
C _{OSS}	Output Capacitance			138		pF
C _{RSS}	Reverse Transfer Capacitance			67		pF
SWITCHING CHARACTERISTICS [°]						
t _{D(ON)}	Turn-On Delay Time	V _{DD} =-20V I _D =-1.0A V _{GS} =-10V R _{GEN} =3.3 ohm		14		ns
t _r	Rise Time			14		ns
t _{D(OFF)}	Turn-Off Delay Time			54		ns
t _f	Fall Time			10		ns
Q _g	Total Gate Charge	V _{DS} =-20V,I _D =-9.5A,V _{GS} =-10V		14.5		nC
		V _{DS} =-20V,I _D =-9.5A,V _{GS} =-4.5V		7		nC
Q _{gs}	Gate-Source Charge	V _{DS} =-20V,I _D =-9.5A, V _{GS} =-10V		2.1		nC
Q _{gd}	Gate-Drain Charge			3.4		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I _S	Maximum Continuous Drain-Source Forward Current				-2.0	A
V _{SD}	Diode Forward Voltage ^b	V _{GS} =0V,I _S = -2.0A		-0.77	-1.3	V

Notes

- Surface Mounted on FR4 Board, t ≤ 10sec.
- Pulse Test: Pulse Width ≤ 300us, Duty Cycle ≤ 2%.
- Guaranteed by design, not subject to production testing.
- Starting T_J=25°C, L=0.5mH, V_{DD} = 20V .(See Figure13)

Aug,08,2008

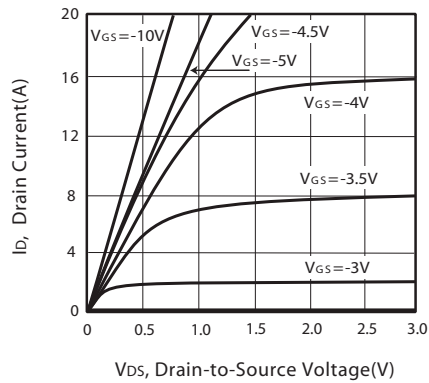


Figure 1. Output Characteristics

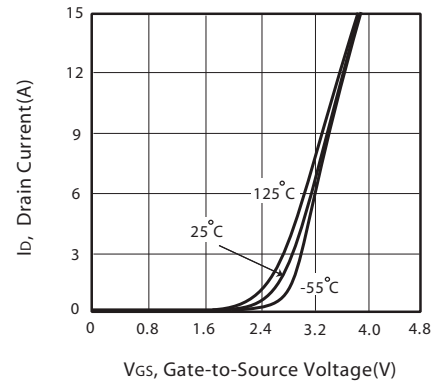


Figure 2. Transfer Characteristics

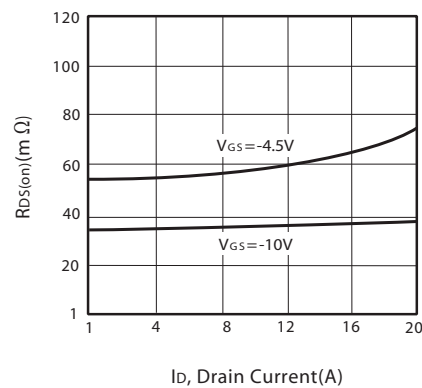


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

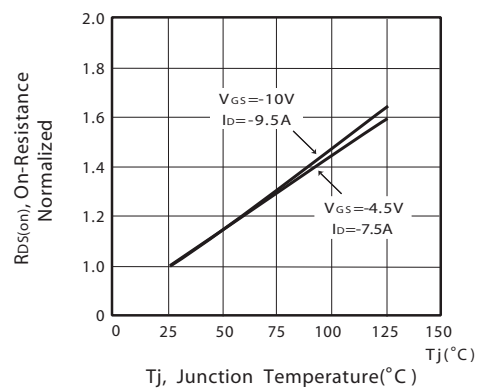


Figure 4. On-Resistance Variation with Drain Current and Temperature

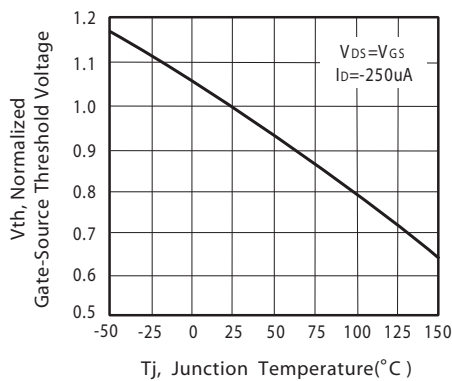


Figure 5. Gate Threshold Variation with Temperature

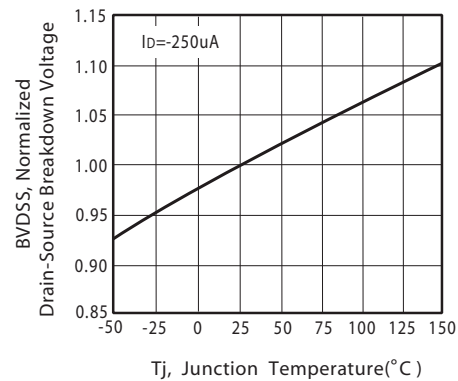


Figure 6. Breakdown Voltage Variation with Temperature

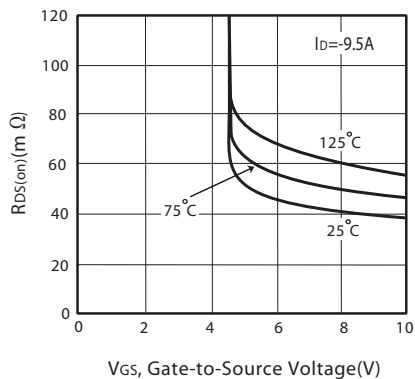


Figure 7. On-Resistance vs. Gate-Source Voltage

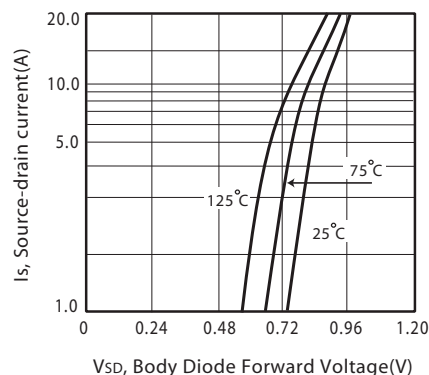


Figure 8. Body Diode Forward Voltage Variation with Source Current

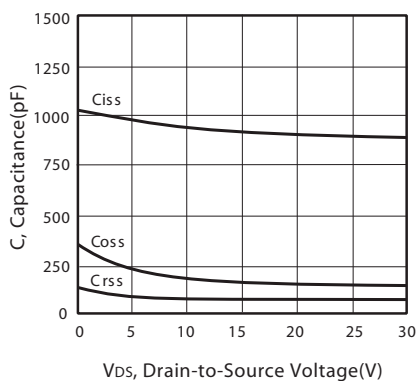


Figure 9. Capacitance

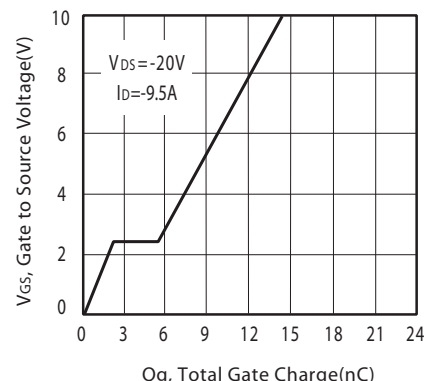


Figure 10. Gate Charge

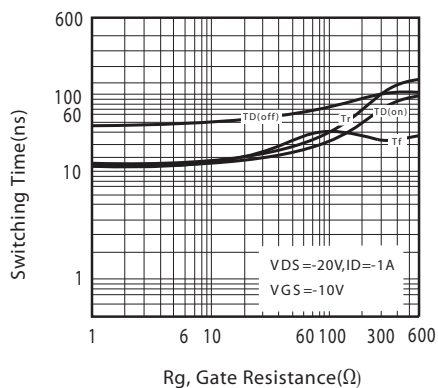


Figure 11. switching characteristics

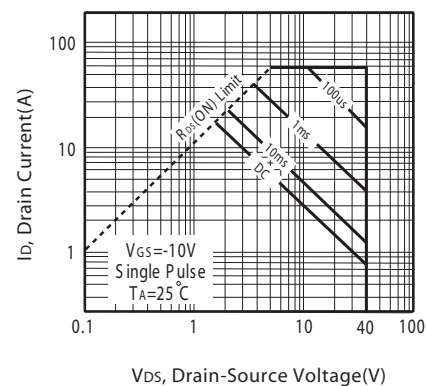
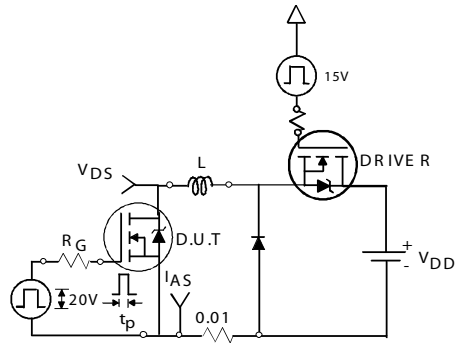
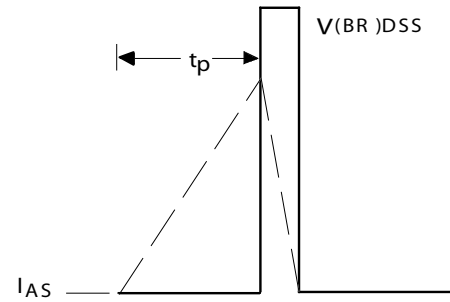


Figure 12. Maximum Safe Operating Area



Unclamped Inductive Test Circuit

Figure 13a.



Unclamped Inductive Waveforms

Figure 13b.

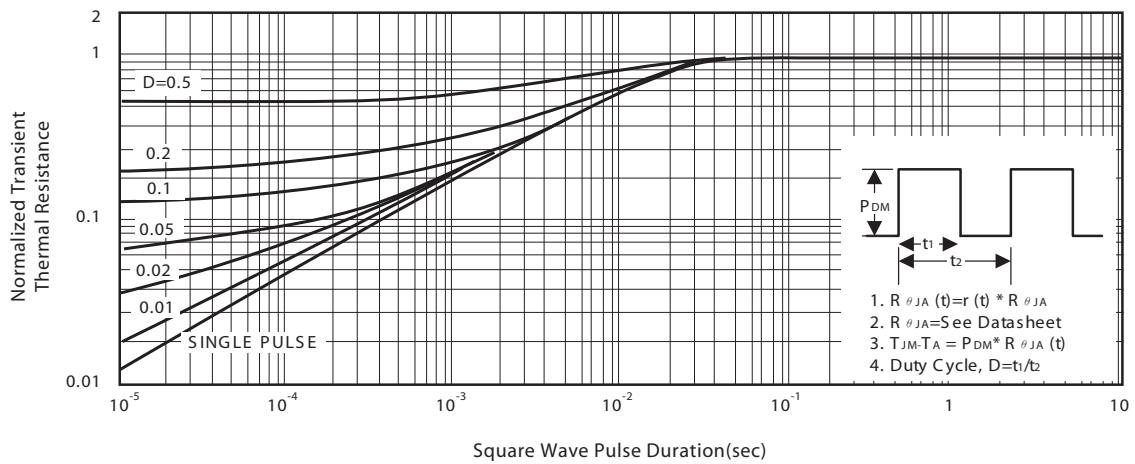
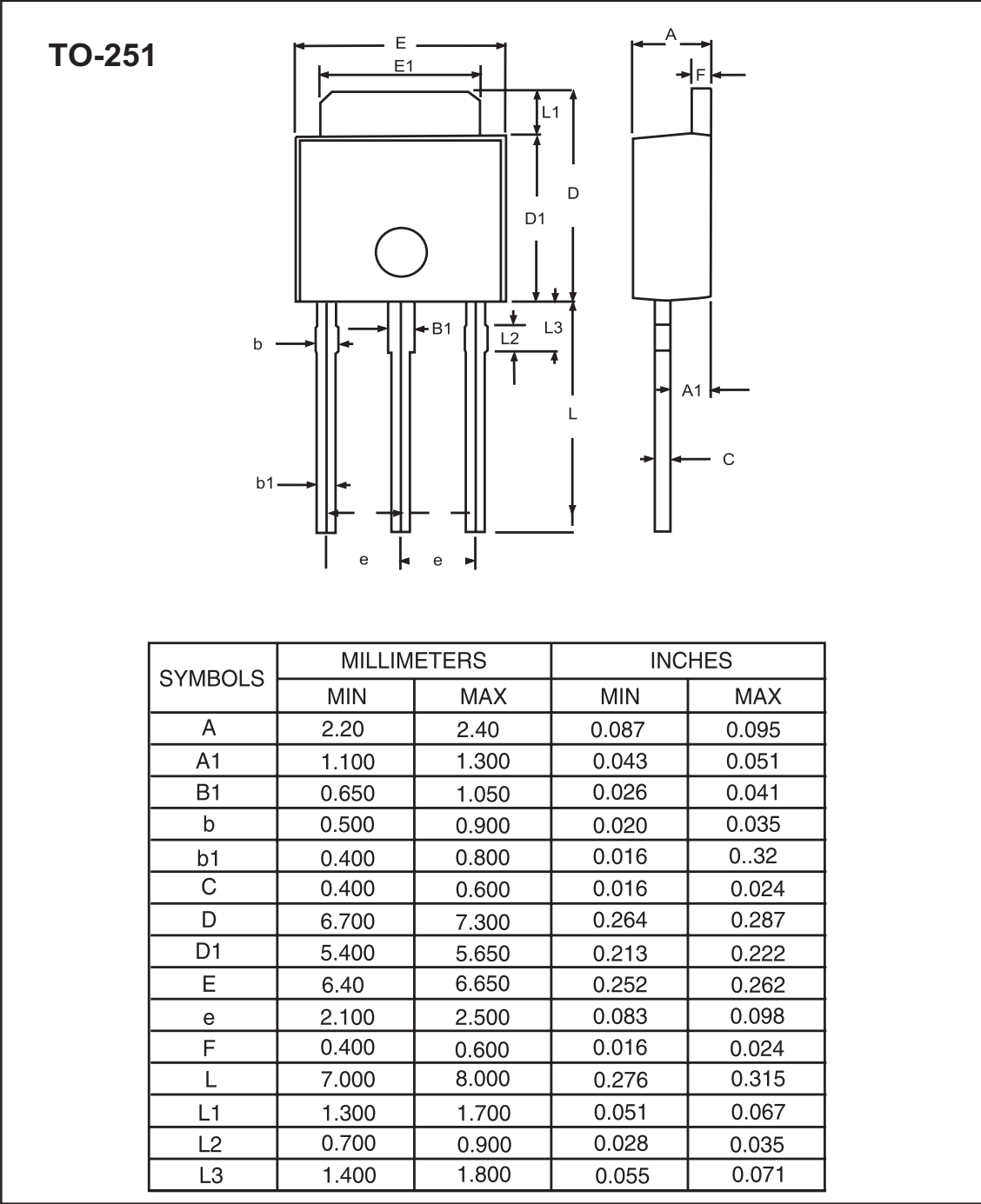


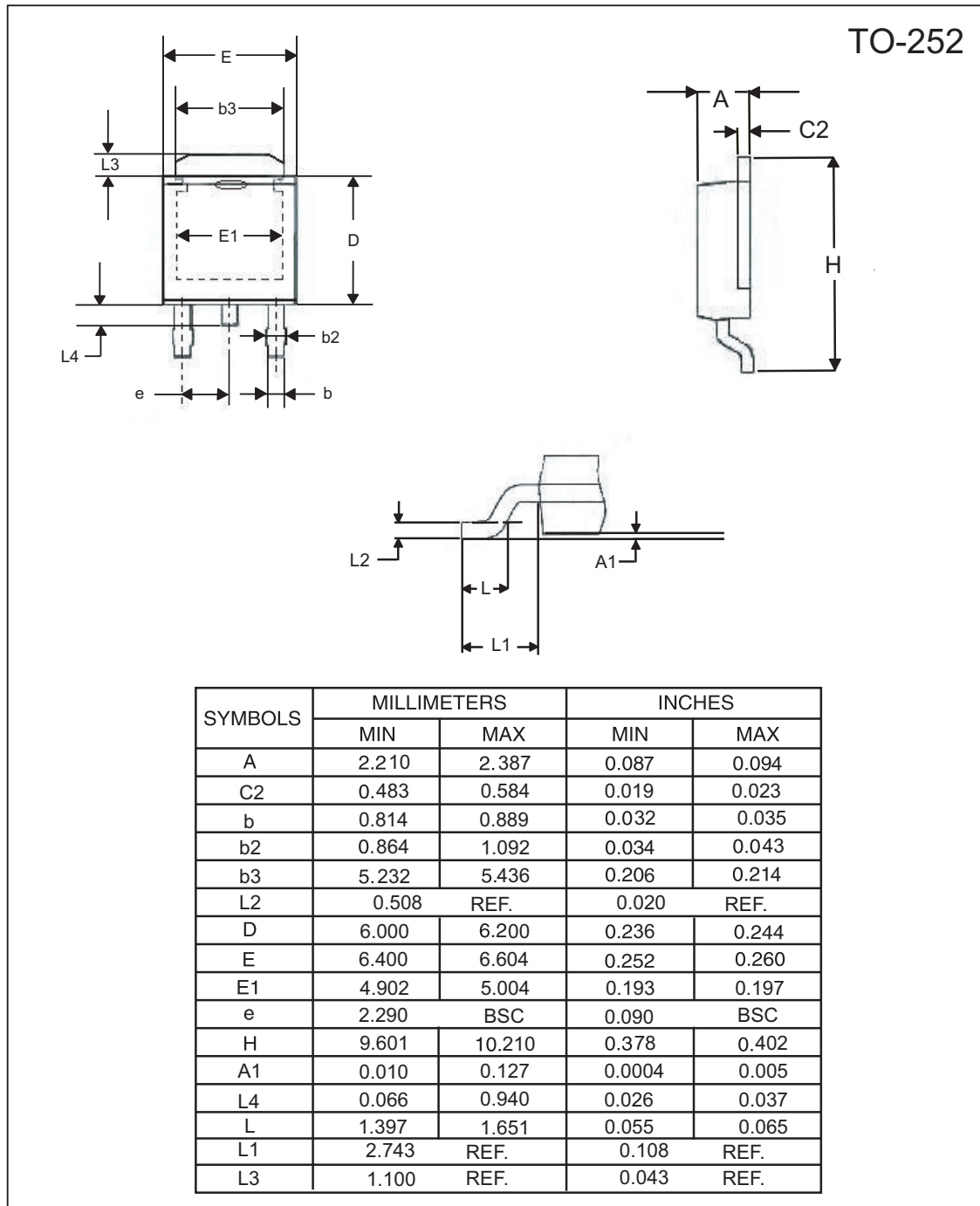
Figure 14. Normalized Thermal Transient Impedance Curve

PACKAGE OUTLINE DIMENSIONS



STU/D413S

Ver 1.0



Aug,08,2008

