



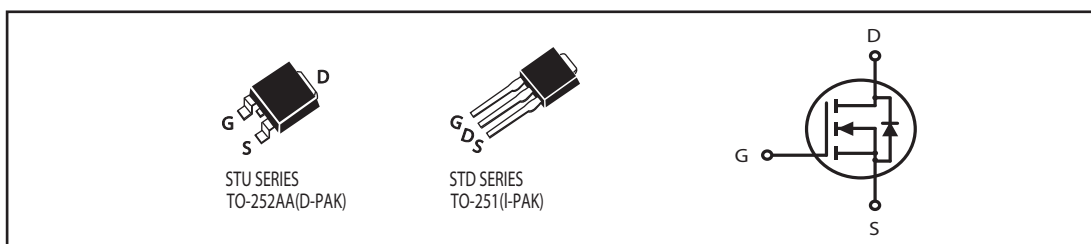
N-Channel Logic Level Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY

V _{DSS}	I _D	R _{DS(ON)} (mΩ) Max
40V	50A	9 @ V _{GS} = 10V

FEATURES

- Super high dense cell design for low R_{DS(ON)}.
- Rugged and reliable.
- TO-252 and TO-251 Package.



ABSOLUTE MAXIMUM RATINGS (TC=25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	40	V
Gate-Source Voltage	V _{GS}	±20	V
Drain Current-Continuous ^a @Ta	I _D	50	A
25°C			
-Pulsed ^b	I _{DM}	100	A
Drain-Source Diode Forward Current ^a	I _S	20	A
Avalanche Current ^c	I _{AS}	23	A
Avalanche Energy ^c	E _{AS}	130	mJ
Maximum Power Dissipation ^a	P _D	50	W
Ta=25°C			
Operating Junction and Storage Temperature Range	T _J , T _{STG}	-55 to 175	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Case	R _{θJC}	3	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	50	°C/W

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ELECTRICAL CHARACTERISTICS ($T_C=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	40			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=32V, V_{GS}=0V$			1	μA
Gate-Body Leakage	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$			± 100	nA
ON CHARACTERISTICS ^a						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.25	1.6	3	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=10A$		7	9	m Ω
		$V_{GS}=4.5V, I_D=5A$		9	11	m Ω
On-State Drain Current	$I_{D(ON)}$	$V_{DS}=10V, V_{GS}=10V$	30			A
Forward Transconductance	g_{FS}	$V_{DS}=10V, I_D=10A$		28		S
DYNAMIC CHARACTERISTICS ^b						
Input Capacitance	C_{ISS}	$V_{DS}=15V, V_{GS}=0V$ $f=1.0MHz$		1130		pF
Output Capacitance	C_{OSS}			240		pF
Reverse Transfer Capacitance	C_{RSS}			145		pF
SWITCHING CHARACTERISTICS ^b						
Turn-On Delay Time	$t_{D(ON)}$	$V_{DD}=15V$ $I_D=10A$ $V_{GS}=10V$ $R_{GEN}=3.3\Omega$		18		ns
Rise Time	t_r			22		ns
Turn-Off Delay Time	$t_{D(OFF)}$			61		ns
Fall Time	t_f			9.6		ns
Total Gate Charge	Q_g	$V_{DS}=15V, I_D=10A, V_{GS}=10V$		23.5		nC
		$V_{DS}=15V, I_D=10A, V_{GS}=4.5V$		11.5		nC
Gate-Source Charge	Q_{gs}	$V_{DS}=15V, I_D=10A$ $V_{GS}=10V$		2.7		nC
Gate-Drain Charge	Q_{gd}			3.2		nC

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ELECTRICAL CHARACTERISTICS ($T_C=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS ^a						
Diode Forward Voltage	V_{SD}	$V_{GS} = 0V, I_S = 20A$		0.91	1.3	V

Notes

a. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

c. Starting $T_J=25^\circ\text{C}$, $L=0.5\text{ mH}$, $R_G=25\Omega$, $I_{AS}=23A$, $V_{DD}\leq V_{(BR)DSS}$ (See Figure13)

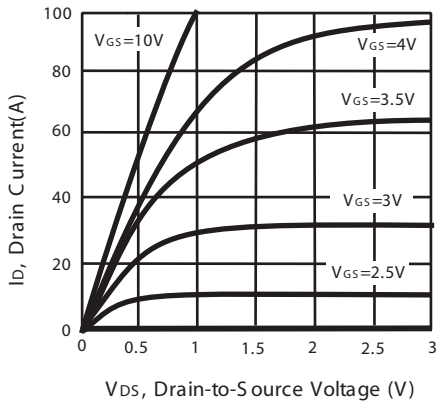


Figure 1. Output Characteristics

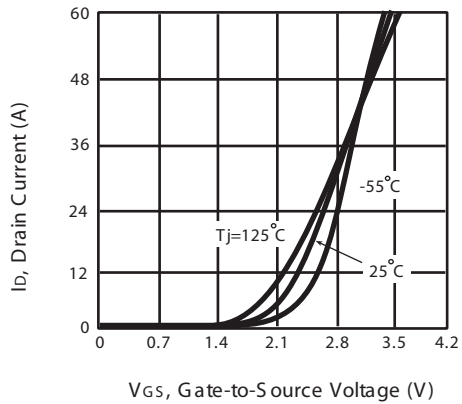


Figure 2. Transfer Characteristics

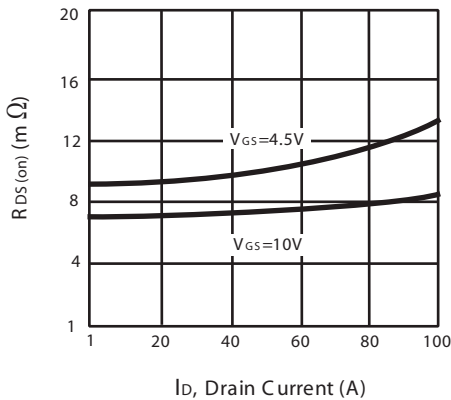


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

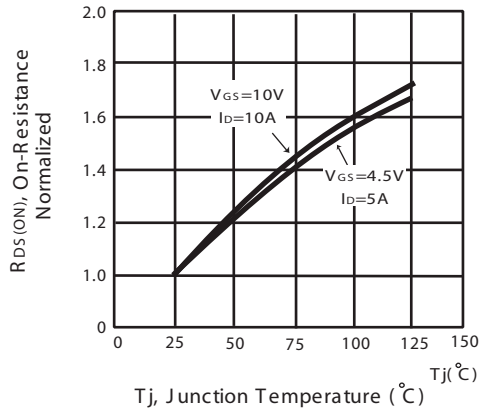


Figure 4. On-Resistance Variation with Drain Current and Temperature

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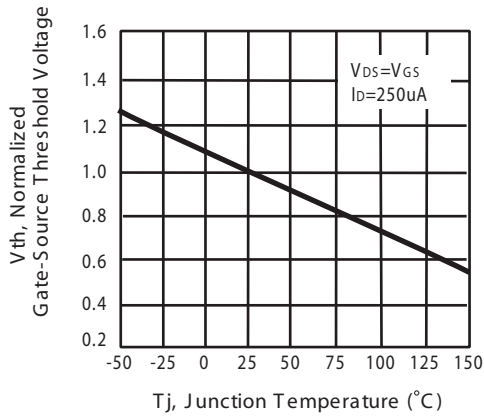


Figure 5. Gate Threshold Variation with Temperature

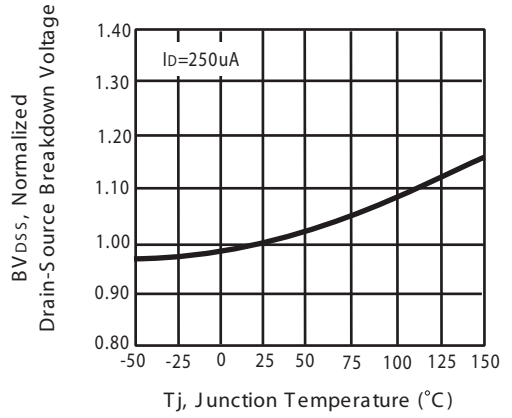


Figure 6. Breakdown Voltage Variation with Temperature

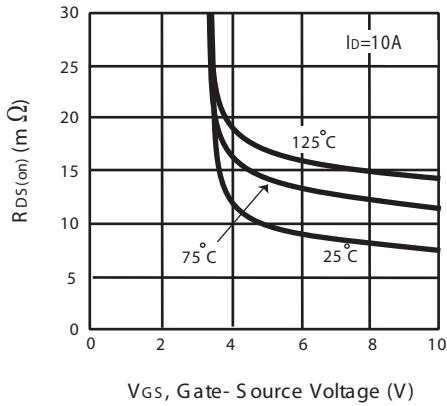


Figure 7. On-Resistance vs. Gate-Source Voltage

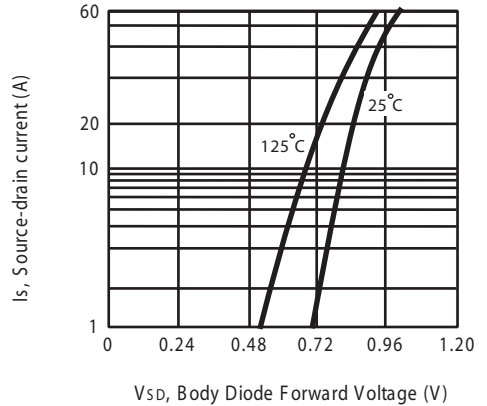


Figure 8. Body Diode Forward Voltage Variation with Source Current

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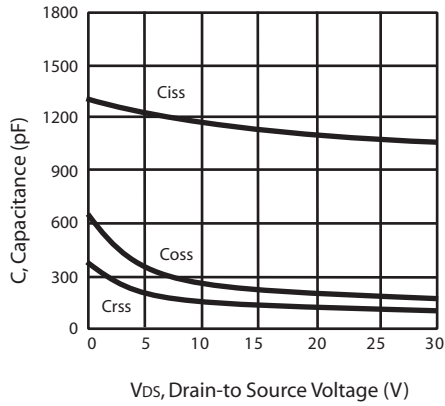


Figure 9. Capacitance

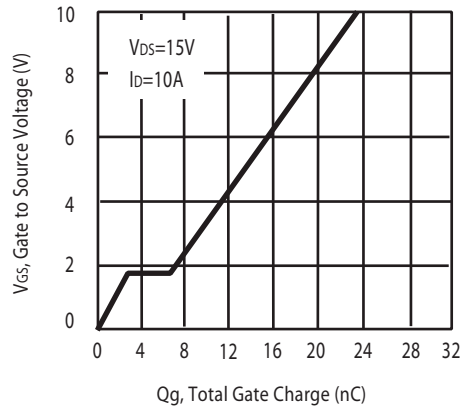


Figure 10. Gate Charge

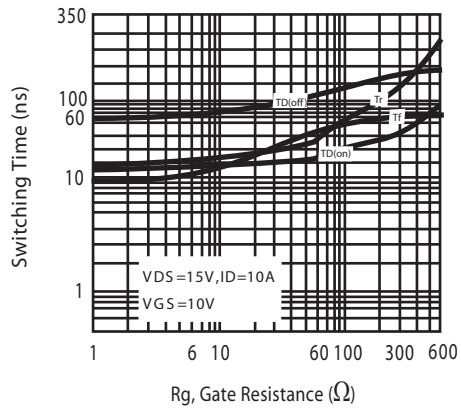


Figure 11. switching characteristics

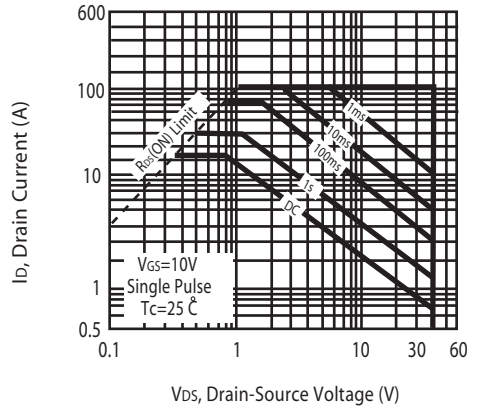


Figure 12. Maximum Safe Operating Area