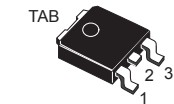
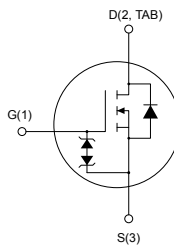



## Automotive-grade N-channel 950 V, 0.95 $\Omega$ typ., 9 A MDmesh K5 Power MOSFET in a DPAK package


**DPAK**


AM01476v1\_tab

### Features

Order code	$V_{DS}$	$R_{DS(on)max.}$	$I_D$	$P_{TOT}$
STD7N95K5AG	950 V	1.25 $\Omega$	9 A	110 W

- AEC-Q101 qualified 
- Industry's lowest  $R_{DS(on)}$  x area
- Industry's best FoM (figure of merit)
- Ultra-low gate charge
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

This very high voltage N-channel Power MOSFET is designed using MDmesh K5 technology based on an innovative proprietary vertical structure. The result is a dramatic reduction in on-resistance and ultra-low gate charge for applications requiring superior power density and high efficiency.



#### Product status link

[STD7N95K5AG](#)

#### Product summary <sup>(1)</sup>

<b>Order code</b>	STD7N95K5AG
<b>Marking</b>	7N95K5
<b>Package</b>	DPAK
<b>Packing</b>	Tape and reel

1. The HTRB test was performed at 80%  $V_{(BR)DSS}$  in compliance with AEC-Q101 rev. C. All the other tests were performed according to rev. D.

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V <sub>GS</sub>	Gate- source voltage	±30	V
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 25 °C	9	A
I <sub>D</sub>	Drain current (continuous) at T <sub>C</sub> = 100 °C	6	A
I <sub>DM</sub> <sup>(1)</sup>	Drain current (pulsed)	13	A
P <sub>TOT</sub>	Total power dissipation at T <sub>C</sub> = 25 °C	110	W
I <sub>AR</sub>	Avalanche current, repetitive or not repetitive (pulse width limited by T <sub>J</sub> max.)	3	A
E <sub>AS</sub>	Single pulse avalanche energy (starting T <sub>J</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	90	mJ
dv/dt <sup>(2)</sup>	Peak diode recovery voltage slope	4.5	V/ns
dv/dt <sup>(3)</sup>	MOSFET dv/dt ruggedness	50	V/ns
T <sub>J</sub>	Operating junction temperature range	-55 to 150	°C
T <sub>stg</sub>	Storage temperature range		

1. Pulse width limited by safe operating area.
2.  $I_{SD} \leq 9 \text{ A}$ ,  $di/dt \leq 100 \text{ A}/\mu\text{s}$ ,  $V_{DS(peak)} \leq V_{(BR)DSS}$ .
3.  $V_{DS} \leq 760 \text{ V}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
R <sub>thJC</sub>	Thermal resistance, junction-to-case	1.15	°C/W
R <sub>thJB</sub> <sup>(1)</sup>	Thermal resistance, junction-to-board	50	°C/W

1. When mounted on 1 inch<sup>2</sup> FR-4 board, 2 oz Cu.

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ }^{\circ}\text{C}$  unless otherwise specified)

**Table 3. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 1\text{ mA}$	950			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 950\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 950\text{ V}$ , $T_c = 125\text{ }^{\circ}\text{C}^{(1)}$			50	$\mu\text{A}$
$I_{GSS}$	Gate body leakage current	$V_{DS} = 0$ , $V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 3\text{ A}$		0.95	1.25	$\Omega$

1. Defined by design, not subject to production test.

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{GS} = 0\text{ V}$ , $V_{DS} = 100\text{ V}$ , $f = 1\text{ MHz}$	-	430	-	pF
$C_{oss}$	Output capacitance		-	36	-	pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{GS} = 0\text{ V}$ , $V_{DS} = 0\text{ to }760\text{ V}$	-	52	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	19	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ , $I_D = 0\text{ A}$	-	7	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 760\text{ V}$ , $I_D = 6\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ , (see Figure 15. Test circuit for gate charge behavior)	-	9.6	-	nC
$Q_{gs}$	Gate-source charge		-	3.2	-	nC
$Q_{gd}$	Gate-drain charge		-	4.4	-	nC

- $C_{o(tr)}$  is a constant capacitance value that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- $C_{o(er)}$  is a constant capacitance value that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 475\text{ V}$ , $I_D = 3\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	13	-	ns
$t_r$	Rise time		-	11	-	ns
$t_{d(off)}$	Turn-off delay time		-	30	-	ns
$t_f$	Fall time		-	18	-	ns

**Table 6. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		9	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		13	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 6\text{ A}, V_{GS} = 0\text{ V}$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 6\text{ A}, V_{DD} = 60\text{ V}$	-	420		ns
$Q_{rr}$	Reverse recovery charge	$di/dt = 100\text{ A}/\mu\text{s}$ , (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	4.8		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	17		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 6\text{ A}, V_{DD} = 60\text{ V}$	-	620		ns
$Q_{rr}$	Reverse recovery charge	$di/dt = 100\text{ A}/\mu\text{s}, T_j = 150\text{ }^\circ\text{C}$	-	6.7		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	14.5		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 $\mu\text{s}$ , duty cycle 1.5%

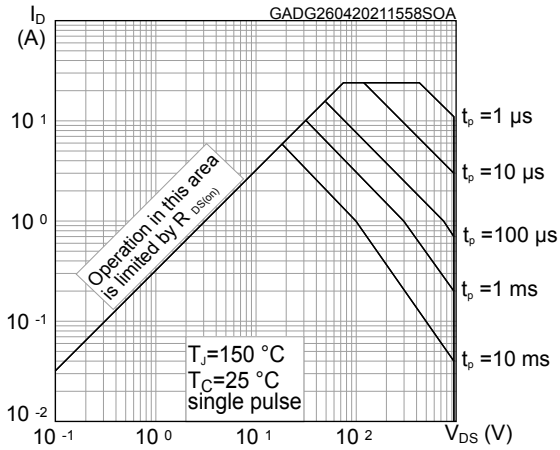
**Table 7. Gate-source Zener diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}, I_D = 0\text{ A}$	$\pm 30$	-	-	V

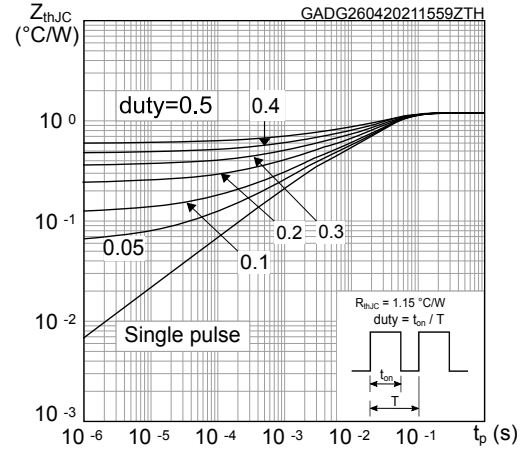
The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

## 2.1 Electrical characteristics (curves)

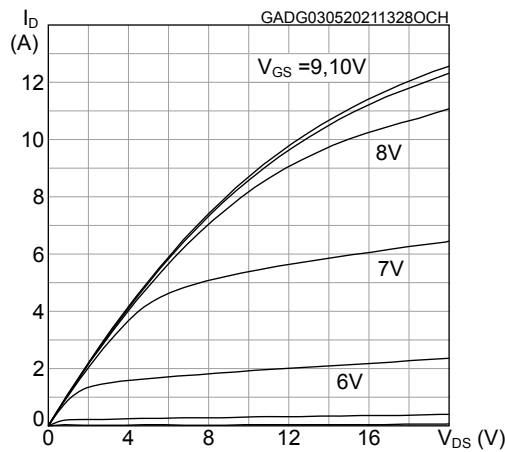
**Figure 1. Safe operating area**



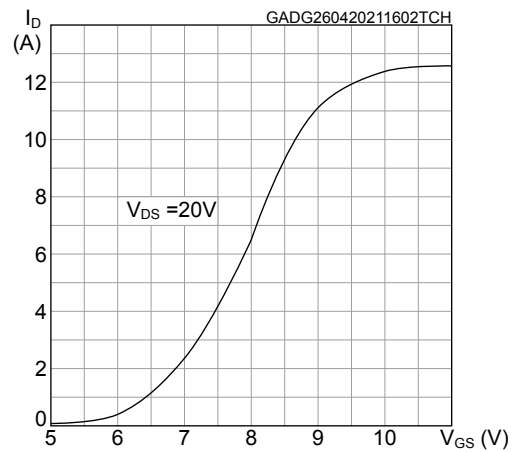
**Figure 2. Maximum transient thermal impedance**



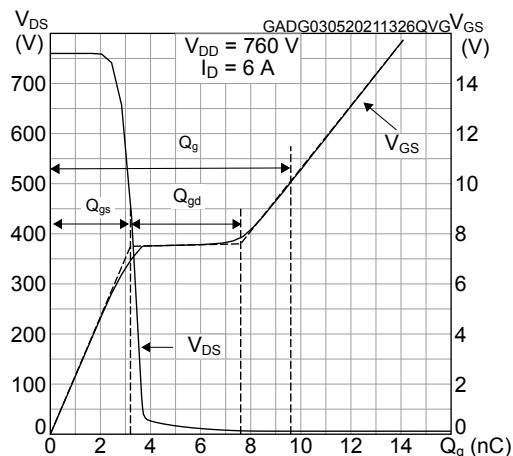
**Figure 3. Typical output characteristics**



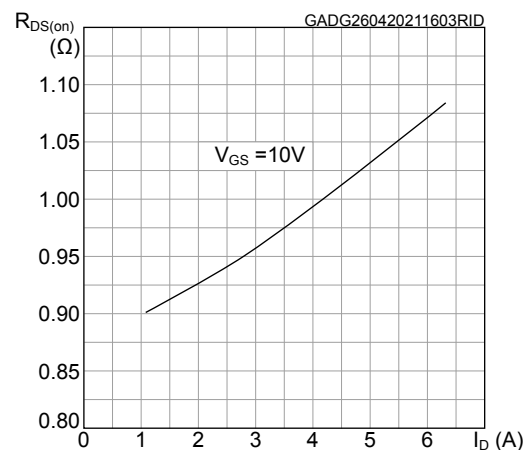
**Figure 4. Typical transfer characteristics**



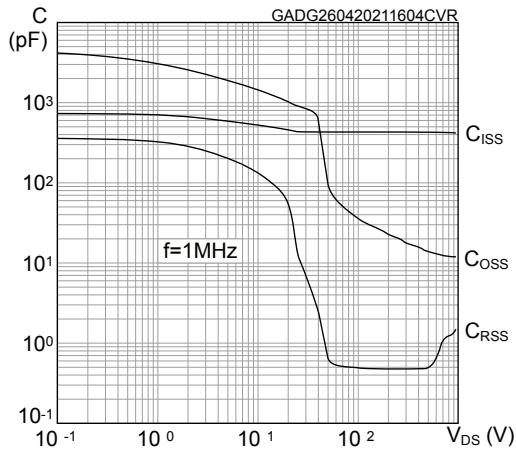
**Figure 5. Typical gate charge characteristics**



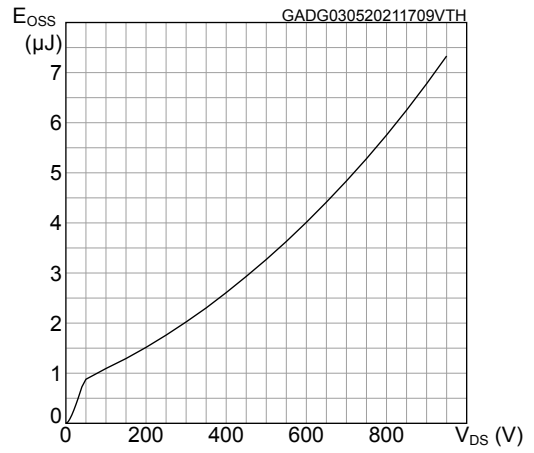
**Figure 6. Typical drain-source on-resistance**



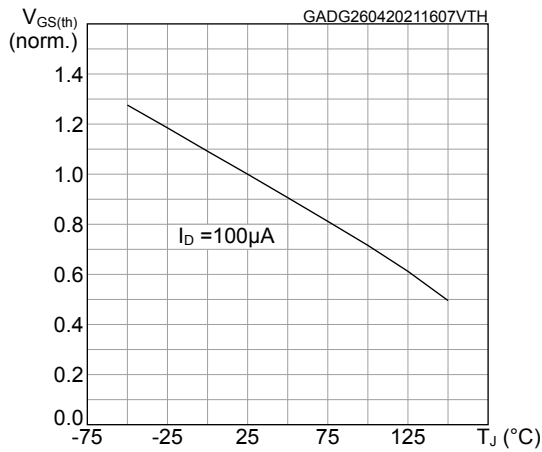
**Figure 7. Typical capacitance characteristics**



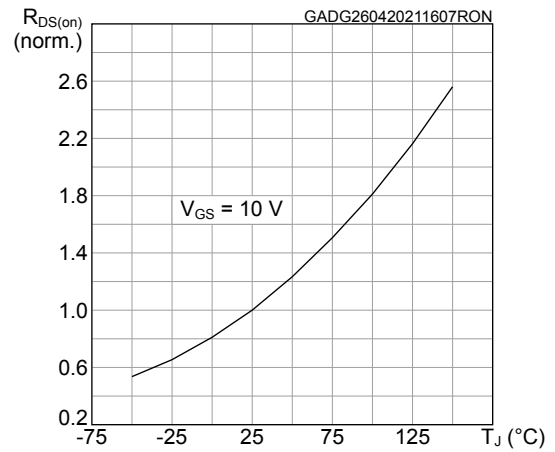
**Figure 8. Typical output capacitance stored energy**



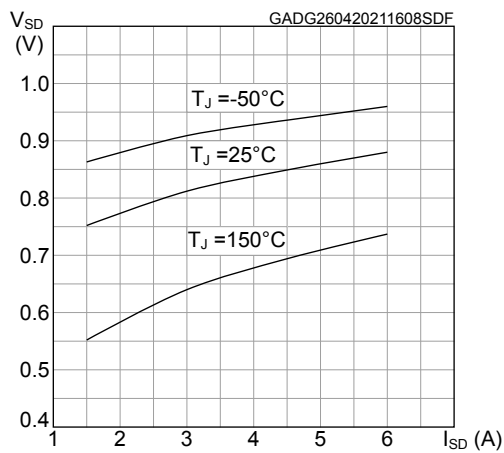
**Figure 9. Normalized gate threshold vs temperature**



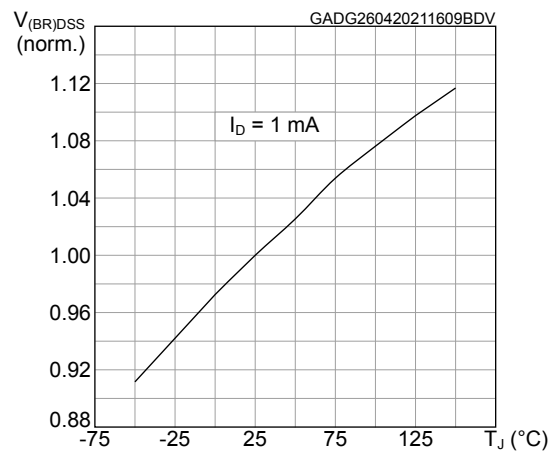
**Figure 10. Normalized on-resistance vs temperature**



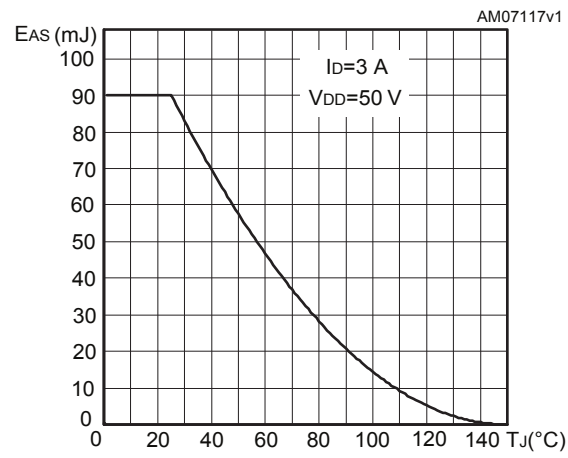
**Figure 11. Typical reverse diode forward characteristics**



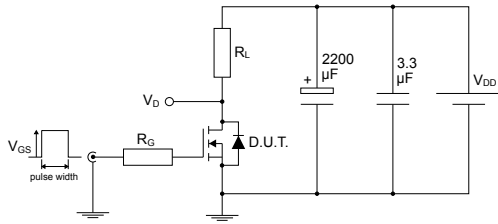
**Figure 12. Normalized breakdown voltage vs temperature**



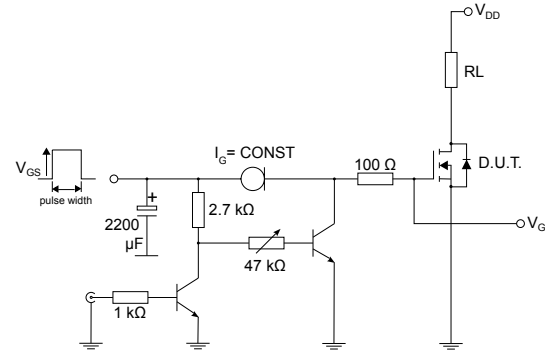
**Figure 13. Maximum avalanche energy vs starting  $T_J$**



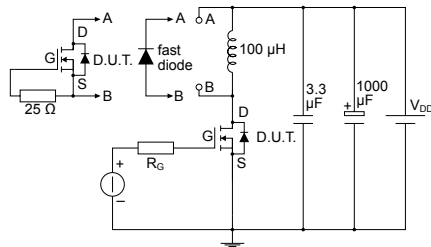
### 3 Test circuits

**Figure 14. Test circuit for resistive load switching times**


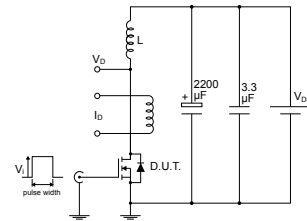
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**Figure 15. Test circuit for gate charge behavior**


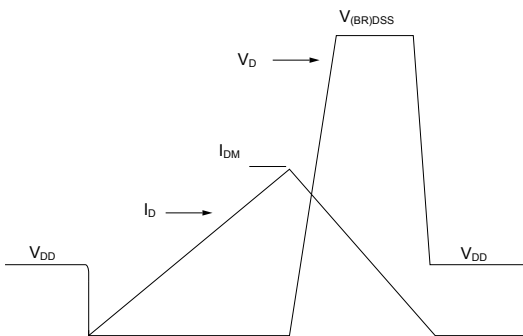
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**Figure 16. Test circuit for inductive load switching and diode recovery times**


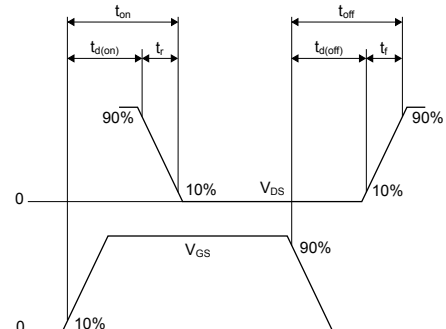
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**Figure 17. Unclamped inductive load test circuit**


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**Figure 18. Unclamped inductive waveform**


AM01472v1

**Figure 19. Switching time waveform**


AM01473v1

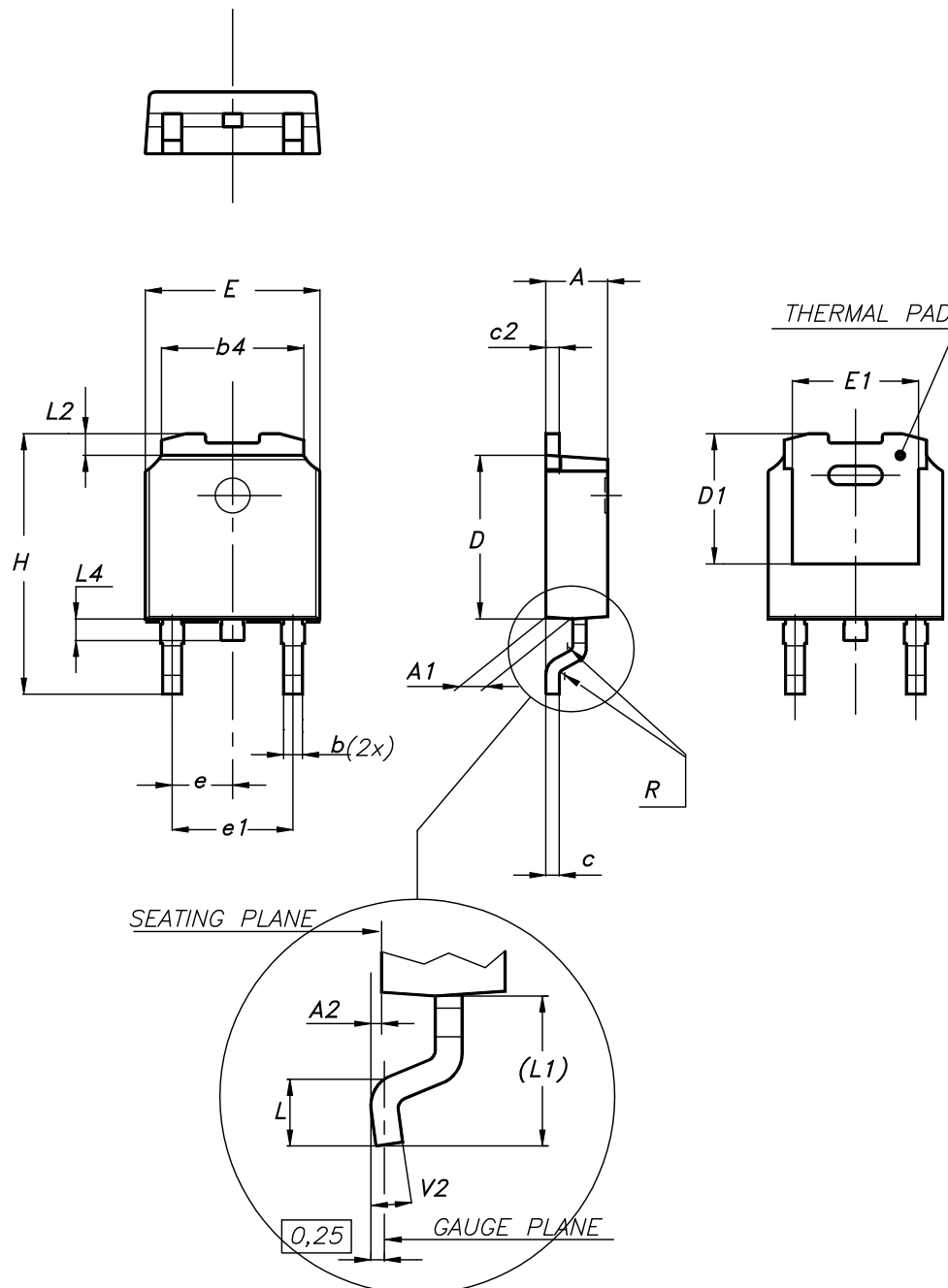


## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 4.1 DPAK (TO-252) type A2 package information

Figure 20. DPAK (TO-252) type A2 package outline



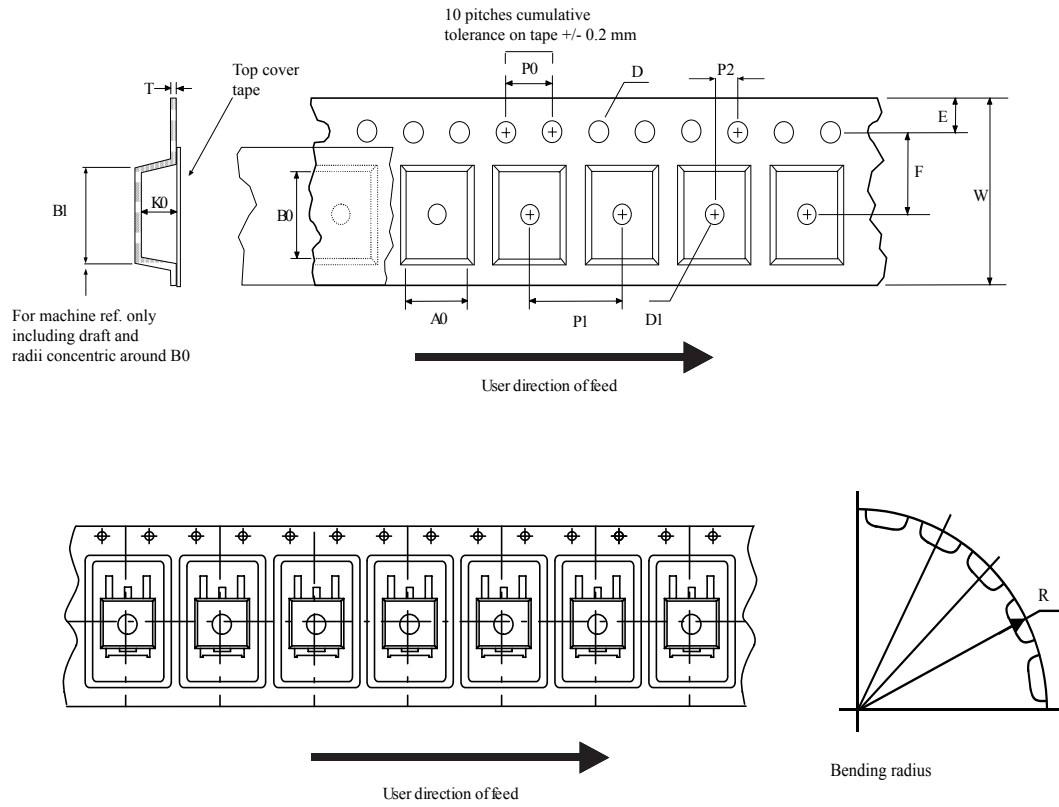
0068772\_type-A2\_rev30

**Table 8. DPAK (TO-252) type A2 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

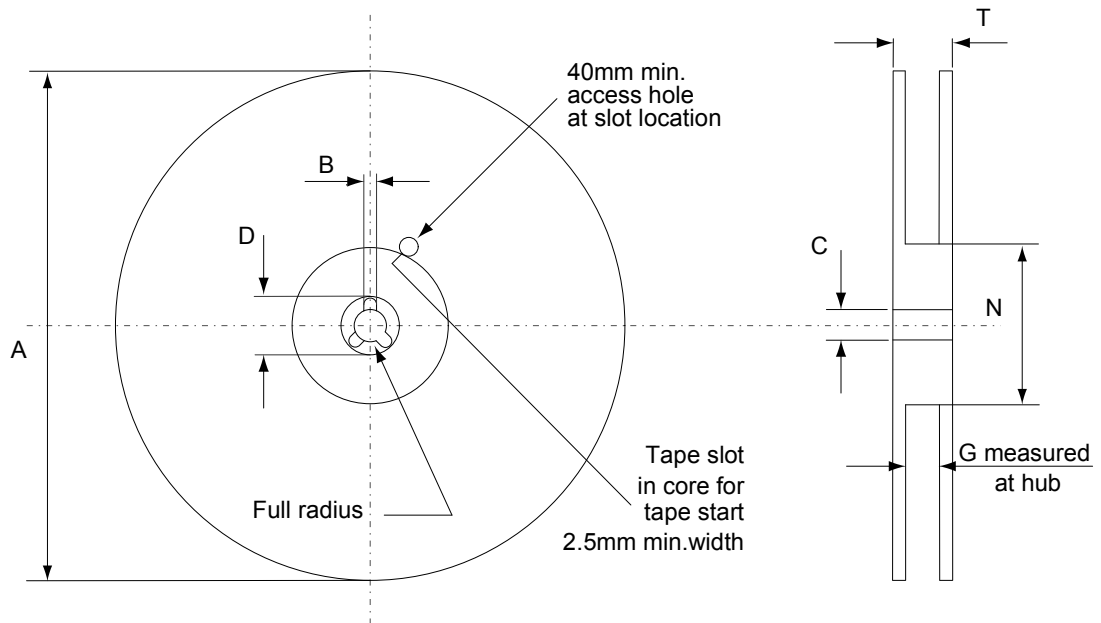
## 4.2 DPAK (TO-252) packing information

Figure 21. DPAK (TO-252) tape outline



AM08852v1

**Figure 22. DPAK (TO-252) reel outline**



AM06038v1

**Table 9. DPAK (TO-252) tape and reel mechanical data**

Dim.	Tape		Dim.	Reel	
	mm			mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1		Base qty.	2500
P1	7.9	8.1		Bulk qty.	2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

## Revision history

**Table 10. Document revision history**

Date	Revision	Changes
05-May-2021	1	First release.

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