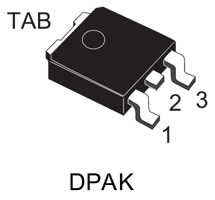
STD80N6F6

Automotive-grade N-channel 60 V, 4.4 mΩ typ., 80 A STripFET™ F6 Power MOSFET in a DPAK package

Datasheet - production data



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STD80N6F6	60 V	5 mΩ	80 A

- AEC-Q101 qualified
- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the STripFET™ F6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{DS(on)}$ in all packages.

Figure 1: Internal schematic diagram

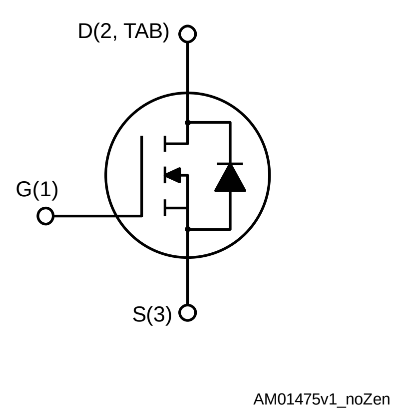


Table 1: Device summary

Order code	Marking	Package	Packaging
STD80N6F6	80N6F6	DPAK	Tape and reel

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	±20	V
I_D(1)	Drain current (continuous) at T_C = 25 °C	80	A
I_D(1)	Drain current (continuous) at T_C= 100 °C	80	A
I_{DM}(2)	Drain current (pulsed)	320	A
P_{TOT}	Total dissipation at T_C = 25 °C	120	W
T_{stg}	Storage temperature range	- 55 to 175	°C
T_j	Operating junction temperature range		

Notes:

(1)Current limited by package.

(2) Pulse width limited by safe operating area.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	1.25	°C/W
$R_{thj\text{-}pcb}$(1)	Thermal resistance junction-pcb	50	°C/W

Notes:

(1)When mounted on a 1-inch² FR-4 board, 2oz Cu.

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified).

Table 4: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 250 µA	60			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 60 V			1	µA
		V_{GS} = 0 V, V_{DS} = 60 V, T_j = 125 °C (1)			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D= 40 A		4.4	5	mΩ

Notes:

(1)Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0 V	-	8325	-	pF
C_{oss}	Output capacitance		-	500	-	pF
C_{rss}	Reverse transfer capacitance		-	400	-	pF
Q_g	Total gate charge	V_{DD} = 30 V, I_D = 80 A, V_{GS} = 0 to 10 V (see *Figure 14: "Test circuit for gate charge behavior"*)	-	147	-	nC
Q_{gs}	Gate-source charge		-	44	-	nC
Q_{gd}	Gate-drain charge		-	46	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 30 V, I_D = 40 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 13: "Test circuit for resistive load switching times"* and *Figure 18: "Switching time waveform"*)	-	40	-	ns
t_r	Rise time		-	71	-	ns
$t_{d(off)}$	Turn-off delay time		-	132	-	ns
t_f	Fall time		-	40	-	ns

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}(1)	Source-drain current		-		80	A
I_{SDM}(2)	Source-drain current (pulsed)		-		320	A
V_{SD}(3)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 80 A	-		1.3	V
t_{rr}	Reverse recovery time	I_{SD} = 80 A, di/dt = 100 A/µs, V_{DD} = 48 V, T_j = 150 °C (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*)	-	46		ns
Q_{rr}	Reverse recovery charge		-	65		nC
I_{RRM}	Reverse recovery current		-	2.8		A

Notes:

(1) Current limited by package.

(2) Pulse width limited by safe operating area.

(3) Pulsed: pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

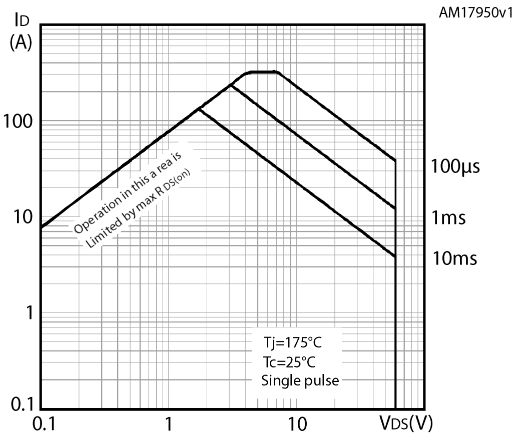


Figure 3: Thermal impedance

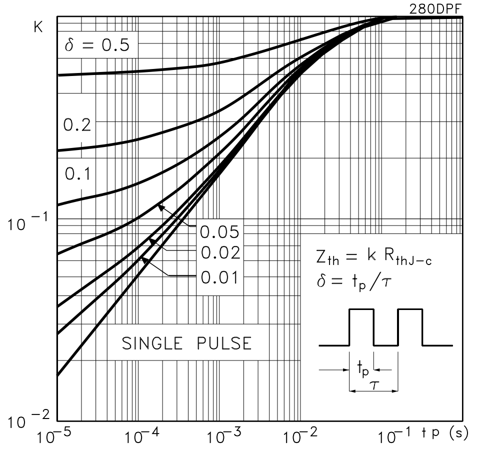


Figure 4: Output characteristics

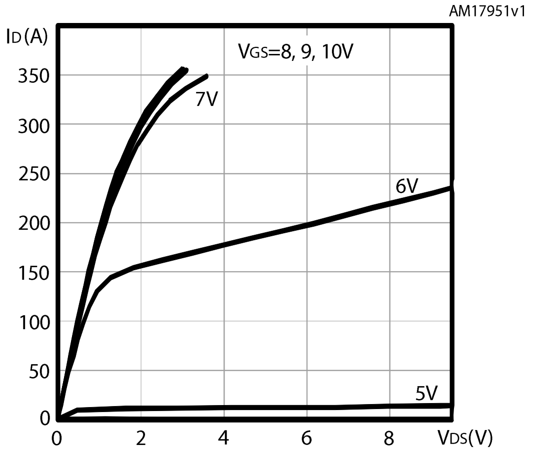


Figure 5: Transfer characteristics

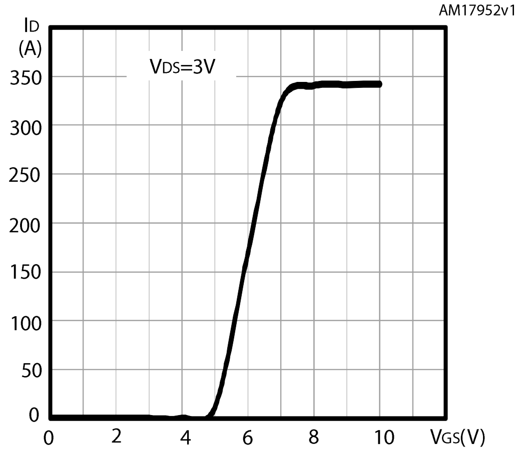


Figure 6: Normalized gate threshold voltage vs. temperature

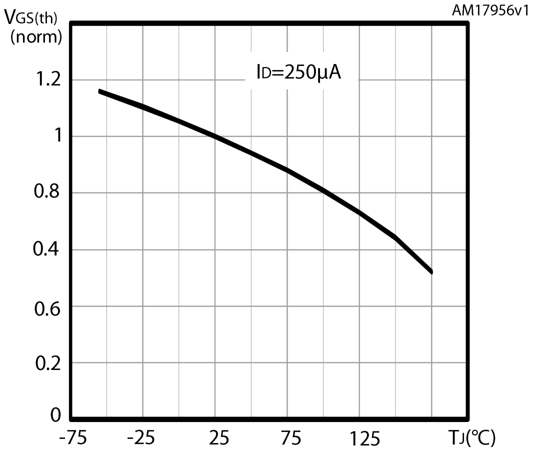


Figure 7: Normalized V(BR)DSS vs. temperature

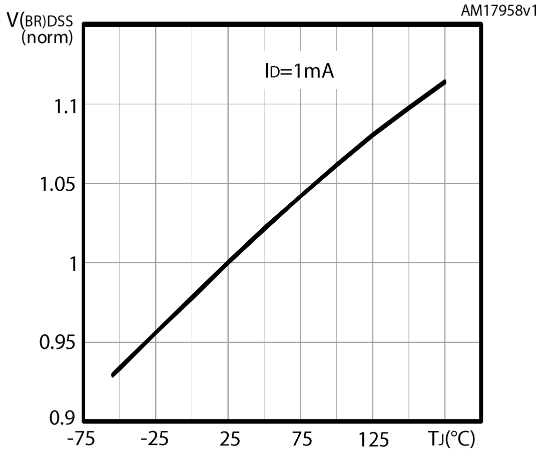


Figure 8: Static drain-source on-resistance

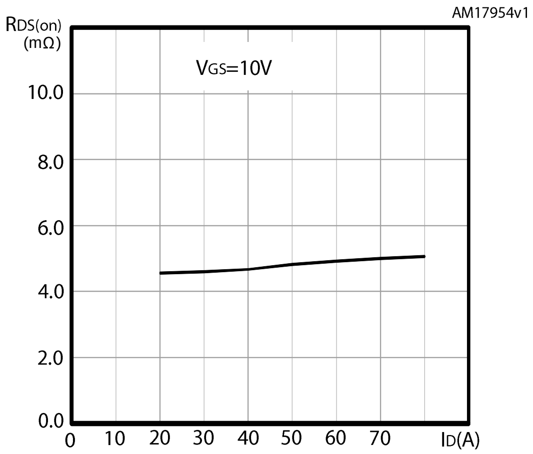


Figure 9: Normalized on-resistance vs. temperature

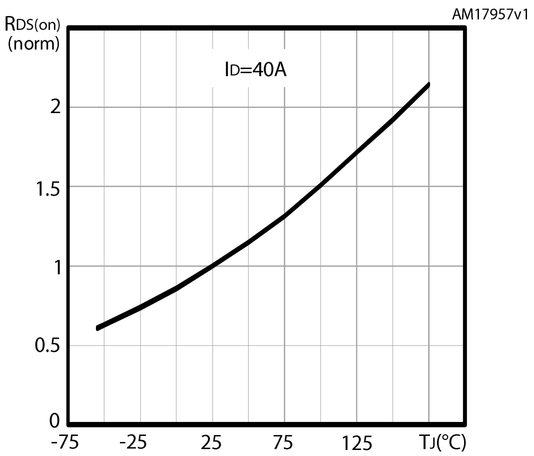


Figure 10: Gate charge vs. gate-source voltage

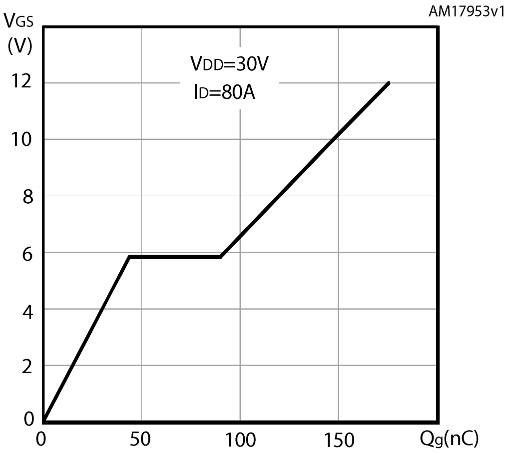


Figure 11: Capacitance variations

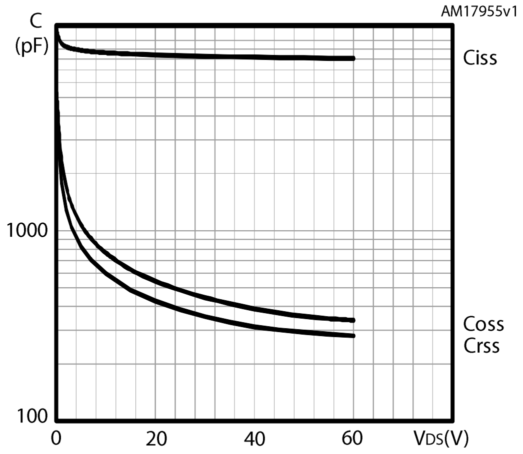
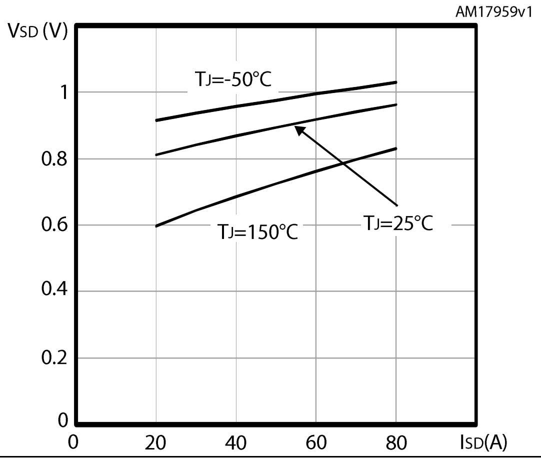


Figure 12: Source- drain diode forward characteristics



3 Test circuits

Figure 13: Test circuit for resistive load switching times

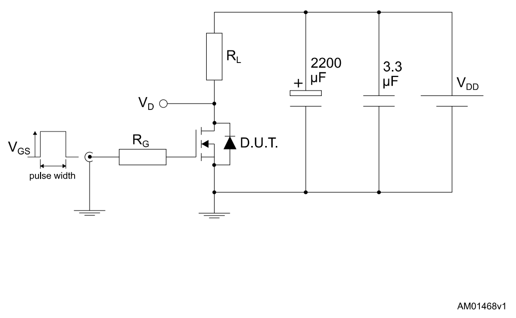


Figure 14: Test circuit for gate charge behavior

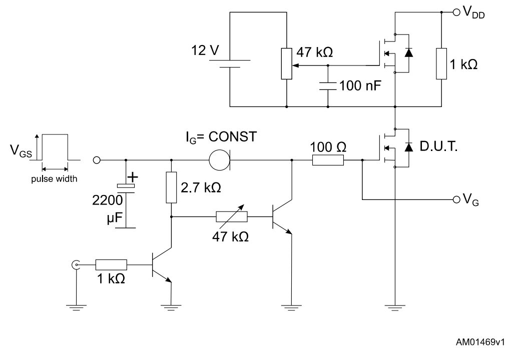


Figure 15: Test circuit for inductive load switching and diode recovery times

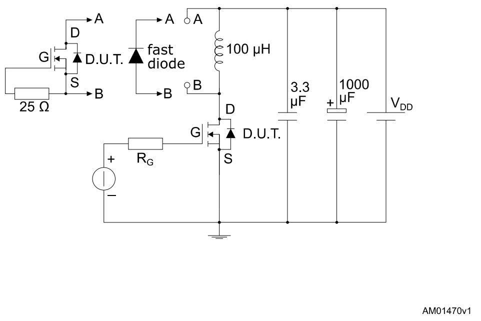


Figure 16: Unclamped inductive load test circuit

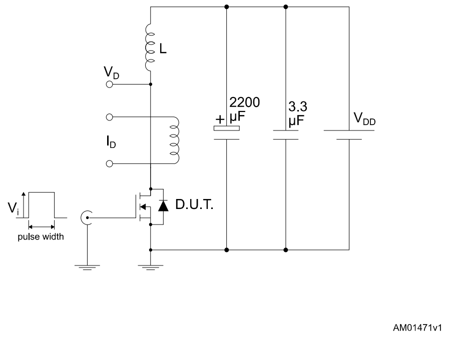


Figure 17: Unclamped inductive waveform

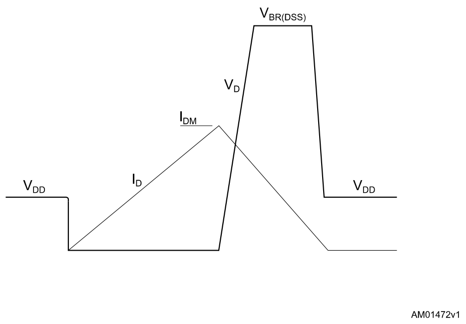
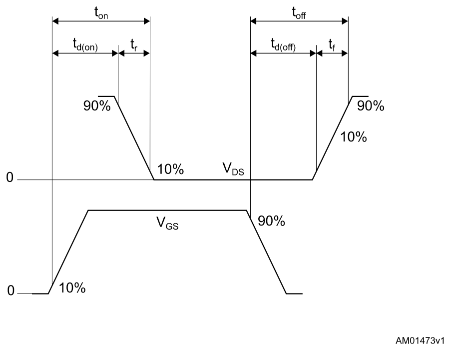


Figure 18: Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A2 package information

Figure 19: DPAK (TO-252) type A2 package outline

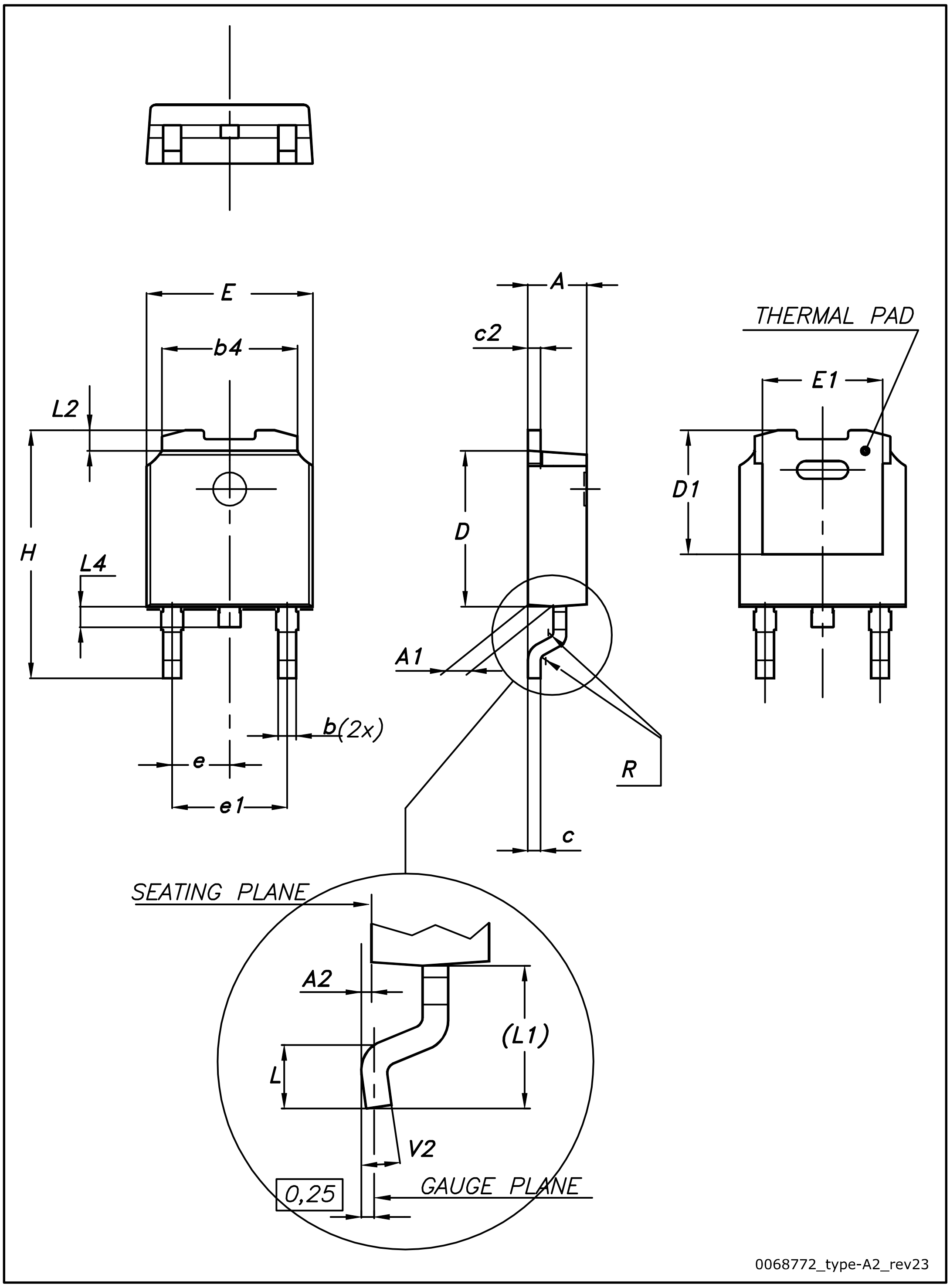
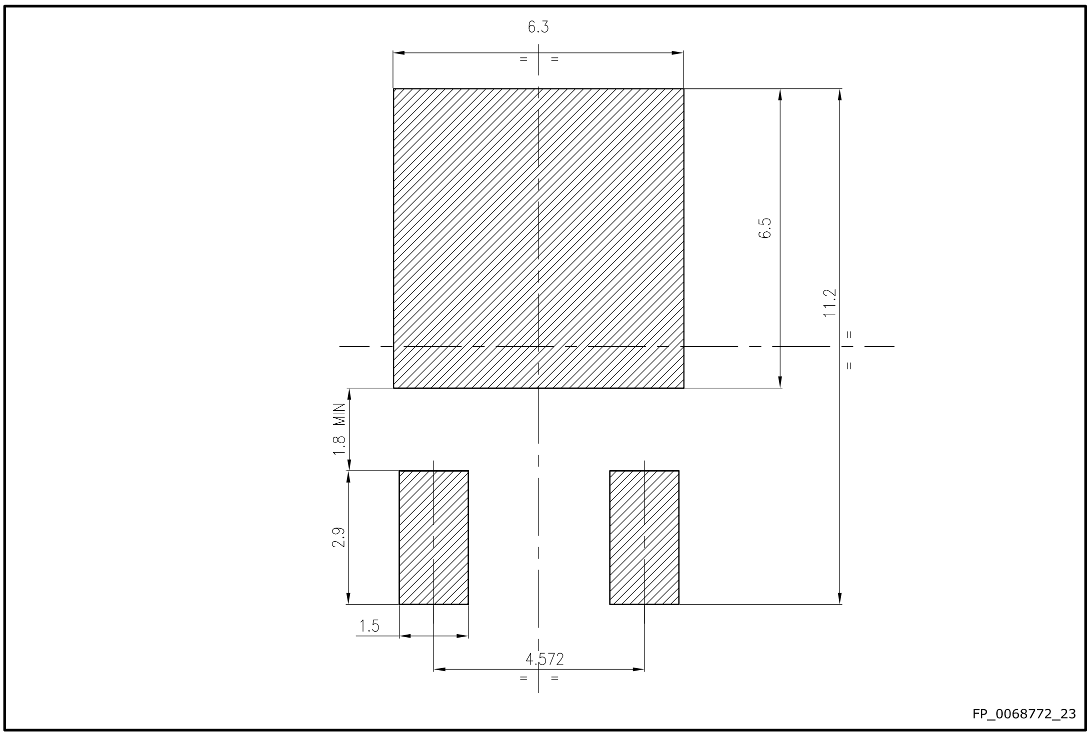


Table 8: DPAK (TO-252) type A2 mechanical data

Dim.	mm		
	Min.	**Typ.**	**Max.**
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 20: DPAK (TO-252) type A2 recommended footprint (dimensions are in mm)



4.2 DPAK (TO-252) tape and reel mechanical data

Figure 21: DPAK (TO-252) tape outline

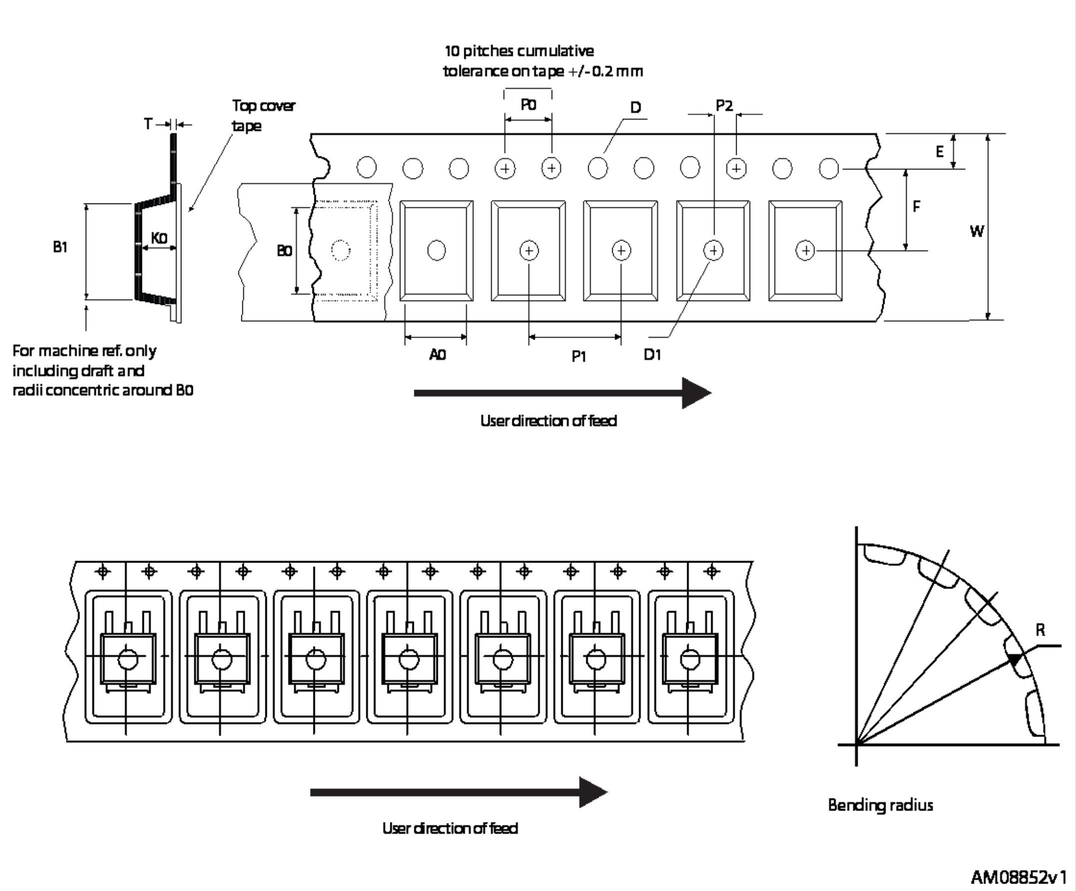


Figure 22: DPAK (TO-252) reel outline

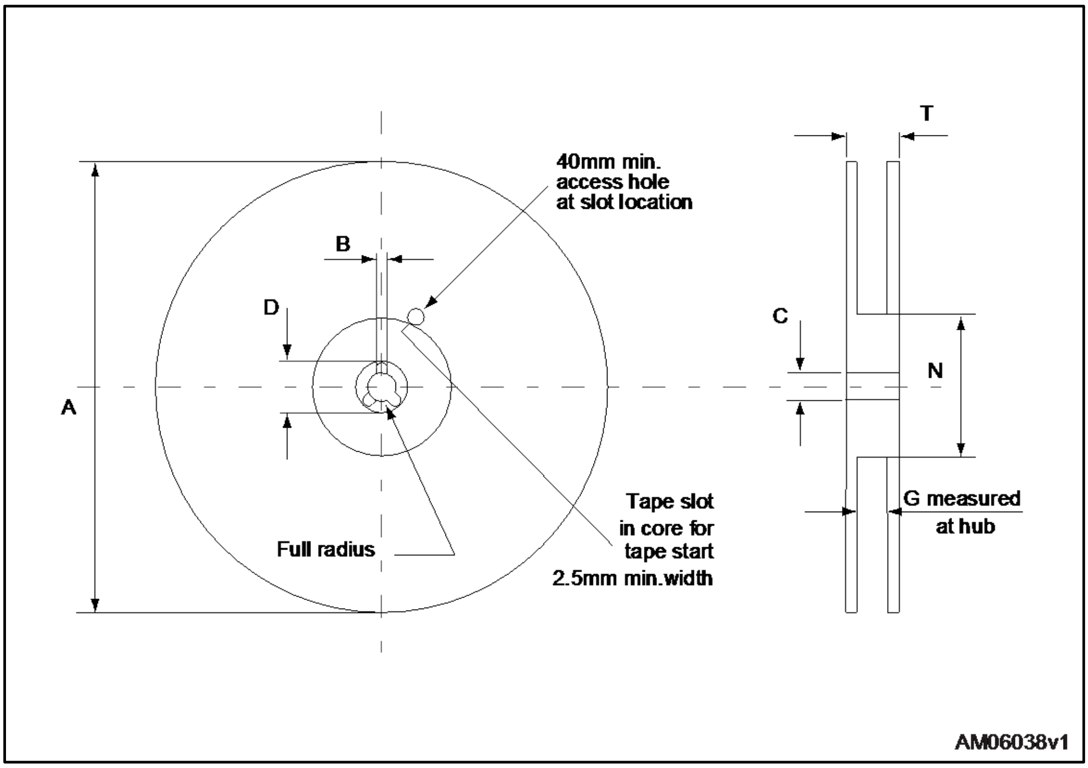


Table 9: DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	**mm**		**Dim.**	**mm**	
	Min.	**Max.**		**Min.**	**Max.**
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
08-Aug-2012	1	Initial release.
17-Jan-2014	2	– Document status promoted from preliminary to production data – Modified: title – Modified: Features – Added: note 1 in cover page – Modified: RDS(on)max and ID values in cover page – Modified: Derating factor value in Table 2 – Modified: RDS(on) values in Table 4 – Modified: ID and the entire typical values in Table 5, 6 and 7 – Added: Section 2.1: Electrical characteristics (curves) – Updated: Section 3: Package mechanical data – Minor text changes
23-May-2017	3	Modified title and features on cover page. Modified *Table 3: "Thermal data"*. Modified *Section 4: "Package mechanical data"*. Minor text changes.