



STD840DN40

Dual NPN high voltage transistors in a single package

Preliminary data

Features

- Low $V_{CE(sat)}$
- Simplified circuit design
- Reduced component count
- Fast switching speed

Applications

- Compact fluorescent lamp (CFL) 220 V mains
- Electronic ballast for fluorescent lighting

Description

The device is a dual NPN high voltage power transistors manufactured in multi-epitaxial planar technology. It is housed in dual island DIP-8 package with separated terminals for high assembly flexibility.

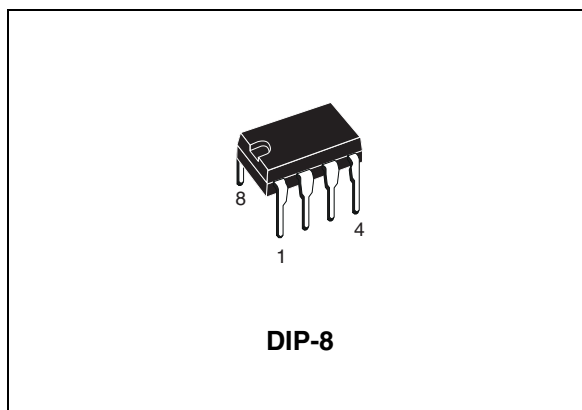
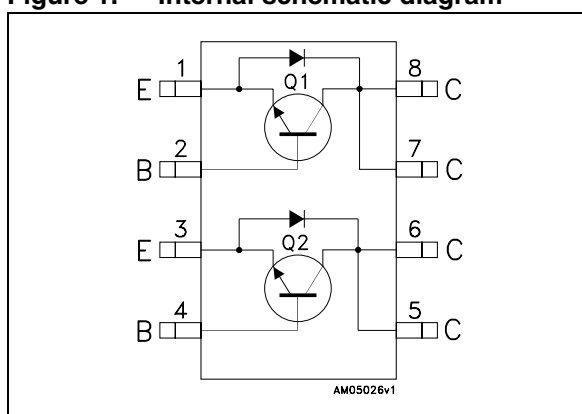


Figure 1. Internal schematic diagram



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Table 1. Device summary

Order code	Marking	Package	Packaging
STD840DN40	D840DN40	DIP-8	Tube

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-base voltage ($I_E = 0$)	700	V
V_{CEO}	Collector-emitter voltage ($I_B = 0$)	400	V
V_{EBO}	Emitter-base voltage ($I_C = 0$, $I_B = 1.5$ A, $t_p < 10$ ms)	$V_{(BR)EBO}$	V
I_C	Collector current	4	A
I_{CM}	Collector peak current ($t_p < 5$ ms)	8	A
I_B	Base current	1.5	A
I_{BM}	Base peak current ($t_p < 5$ ms)	3	A
P_{TOT}	Total dissipation at $T_{amb} = 25$ °C single transistor	TBD	W
	Total dissipation at $T_{amb} = 25$ °C both transistors	TBD	W
T_{STG}	Storage temperature	-65 to 150	°C
T_J	Max. operating junction temperature	150	°C

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJA}^{(1)}$	Thermal resistance junction-ambient (Single transistor)	TBD	°C/W
	Thermal resistance junction-ambient (Both transistors)	TBD	°C/W

1. When mounted on 1 inch square pad of 2 oz. copper, $t \leq 10$ sec.

2 Electrical characteristics

$T_{\text{case}} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector cut-off current ($V_{\text{BE}} = 0$)	$V_{\text{CE}} = 700\text{ V}$ $V_{\text{CE}} = 700\text{ V}$ $T_{\text{c}} = 125\text{ }^{\circ}\text{C}$			100 500	μA μA
I_{CEO}	Collector cut-off current ($I_{\text{B}} = 0$)	$V_{\text{CE}} = 400\text{ V}$			250	μA
$V_{(\text{BR})\text{EBO}}$	Emitter-base breakdown voltage ($I_{\text{C}} = 0$)	$I_{\text{E}} = 10\text{ mA}$	9		18	V
$V_{\text{CEO(sus)}}^{(1)}$	Collector-emitter sustaining voltage ($I_{\text{B}} = 0$)	$I_{\text{C}} = 10\text{ mA}$	400			V
$V_{\text{CE(sat)}}^{(1)}$	Collector-emitter saturation voltage	$I_{\text{C}} = 1\text{ A}$ $I_{\text{B}} = 0.2\text{ A}$ $I_{\text{C}} = 2\text{ A}$ $I_{\text{B}} = 0.4\text{ A}$			0.5 1	V V
$V_{\text{BE(sat)}}^{(1)}$	Base-emitter saturation voltage	$I_{\text{C}} = 1\text{ A}$ $I_{\text{B}} = 0.2\text{ A}$ $I_{\text{C}} = 2\text{ A}$ $I_{\text{B}} = 0.4\text{ A}$			1.2 1.3	V V
$h_{\text{FE}}^{(1)}$	DC current gain	$I_{\text{C}} = 10\text{ mA}$ $V_{\text{CE}} = 5\text{ V}$ $I_{\text{C}} = 2\text{ A}$ $V_{\text{CE}} = 5\text{ V}$	10 8		24	
V_{F}	Diode forward voltage	$I_{\text{F}} = 1\text{ A}$			2.5	V
t_{s} t_{f}	Resistive load Storage time Fall time	$I_{\text{C}} = 1\text{ A}$ $I_{\text{B1}} = - I_{\text{B2}} = 0.2\text{ A}$ $V_{\text{CC}} = 125\text{ V}$ $t_{\text{p}} = 20\text{ }\mu\text{s}$		2.5 0.2		μs μs

1. Pulse test: pulse duration $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

2.1 Electrical characteristics (curves)

Figure 2. DC current gain ($V_{CE} = 1\text{ V}$)

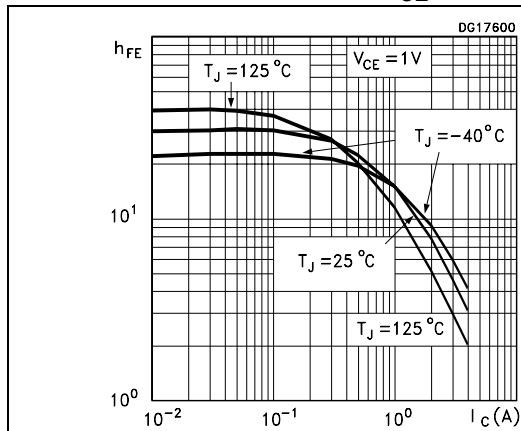


Figure 3. DC current gain ($V_{CE} = 5\text{ V}$)

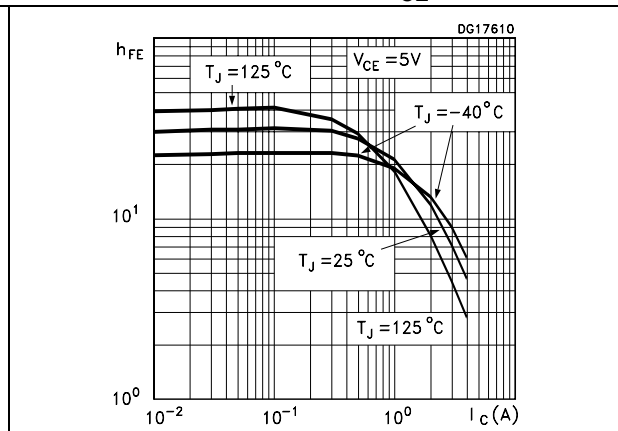


Figure 4. Collector-emitter saturation voltage

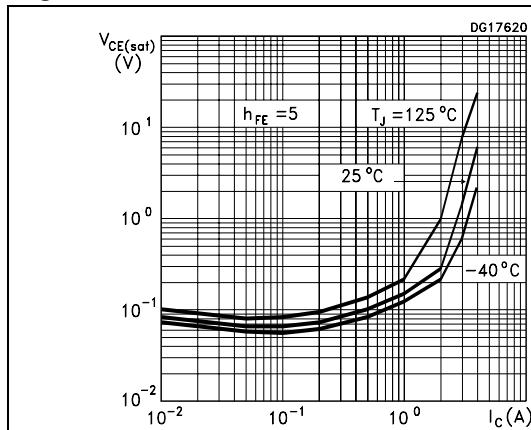


Figure 5. Base-emitter saturation voltage

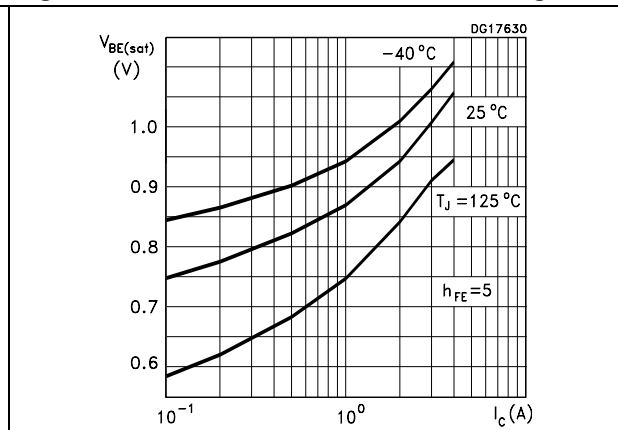


Figure 6. Freewheel diode forward voltage

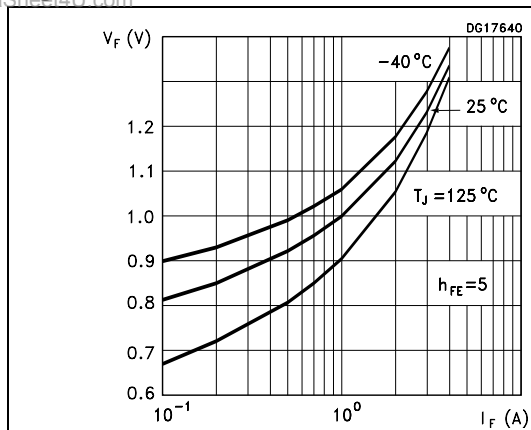
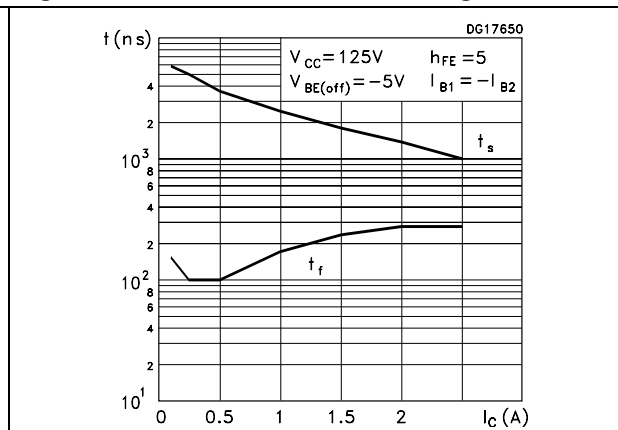
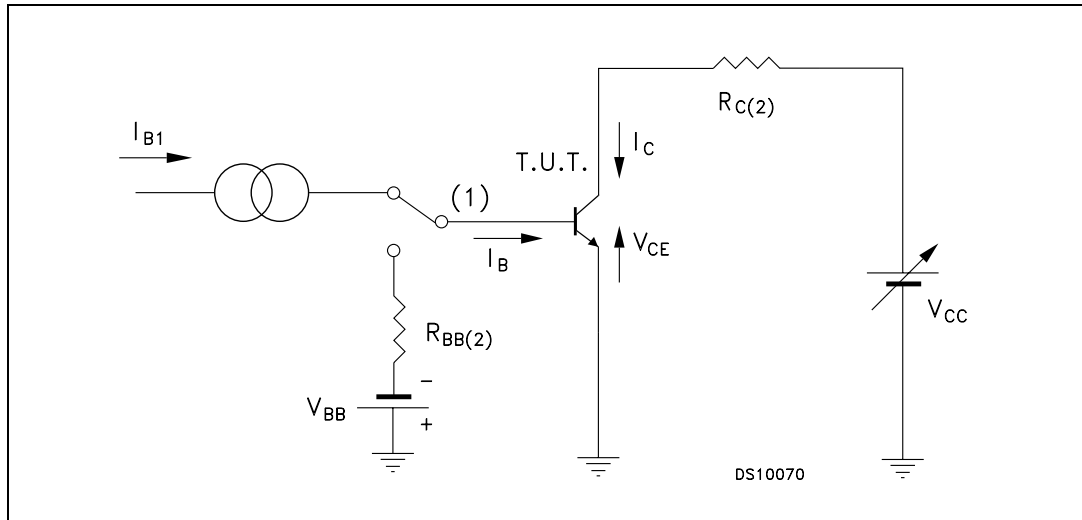


Figure 7. Resistive load switching time



3 Test circuit

Figure 8. Resistive load switching test circuit



1. Fast electronic switch
2. Non-inductive resistor

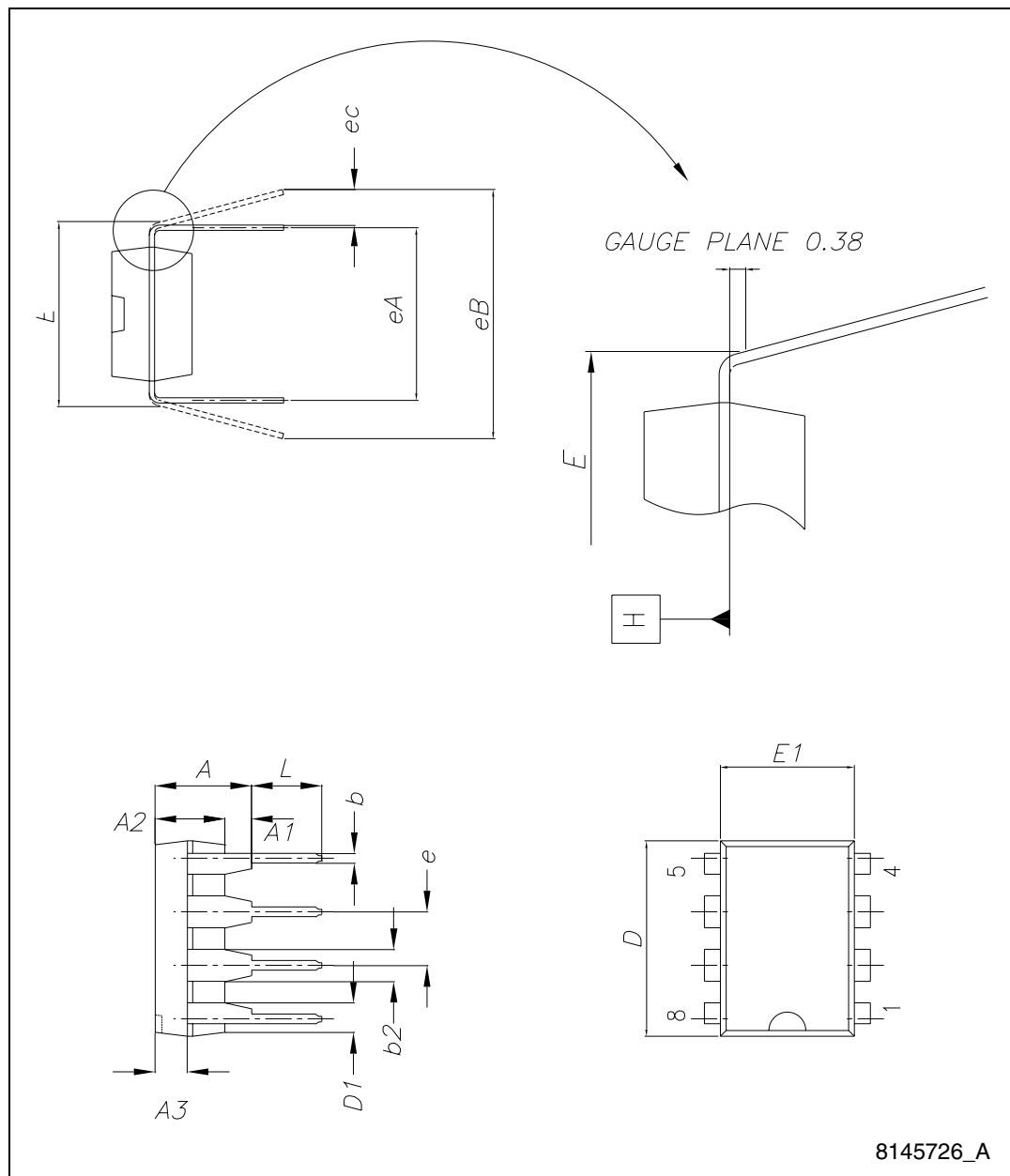
4 Package mechanical data

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Table 5. DIP-8 mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A			4.80
A1	0.50		
A2	3.10		3.50
A3	1.40		1.60
b	0.38		0.55
b1	0.38		0.51
b2	1.47		1.57
b3	0.89		1.09
c	0.21		0.35
c1	0.20		0.30
D	9.10		9.30
D1	0.13		
E	7.62		8.25
E1	6.25		6.45
e		2.54	
eA		7.62	
eB	7.62		10.90
eC	0		1.52
L	2.92		3.81

Figure 9. Drawing dimension DIP-8



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5 Revision history

Table 6. Document revision history

Date	Revision	Changes
18-Nov-2009	1	Initial release.

STD840DN40

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