



STD888

HIGH CURRENT, HIGH PERFORMANCE, LOW VOLTAGE PNP TRANSISTOR

Ordering Code	Marking
STD888	D888

- VERY LOW COLLECTOR TO EMITTER SATURATION VOLTAGE
- DC CURRENT GAIN, $h_{FE} > 100$
- 5 A CONTINUOUS COLLECTOR CURRENT
- SURFACE-MOUNTING DPAK (TO-252)
- POWER PACKAGE IN TAPE & REEL (Suffix "T4")

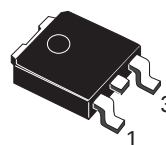
APPLICATIONS

- POWER MANAGEMENT IN PORTABLE EQUIPMENT
- VOLTAGE REGULATION IN BIAS SUPPLY CIRCUITS
- SWITCHING REGULATOR IN BATTERY CHARGER APPLICATIONS
- HEAVY LOAD DRIVER

DESCRIPTION

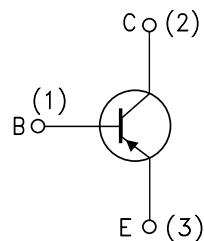
The device is manufactured in low voltage PNP Planar Technology by using a "Base Island" layout.

The resulting Transistor shows exceptional high gain performance coupled with very low saturation voltage.



**DPAK
TO-252**
(Suffix "T4")

INTERNAL SCHEMATIC DIAGRAM



SC08810

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CBO}	Collector-Base Voltage ($I_E = 0$)	-60	V
V_{CEO}	Collector-Emitter Voltage ($I_B = 0$)	-30	V
V_{EBO}	Emitter-Base Voltage ($I_C = 0$)	-6	V
I_C	Collector Current	-5	A
I_{CM}	Collector Peak Current ($t_p < 5$ ms)	-10	A
P_{tot}	Total Dissipation at $T_C = 25$ °C	15	W
T_{stg}	Storage Temperature	-65 to 150	°C
T_j	Max. Operating Junction Temperature	150	°C

THERMAL DATA

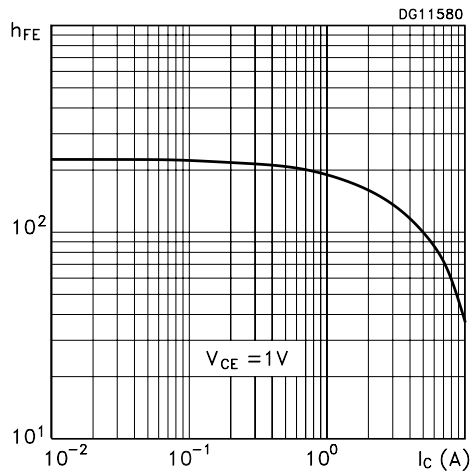
$R_{thj-case}$ •	Thermal Resistance Junction-Case	Max	8.33	°C/W
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ELECTRICAL CHARACTERISTICS ($T_{case} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

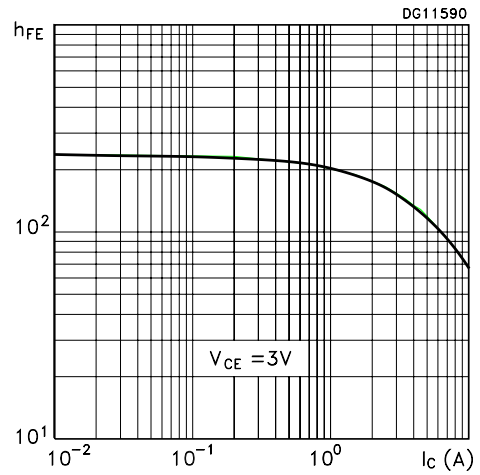
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CBO}	Collector Cut-off Current ($I_E = 0$)	$V_{CB} = -30\text{ V}$ $V_{CB} = -30\text{ V}$ $T_j = 100\text{ }^{\circ}\text{C}$			-10 -1	nA μA
I_{EBO}	Emitter Cut-off Current ($I_C = 0$)	$V_{EB} = -6\text{ V}$			-10	nA
$V_{(BR)CEO}^*$	Collector-Emitter Breakdown Voltage ($I_B = 0$)	$I_C = -10\text{ mA}$	-30			V
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage ($I_E = 0$)	$I_C = -100\text{ }\mu\text{A}$	-60			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage ($I_C = 0$)	$I_E = -100\text{ }\mu\text{A}$	-6			V
$V_{CE(sat)}^*$	Collector-Emitter Saturation Voltage	$I_C = -500\text{ mA}$ $I_B = -5\text{ mA}$ $I_C = -2\text{ A}$ $I_B = -50\text{ mA}$ $I_C = -5\text{ A}$ $I_B = -250\text{ mA}$ $I_C = -6\text{ A}$ $I_B = -250\text{ mA}$ $I_C = -8\text{ A}$ $I_B = -400\text{ mA}$ $I_C = -10\text{ A}$ $I_B = -500\text{ mA}$			-0.15 -0.25 -0.70 -0.70 -1 -1.5	V V V V V V
$V_{BE(sat)}^*$	Base-Emitter Saturation Voltage	$I_C = -2\text{ A}$ $I_B = -50\text{ mA}$ $I_C = -6\text{ A}$ $I_B = -250\text{ mA}$			-1.1 -1.4	V V
h_{FE}^*	DC Current Gain	$I_C = -10\text{ mA}$ $V_{CE} = -1\text{ V}$ $I_C = -500\text{ mA}$ $V_{CE} = -1\text{ V}$ $I_C = -5\text{ A}$ $V_{CE} = -1\text{ V}$ $I_C = -5\text{ A}$ $V_{CE} = -1\text{ V}$ $T_j = 100^{\circ}\text{C}$ $I_C = -8\text{ A}$ $V_{CE} = -1\text{ V}$ $I_C = -10\text{ A}$ $V_{CE} = -1\text{ V}$	150 150 75 75 40 15	200 200 100 100 55 35	300	
t_d t_r t_s t_f	RESISTIVE LOAD Delay Time RiseTime StorageTime Fall Time	$I_C = -3\text{ A}$ $I_{B1} = -I_{B2} = -60\text{ mA}$ $V_{CC} = -20\text{ V}$ (see figure 1)		180 160 250 80	220 210 300 100	ns ns ns ns

* Pulsed: Pulse duration = 300 μs , duty cycle $\leq 1.5\%$

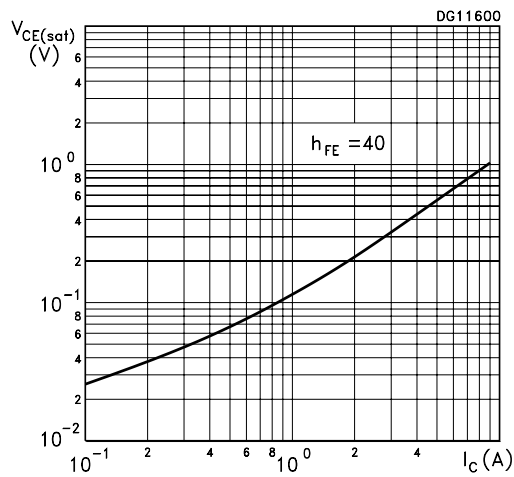
DC Current Gain



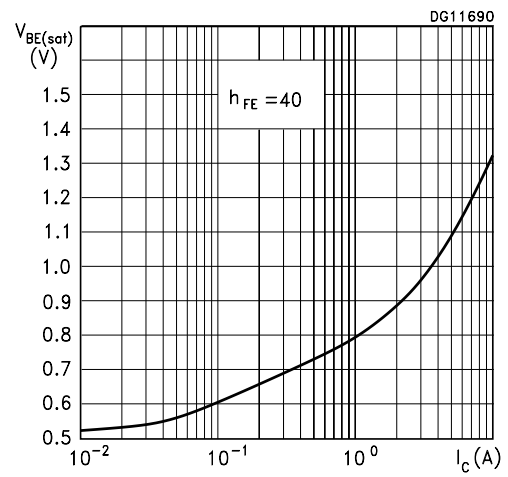
DC Current Gain



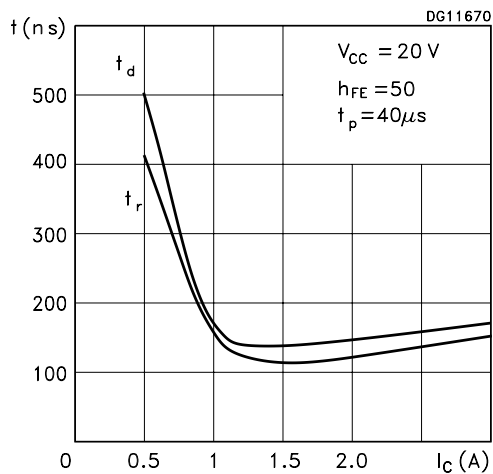
Collector-Emitter Saturation Voltage



Base-Emitter Saturation Voltage



Switching Times Resistive Load



Switching Times Resistive Load

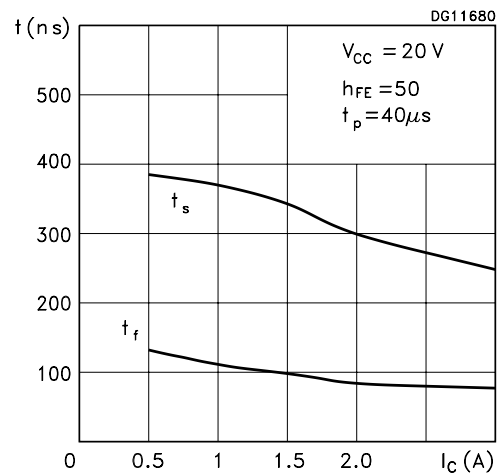
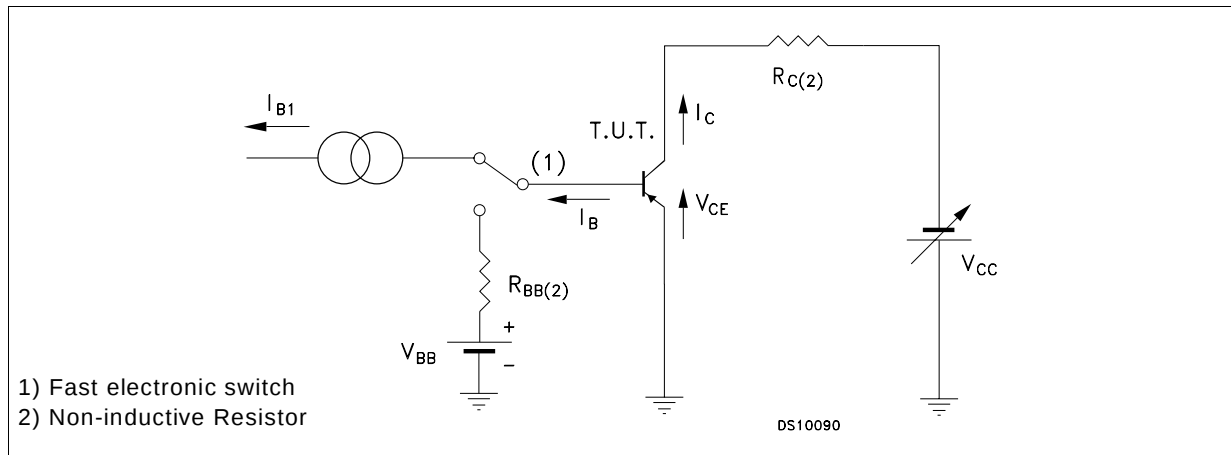
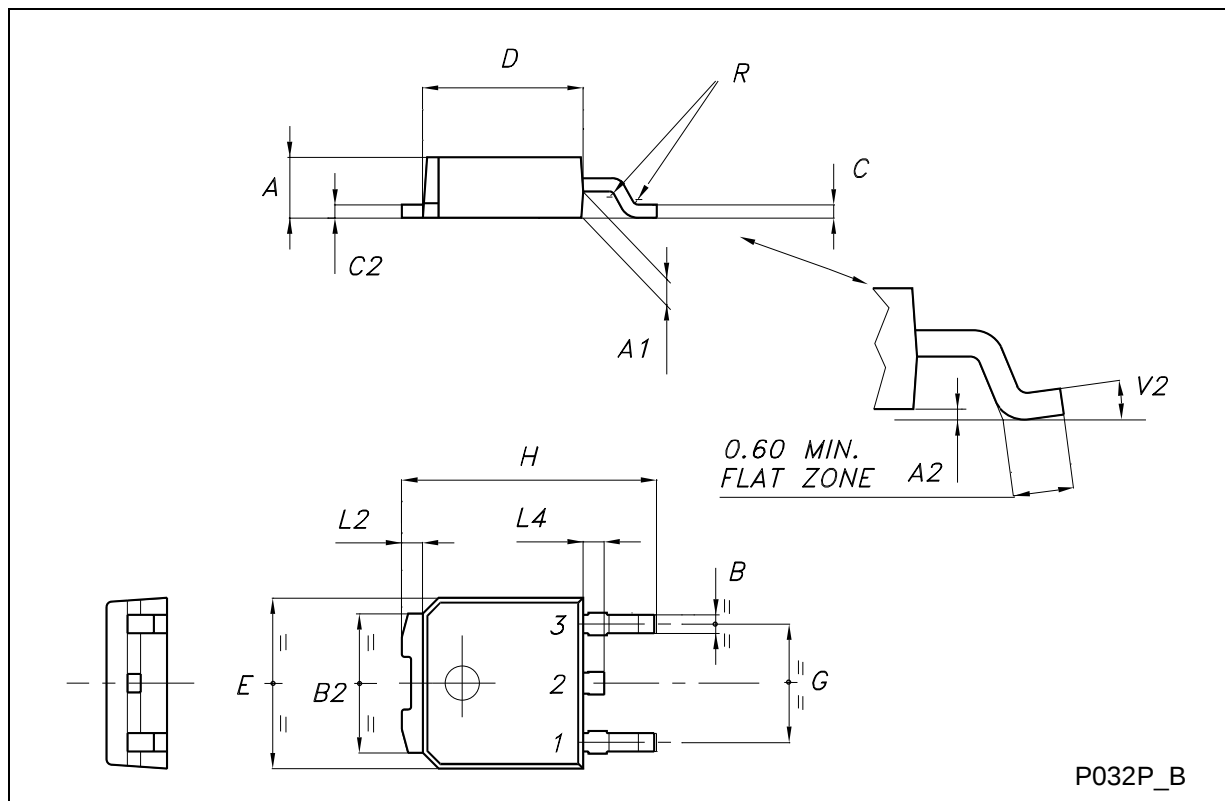


Figure 1: Resistive Load Switching Test Circuit.

TO-252 (DPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°



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