



STD95N4LF3

N-channel 40 V, 5.0 mΩ typ., 80 A STripFET™ III Power MOSFET in a DPAK package

Datasheet — production data

Features

| Type | V _{DSS} | R _{DS(on) max} | I _D | P _D |
|------------|------------------|-------------------------|---------------------|----------------|
| STD95N4LF3 | 40 V | < 6.0 mΩ | 80 A ⁽¹⁾ | 110 W |

1. Value limited by wire bonding

- 100% avalanche tested
- Logic level drive

Applications

- Switching application
 - Automotive

Description

This device is an N-channel enhancement mode Power MOSFET produced using STMicroelectronics' STripFET™ III technology, which is specifically designed to minimize on-resistance and gate charge to provide superior switching performance.

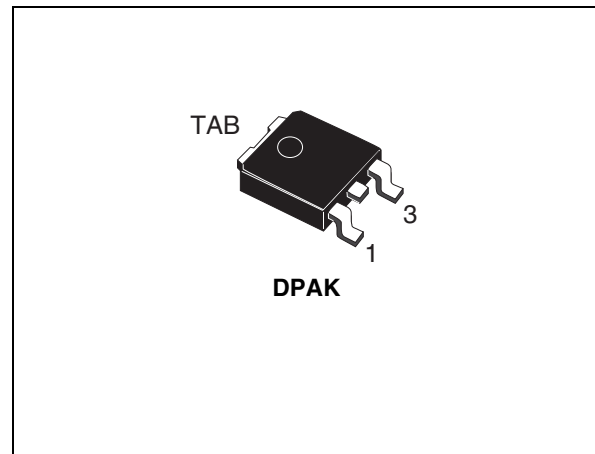


Figure 1. Internal schematic diagram

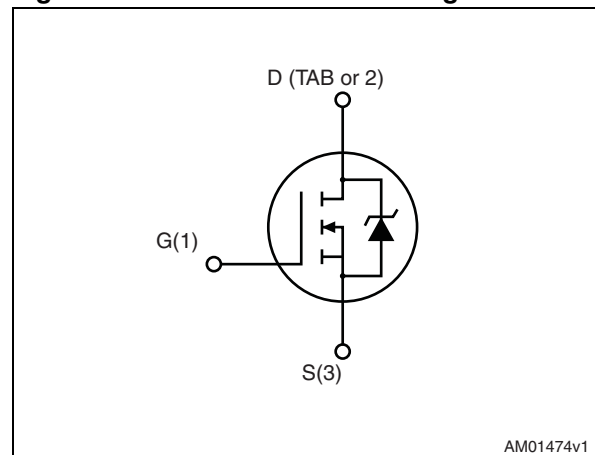


Table 1. Device summary

| Order codes | Marking | Package | Packaging |
|-------------|---------|---------|---------------|
| STD95N4LF3 | 95N4LF3 | DPAK | Tape and reel |

Contents

| | | |
|----------|---|-----------|
| 1 | Electrical ratings | 3 |
| 2 | Electrical characteristics | 4 |
| | 2.1 Electrical characteristics (curves) | 6 |
| 3 | Test circuits | 8 |
| 4 | Package mechanical data | 10 |
| 5 | Packing mechanical data | 12 |
| 6 | Revision history | 14 |

1 Electrical ratings

Table 2. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|--------------------|---|------------|---------------------|
| V_{DS} | Drain-source voltage | 40 | V |
| V_{GS} | Gate-source voltage | ± 16 | V |
| $I_D^{(1)}$ | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$ | 80 | A |
| I_D | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$ | 65 | A |
| $I_{DM}^{(2)}$ | Drain current (pulsed) | 320 | A |
| P_{TOT} | Total dissipation at $T_C = 25\text{ }^\circ\text{C}$ | 110 | W |
| | Derating factor | 0.73 | W/ $^\circ\text{C}$ |
| $dv/dt^{(3)}$ | Peak diode recovery voltage slope | 8 | V/ns |
| $E_{AS}^{(4)}$ | Single pulse avalanche energy | 400 | mJ |
| T_j T_{stg} | Operating junction temperature Storage temperature | -55 to 175 | $^\circ\text{C}$ |

1. Value limited by wire bonding
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 80\text{ A}$, $di/dt \leq 40\text{ A}/\mu\text{s}$, $V_{DS} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$
4. Starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = 40\text{ A}$, $V_{DD} = 35\text{ V}$ [Figure 16](#) and [Figure 17](#)

Table 3. Thermal data

| Symbol | Parameter | Value | Unit |
|---------------------|--------------------------------------|-------|---------------------------|
| $R_{thj-case}$ | Thermal resistance junction-case max | 1.36 | $^\circ\text{C}/\text{W}$ |
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-pcb max | 50 | $^\circ\text{C}/\text{W}$ |

1. When mounted on 1inch² FR-4 2Oz Cu board

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 4. On/off states

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|--|---|------|------|------------|--------------------------------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $I_D = 250\ \mu\text{A}$, $V_{GS} = 0$ | 40 | | | V |
| I_{DSS} | Zero gate voltage drain current ($V_{GS} = 0$) | $V_{DS} = 40\ \text{V}$ $V_{DS} = 40\ \text{V}$, $T_C = 125\text{ °C}$ | | | 10 100 | μA μA |
| I_{GSS} | Gate-body leakage current ($V_{DS} = 0$) | $V_{GS} = \pm 16\ \text{V}$ | | | ± 200 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$ | 1 | | 2.5 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS} = 10\ \text{V}$, $I_D = 40\ \text{A}$ $V_{GS} = 5\ \text{V}$, $I_D = 40\ \text{A}$ | | 5.0 | 6.0 9.0 | $\text{m}\Omega$ $\text{m}\Omega$ |

Table 5. Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------|------------------------------|---|------|------|------|------|
| C_{iss} | Input capacitance | $V_{DS} = 25\ \text{V}$, $f = 1\ \text{MHz}$, $V_{GS} = 0$ | - | 2500 | | pF |
| C_{oss} | Output capacitance | | | 560 | | pF |
| C_{rss} | Reverse transfer capacitance | | | 50 | | pF |
| $t_{d(on)}$ | Turn-on delay time | $V_{DD} = 20\ \text{V}$, $I_D = 40\ \text{A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 10\ \text{V}$ (see Figure 13 and Figure 18) | - | 7.5 | | ns |
| t_r | Rise time | | | 45 | | ns |
| $t_{d(off)}$ | Turn-off delay time | | | 45 | | ns |
| t_f | Fall time | | | 11 | | ns |
| Q_g | Total gate charge | $V_{DD} = 20\ \text{V}$, $I_D = 80\ \text{A}$, $V_{GS} = 10\ \text{V}$ (see Figure 14) | - | 50 | 70 | nC |
| Q_{gs} | Gate-source charge | | | 7 | | nC |
| Q_{gd} | Gate-drain charge | | | 9.5 | | nC |

Table 6. Source drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------------------------|--|--|------|---------------|-----------|---------------|
| I_{SD} $I_{SDM}^{(1)}$ | Source-drain current Source-drain current (pulsed) | | - | | 80 320 | A A |
| $V_{SD}^{(2)}$ | Forward on voltage | $I_{SD} = 80 \text{ A}$, $V_{GS} = 0$ | - | | 1.5 | V |
| t_{rr} Q_{rr} I_{RRM} | Reverse recovery time Reverse recovery charge Reverse recovery current | $I_{SD} = 80 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$, $V_{DD} = 20 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$ (see Figure 15 and Figure 19) | - | 40 55 3 | | ns nC A |

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

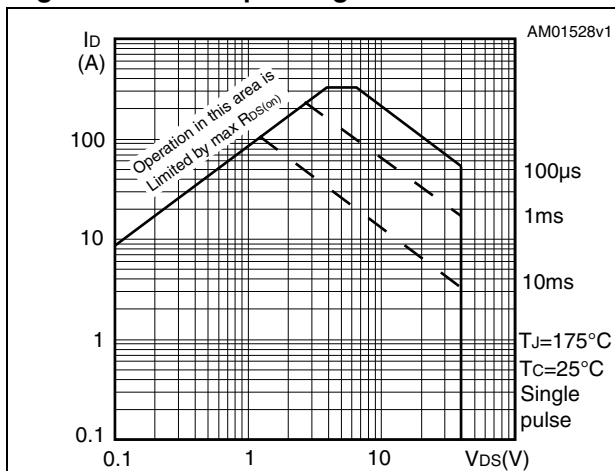


Figure 3. Thermal impedance

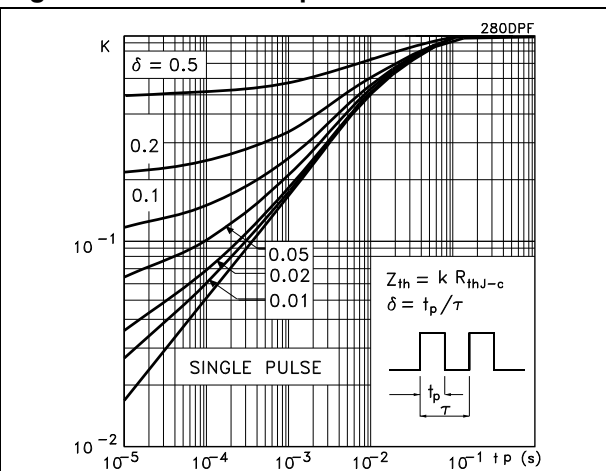


Figure 4. Output characteristics

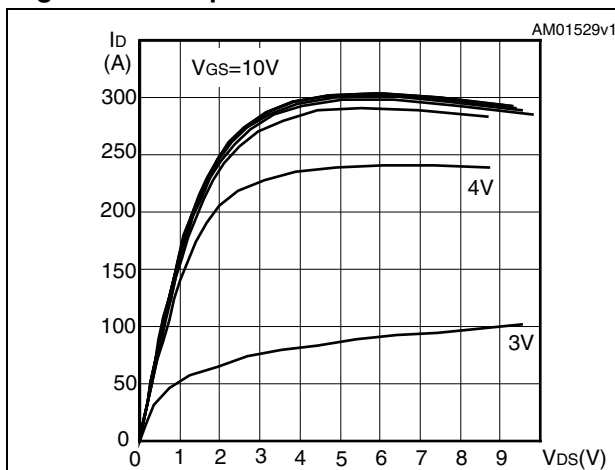


Figure 5. Transfer characteristics

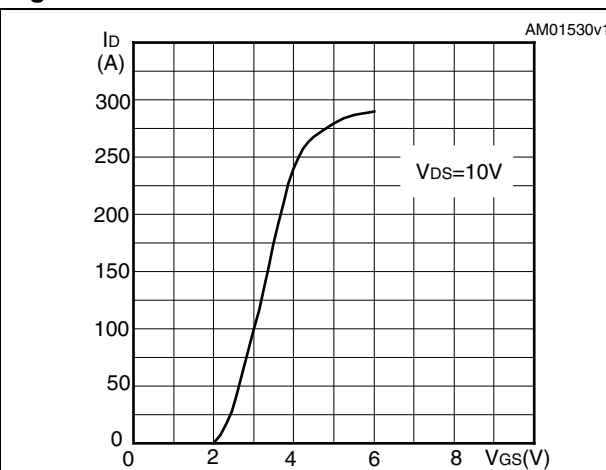


Figure 6. Static drain-source on-resistance

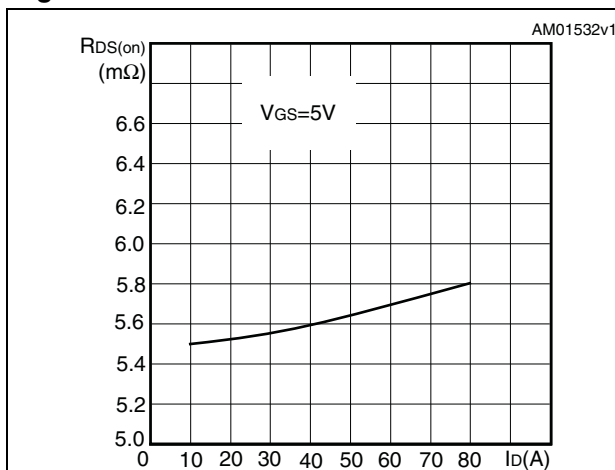


Figure 7. Normalized BV_{DSS} vs temperature

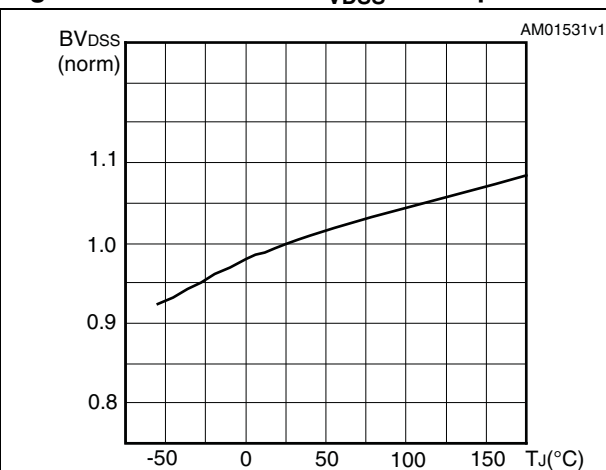


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

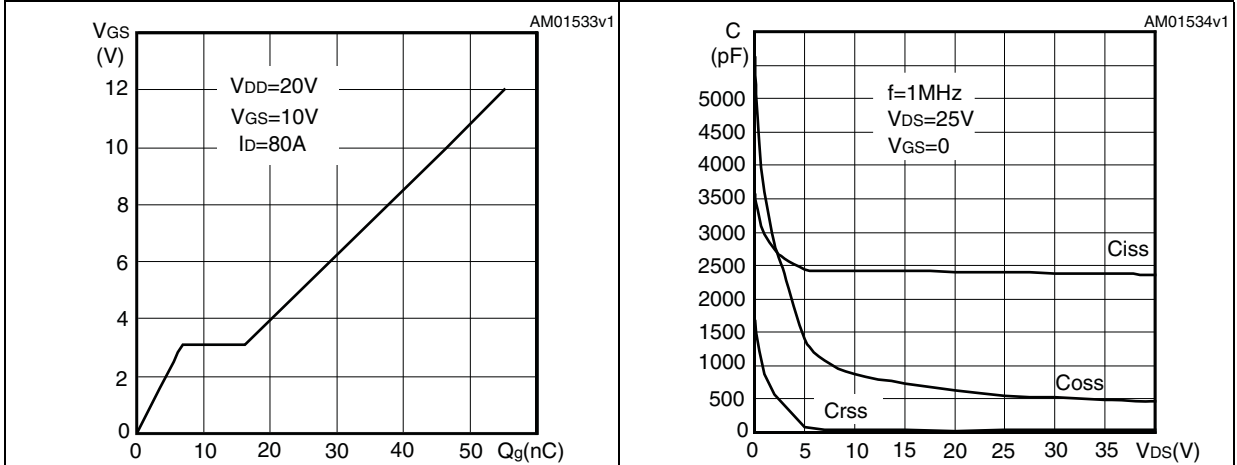


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

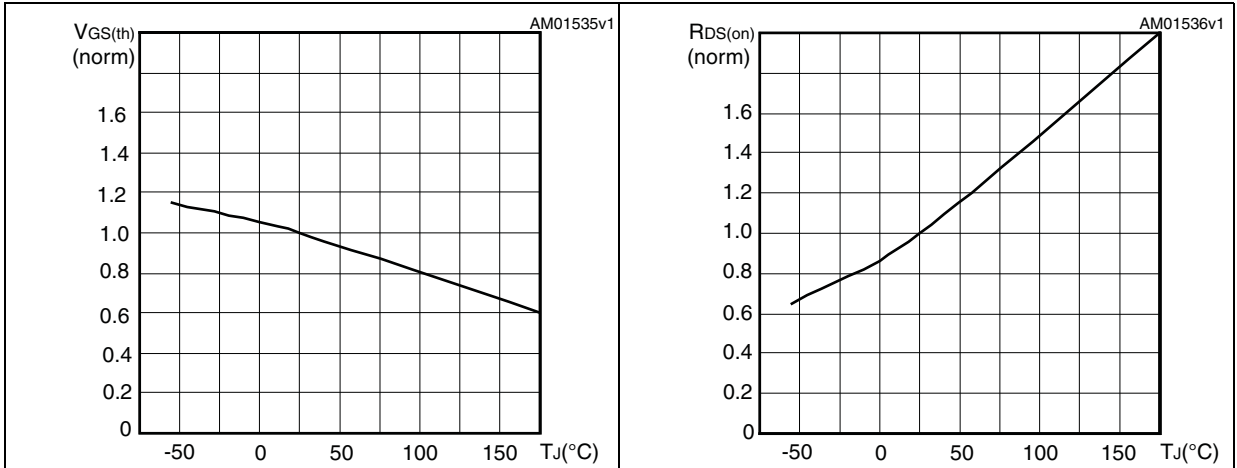
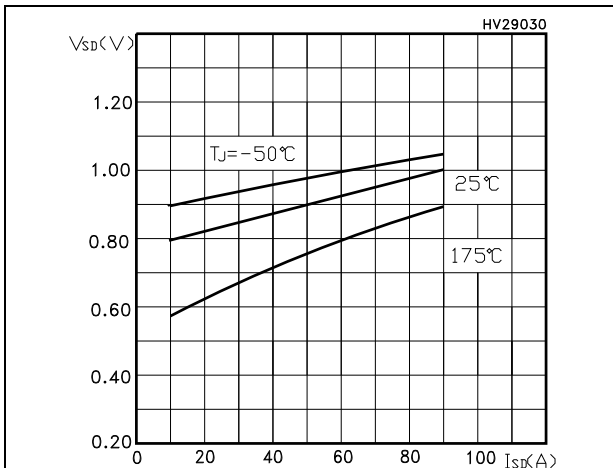


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load



AM01468v1

Figure 14. Gate charge test circuit



AM01469v1

Figure 15. Test circuit for inductive load switching and diode recovery times



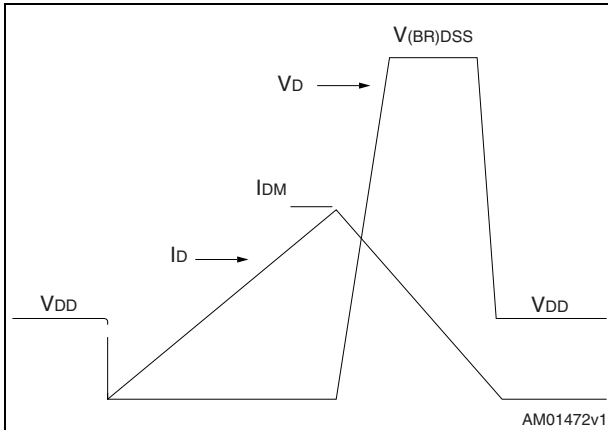
AM01470v1

Figure 16. Unclamped inductive load test circuit



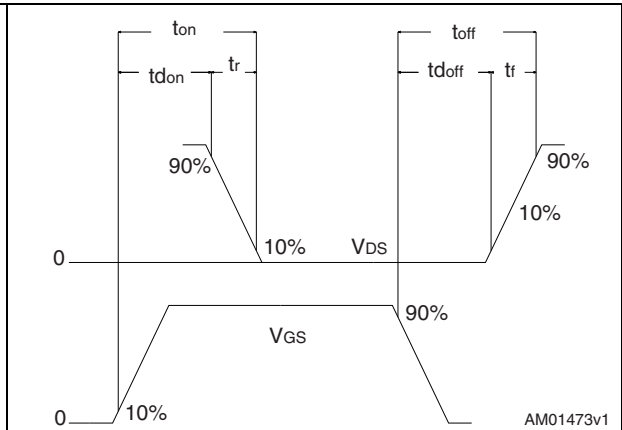
AM01471v1

Figure 17. Unclamped inductive waveform



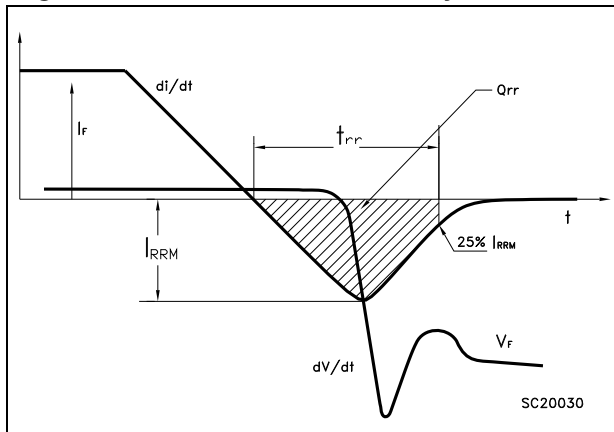
AM01472v1

Figure 18. Switching time waveform



AM01473v1

Figure 19. Diode reverse recovery waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 7. DPAK (TO-252) mechanical data

| Dim. | mm | | |
|------|------|------|-------|
| | Min. | Typ. | Max. |
| A | 2.20 | | 2.40 |
| A1 | 0.90 | | 1.10 |
| A2 | 0.03 | | 0.23 |
| b | 0.64 | | 0.90 |
| b4 | 5.20 | | 5.40 |
| c | 0.45 | | 0.60 |
| c2 | 0.48 | | 0.60 |
| D | 6.00 | | 6.20 |
| D1 | | 5.10 | |
| E | 6.40 | | 6.60 |
| E1 | | 4.70 | |
| e | | 2.28 | |
| e1 | 4.40 | | 4.60 |
| H | 9.35 | | 10.10 |
| L | 1 | | |
| L1 | | 2.80 | |
| L2 | | 0.80 | |
| L4 | 0.60 | | 1 |
| R | | 0.20 | |
| V2 | 0° | | 8° |

Figure 20. DPAK (TO-252) drawing

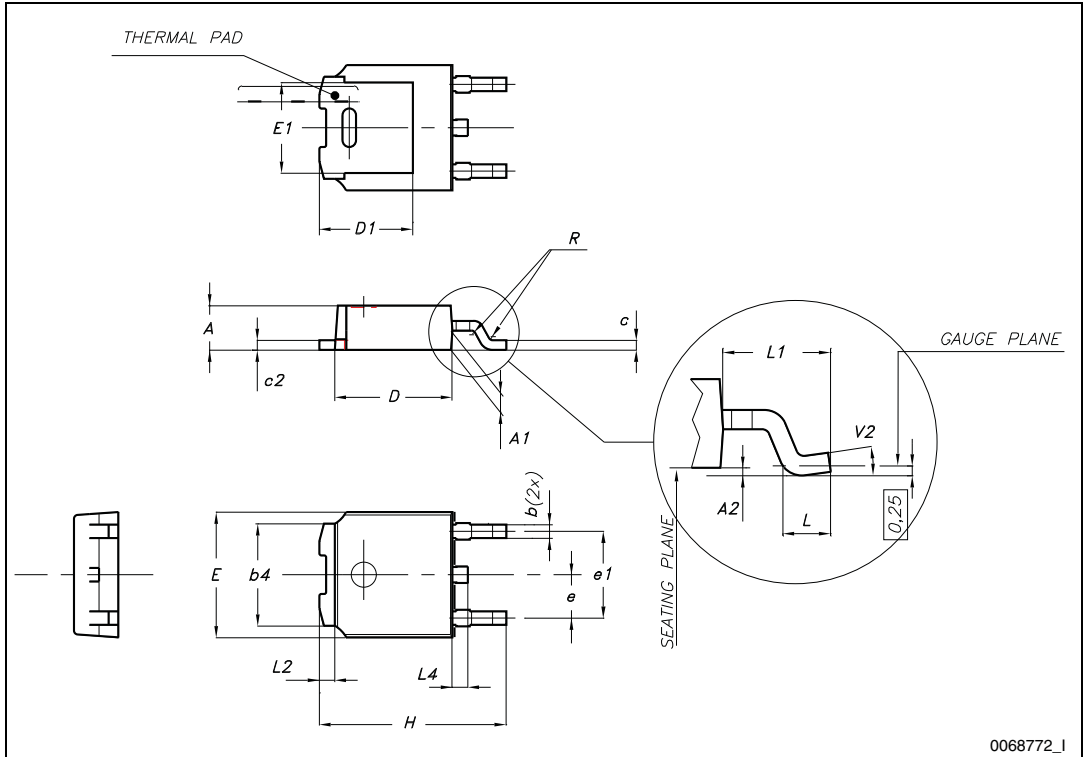
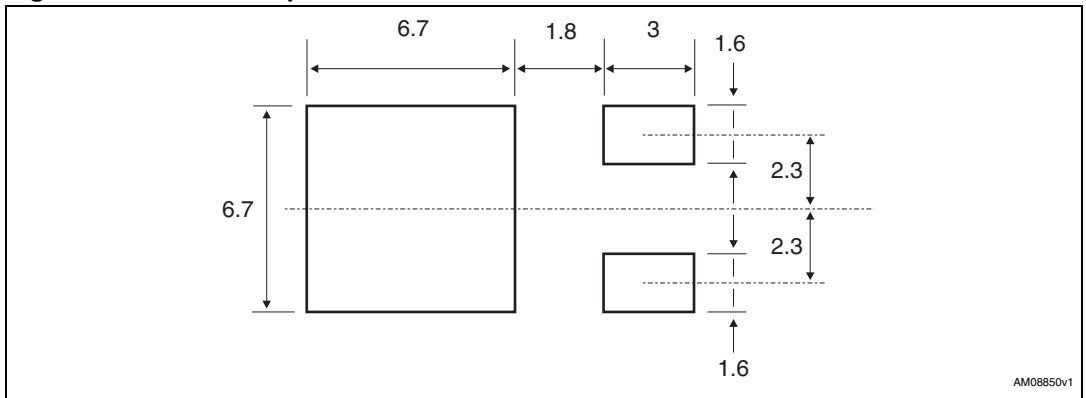


Figure 21. DPAK footprint^(a)



a. All dimensions are in millimeters

5 Packing mechanical data

Table 8. DPAK (TO-252) tape and reel mechanical data

| Tape | | | Reel | | |
|------|------|------|-----------|------|------|
| Dim. | mm | | Dim. | mm | |
| | Min. | Max. | | Min. | Max. |
| A0 | 6.8 | 7 | A | | 330 |
| B0 | 10.4 | 10.6 | B | 1.5 | |
| B1 | | 12.1 | C | 12.8 | 13.2 |
| D | 1.5 | 1.6 | D | 20.2 | |
| D1 | 1.5 | | G | 16.4 | 18.4 |
| E | 1.65 | 1.85 | N | 50 | |
| F | 7.4 | 7.6 | T | | 22.4 |
| K0 | 2.55 | 2.75 | | | |
| P0 | 3.9 | 4.1 | Base qty. | | 2500 |
| P1 | 7.9 | 8.1 | Bulk qty. | | 2500 |
| P2 | 1.9 | 2.1 | | | |
| R | 40 | | | | |
| T | 0.25 | 0.35 | | | |
| W | 15.7 | 16.3 | | | |

Figure 22. Tape for DPAK (TO-252)

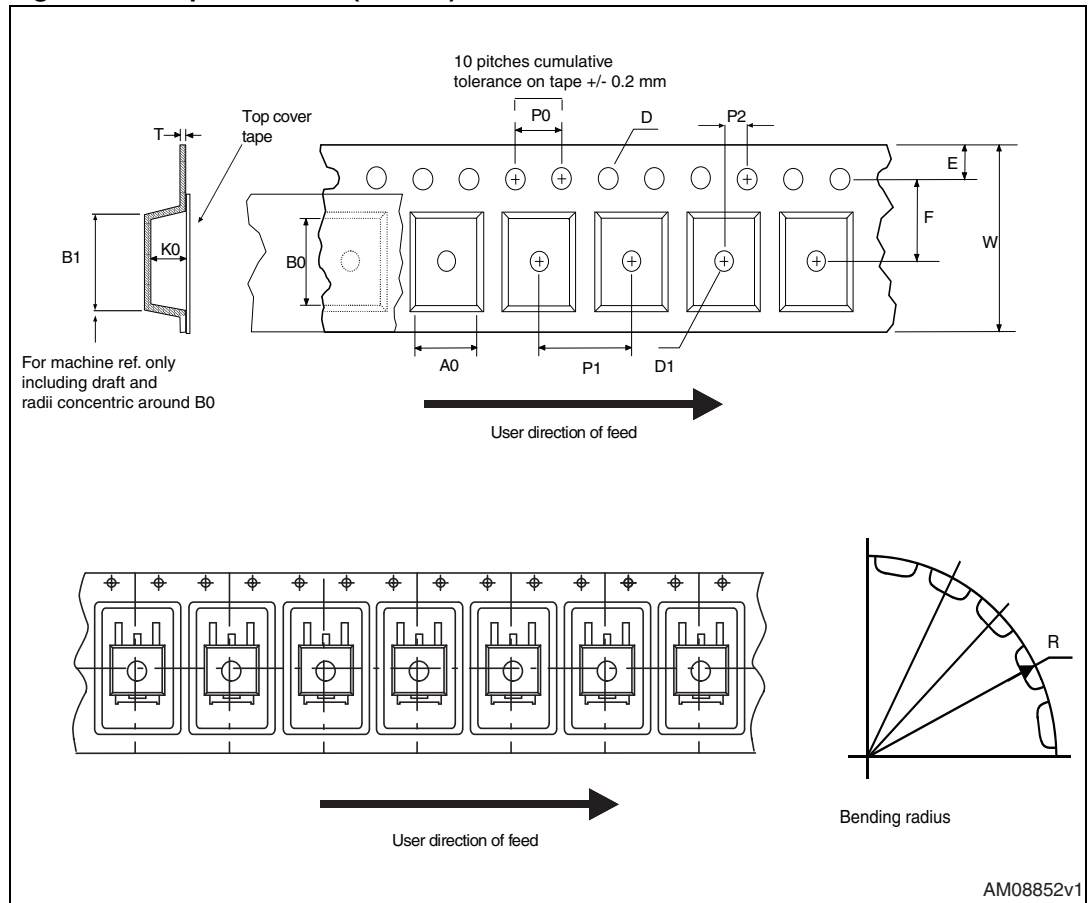
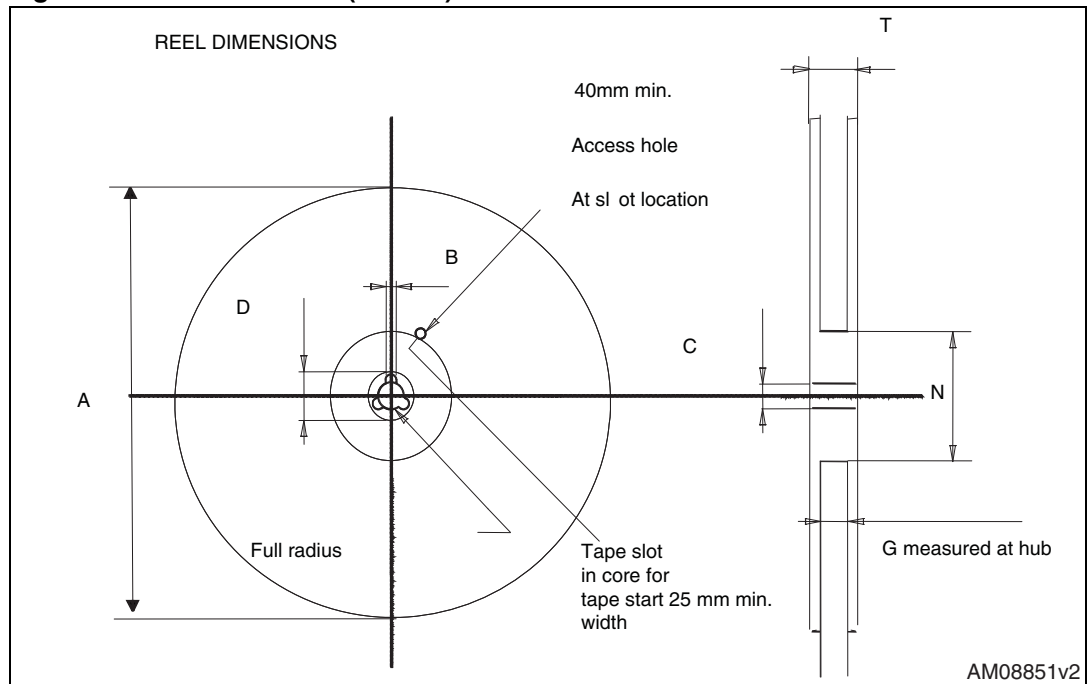


Figure 23. Reel for DPAK (TO-252)



6 Revision history

Table 9. Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 11-Feb-2009 | 1 | First release |
| 23-Jul-2009 | 2 | Marking on device summary has been corrected. |
| 13-Jul-2012 | 3 | Updated title on the cover page. Minor text changes. Updated <i>Section 4: Package mechanical data</i> and <i>Section 5: Packing mechanical data</i> . |

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY TWO AUTHORIZED ST REPRESENTATIVES, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2012 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com

