



# STD9N10 STD9N10-1

## N-CHANNEL 100V - 0.23 $\Omega$ - 9A DPAK/IPAK POWER MOS TRANSISTOR

**Table 1. General Features**

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STD9N10	100 V	< 0.27 $\Omega$	9 A
STD9N10-1	100 V	< 0.27 $\Omega$	9 A

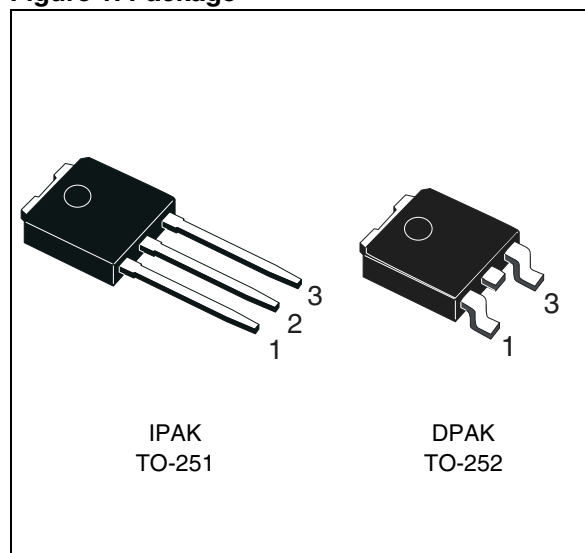
### FEATURES SUMMARY

- TYPICAL R<sub>DS(on)</sub> = 0.23  $\Omega$
- AVALANCHE RUGGED TECHNOLOGY
- 100% AVALANCHE TESTED
- REPETITIVE AVALANCHE DATA AT 100°C
- LOW GATE CHARGE
- HIGH CURRENT CAPABILITY
- 175°C OPERATING TEMPERATURE
- APPLICATION ORIENTED CHARACTERIZATION
- THROUGH-HOLE IPAK (TO-251) POWER PACKAGE IN TUBE (SUFFIX "-1")
- SURFACE-MOUNTING DPAK (TO-252) POWER PACKAGE IN TAPE & REEL (SUFFIX "T4")

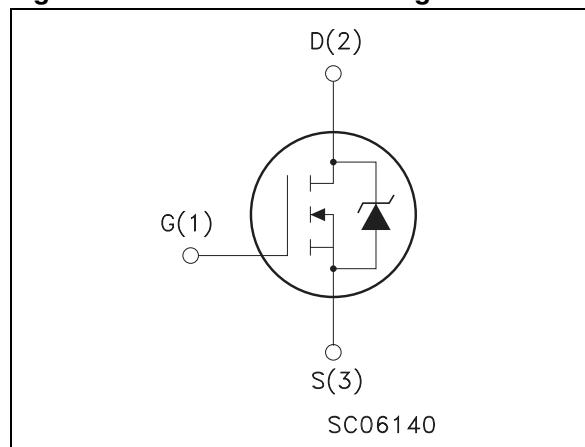
### APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- SOLENOID AND RELAY DRIVERS
- REGULATORS
- DC-DC & DC-AC CONVERTERS
- MOTOR CONTROL, AUDIO AMPLIFIERS
- AUTOMOTIVE ENVIRONMENT (INJECTION, ABS, AIR-BAG, LAMPDRIVERS, Etc.)

**Figure 1. Package**



**Figure 2. Internal Schematic Diagram**



**Table 2. Order Codes**

Part Number	Marking	Package	Packaging
STD9N10T4	D9N10	DPAK	TAPE & REEL
STD9N10-1	D9N10	IPAK	TUBE

**Table 3. Absolute Maximum Ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source Voltage ( $V_{GS} = 0$ )	100	V
$V_{DGR}$	Drain- gate Voltage ( $R_{GS} = 20\text{ k}\Omega$ )	100	V
$V_{GS}$	Gate-source Voltage	$\pm 20$	V
$I_D$	Drain Current (cont.) at $T_C = 25\text{ }^\circ\text{C}$	9	A
$I_D$	Drain Current (cont.) at $T_C = 100\text{ }^\circ\text{C}$	6	A
$I_{DM}^{(1)}$	Drain Current (pulsed)	36	A
$P_{tot}$	Total Dissipation at $T_C = 25\text{ }^\circ\text{C}$	45	W
	Derating Factor	0.3	W/ $^\circ\text{C}$
$T_{stg}$	Storage Temperature	-65 to 175	$^\circ\text{C}$
$T_j$	Max. Operating Junction Temperature	175	$^\circ\text{C}$

Note: 1. Pulse width limited by safe operating area.

**Table 4. Thermal Data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal Resistance Junction-case Max	3.33	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal Resistance Junction-ambient Max	100	$^\circ\text{C}/\text{W}$
$T_l$	Maximum Lead Temperature For Soldering Purpose	275	$^\circ\text{C}$

**Table 5. Avalanche Characteristics**

Symbol	Parameter	Max Value	Unit
$I_{AR}$	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by $T_j$ max, $\delta < 1\%$ )	9	A
$E_{AS}$	Single Pulse Avalanche Energy (starting $T_j = 25\text{ }^\circ\text{C}$ ; $I_D = I_{AR}$ ; $V_{DD} = 25\text{ V}$ )	30	mJ
$E_{AR}$	Repetitive Avalanche Energy (pulse width limited by $T_j$ max, $\delta < 1\%$ )	7	mJ
$I_{AR}$	Avalanche Current, Repetitive or Not-Repetitive ( $T_C = 100\text{ }^\circ\text{C}$ , pulse width limited by $T_j$ max, $\delta < 1\%$ )	6	A

**ELECTRICAL CHARACTERISTICS** ( $T_{case} = 25^{\circ}C$  unless otherwise specified)

**Table 6. Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 250 \mu A; V_{GS} = 0$	100			V
$I_{DSS}$	Zero Gate Voltage	$V_{DS} = \text{Max Rating}$			250	$\mu A$
	Drain Current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating} \times 0.8; T_c = 125^{\circ}C$			1000	$\mu A$
$I_{GSS}$	Gate-body Leakage Current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20 V$			$\pm 100$	nA

**Table 7. On (1)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}; I_D = 250 \mu A$	2	3	4	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10V; I_D = 4.5 A$		0.23	0.27	$\Omega$
		$V_{GS} = 10V; I_D = 4.5 A; T_c = 100^{\circ}C$			0.54	$\Omega$

Note: 1. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %

**Table 8. Dynamic**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward Transconductance	$V_{DS} > I_{D(on)} \times R_{DS(on)max}; I_D = 4.5 A$	2	4		S
$C_{iss}$	Input Capacitance	$V_{DS} = 25 V; f = 1 MHz; V_{GS} = 0$		330	450	pF
$C_{oss}$	Output Capacitance			90	120	pF
$C_{rss}$	Reverse Transfer Capacitance			25	40	pF

Note: 1. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %

**Table 9. Switching On**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Time	$V_{DD} = 50 V; I_D = 4.5 A; R_G = 4.7 \Omega$		10	15	ns
$t_r$	Rise Time	$V_{GS} = 10 V$ (see test circuit, Figure 22)		40	60	ns
$(di/dt)_{on}$	Turn-on Current Slope	$V_{DD} = 80 V; I_D = 9 A; R_G = 4.7 \Omega$ $V_{GS} = 10 V$ (see test circuit, Figure 22)		440		A/ $\mu s$
$Q_g$	Total Gate Charge	$V_{DD} = 80 V; I_D = 9 A; V_{GS} = 10 V$		15	25	nC
$Q_{gs}$	Gate-Source Charge			6		nC
$Q_{gd}$	Gate-Drain Charge			5		nC

**Table 10. Switching Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 80 V; I_D = 9 A; R_G = 4.7 \Omega$		15	25	ns
$t_f$	Fall Time	$V_{GS} = 10 V$ (see test circuit, Figure 24)		25	35	ns
$t_c$	Cross-over Time			50	70	ns

Table 11. Source Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				9	A
$I_{SDM}^{(1)}$	Source-drain Current (pulsed)				36	A
$V_{SD}^{(2)}$	Forward On Voltage	$I_{SD} = 9\text{ A}; V_{GS} = 0$			1.5	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 9\text{ A}; di/dt = 100\text{ A}/\mu\text{s}$		80		ns
$Q_{rr}$	Reverse Recovery Charge	$V_{DD} = 20\text{ V}; T_j = 150\text{ }^\circ\text{C}$ (see test circuit, Figure 24)		0.2		$\mu\text{C}$
$I_{RRAM}$	Reverse Recovery Current			5		A

Note: 1. Pulse width limited by safe operating area  
 2. Pulsed: Pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5 %

Figure 3. Safe Operating Area

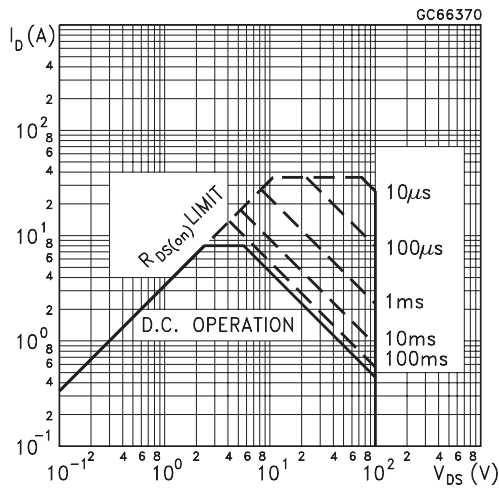


Figure 4. Thermal Impedance

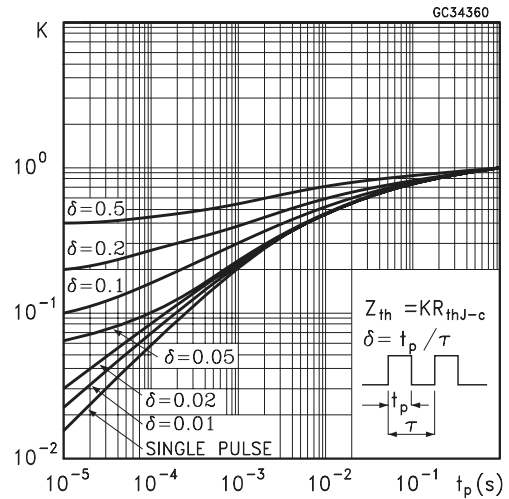


Figure 5. Derating Curve

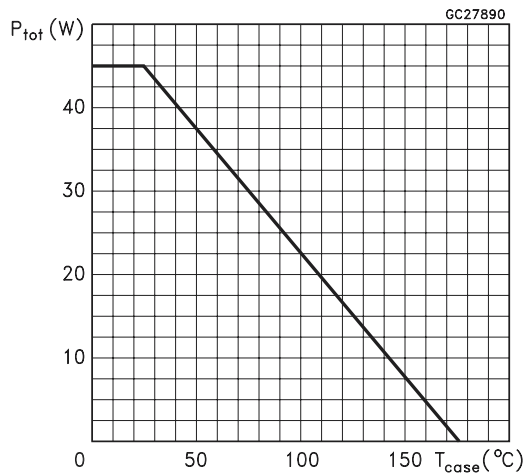


Figure 6. Output Characteristics

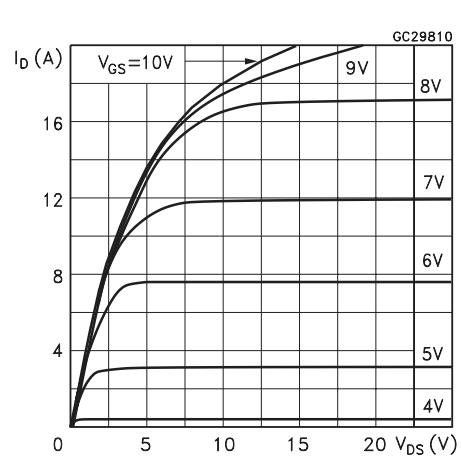


Figure 7. Transfer Characteristics

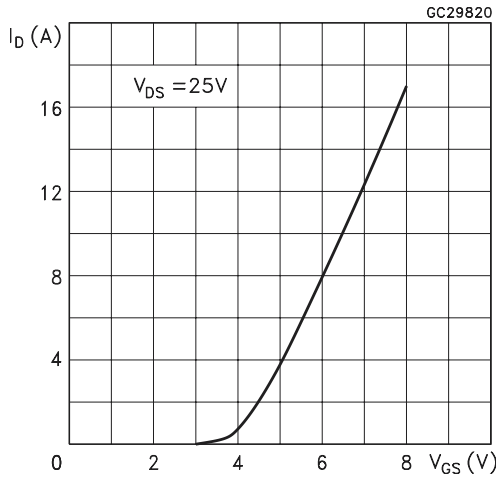


Figure 8. Transconductance

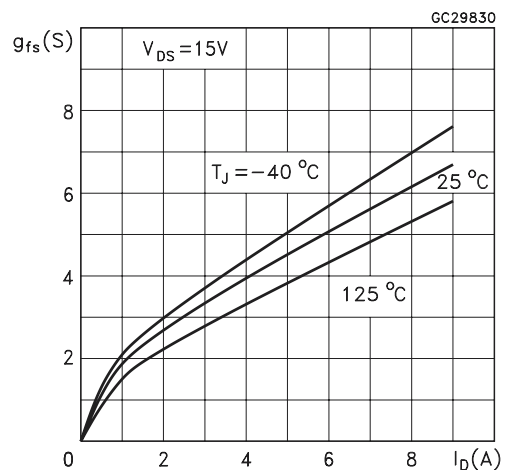


Figure 9. Static Drain-source On Resistance

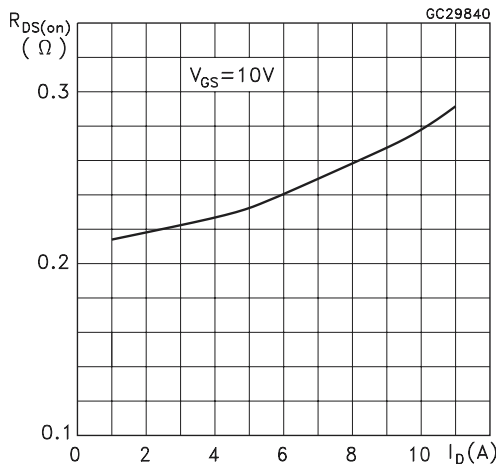


Figure 10. Gate Charge vs Gate-source Voltage

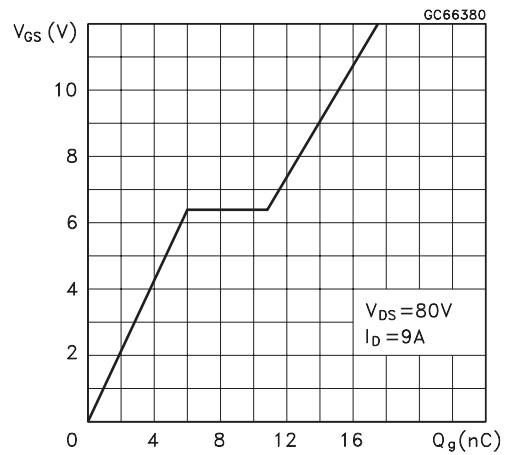


Figure 11. Capacitance Variations

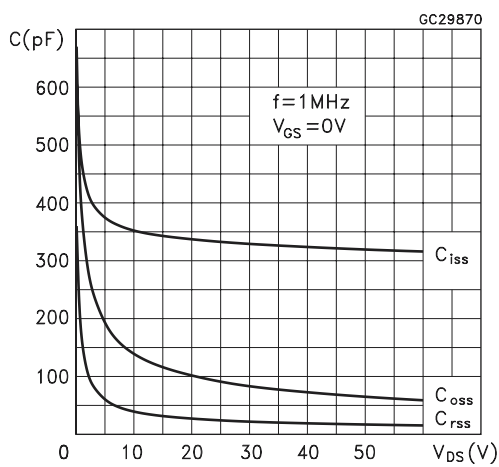


Figure 12. Normalized Gate Threshold Voltage vs Temperature

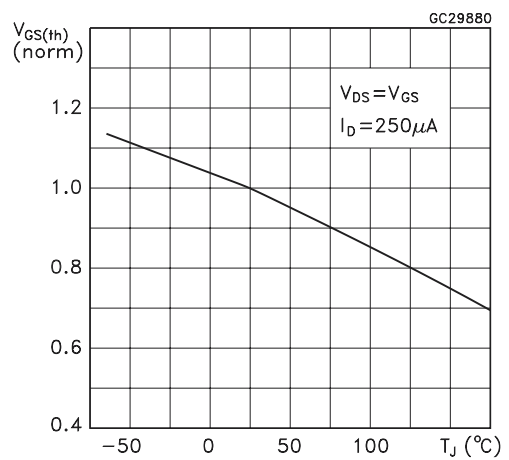


Figure 13. Normalized On Resistance vs Temperature

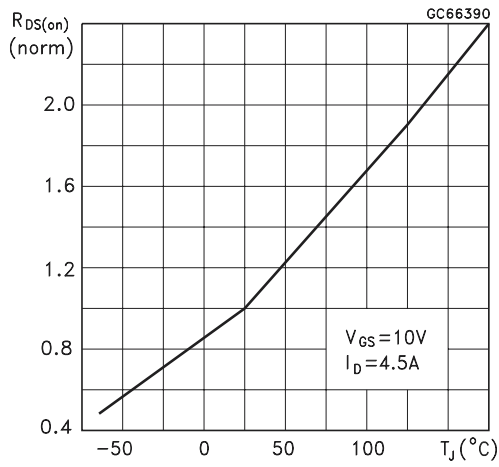


Figure 14. Turn-on Current Slope

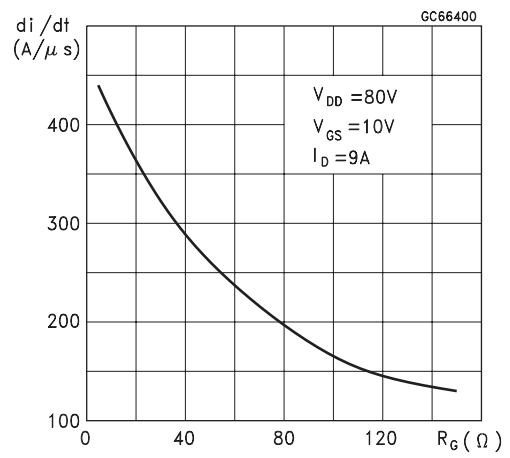


Figure 15. Turn-off Drain-source Voltage Slope

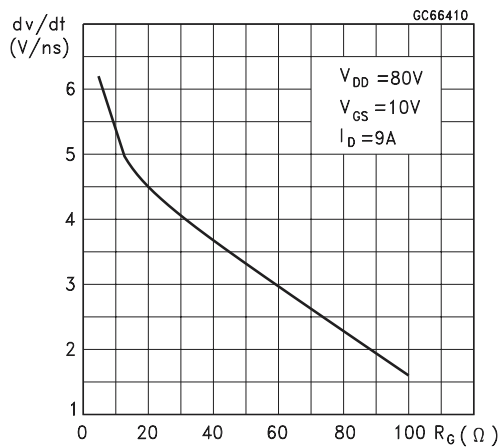


Figure 16. Cross-over Time

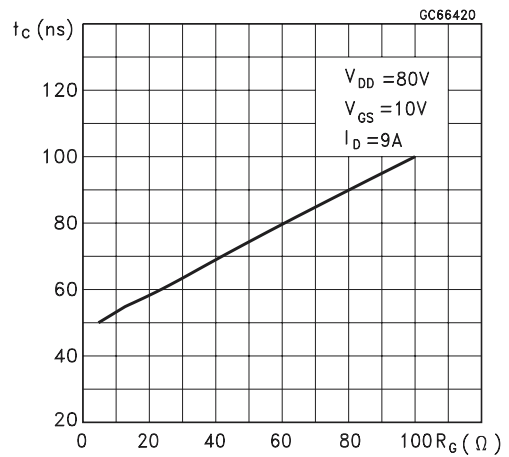


Figure 17. Switching Safe Operating Area

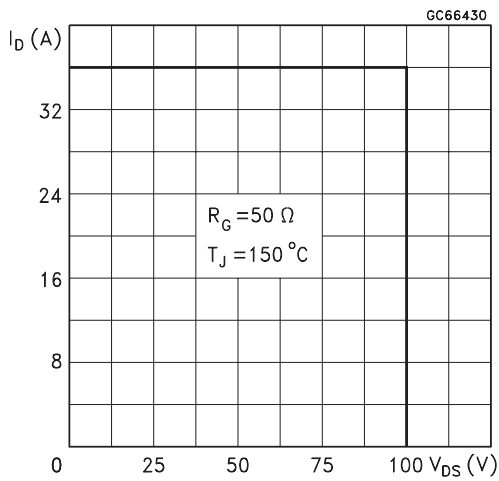
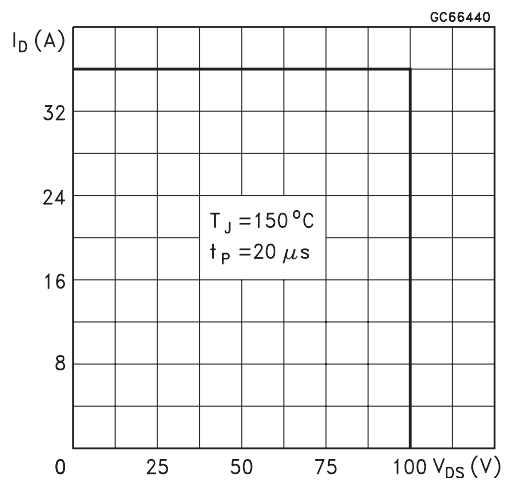


Figure 18. Accidental Overload Area



**Figure 19. Source-drain Diode Forward Characteristics**

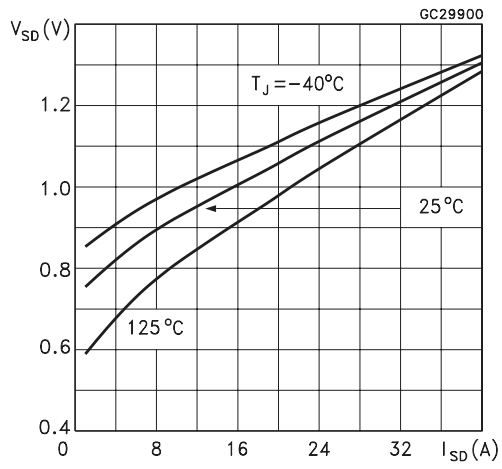


Figure 20. Unclamped Inductive Load Test Circuit

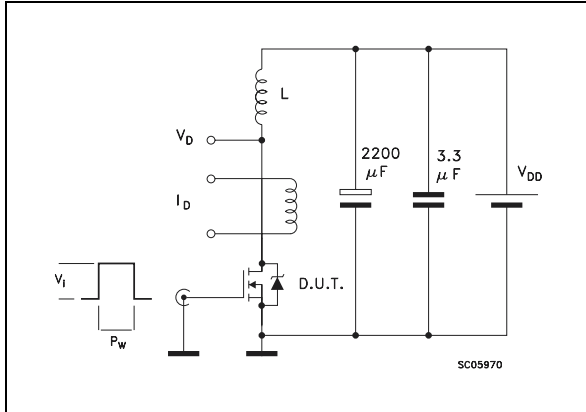


Figure 21. Unclamped Inductive Waveforms

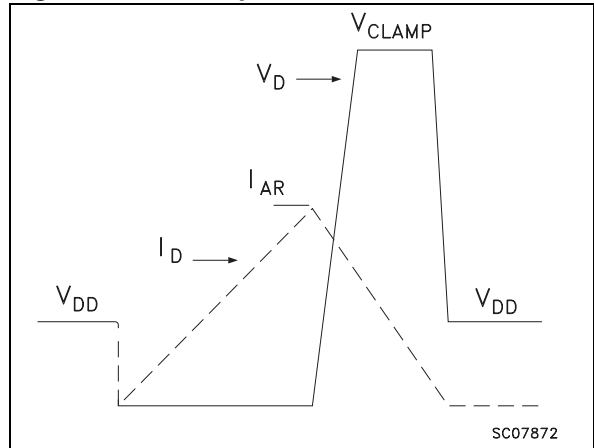


Figure 22. Switching Times Test Circuits For Resistive Load

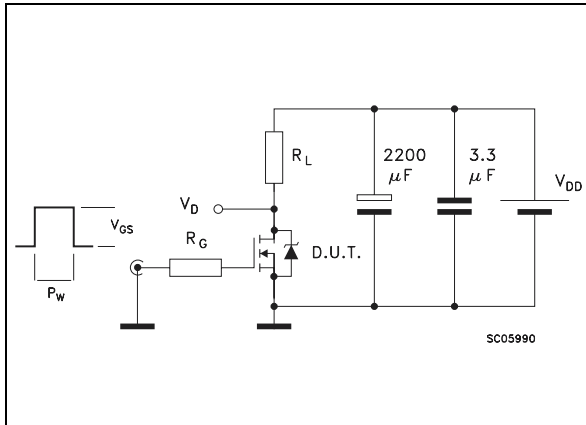


Figure 23. Gate Charge Test Circuit

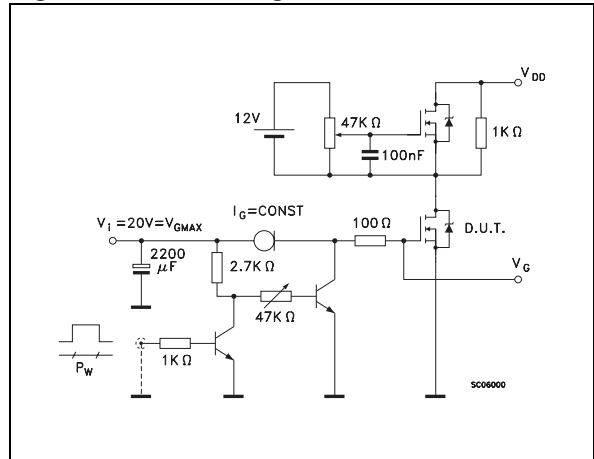
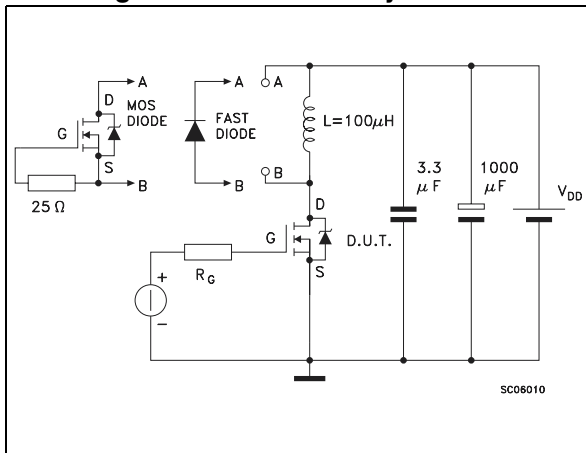


Figure 24. Test Circuit For Inductive Load Switching And Diode Recovery Times



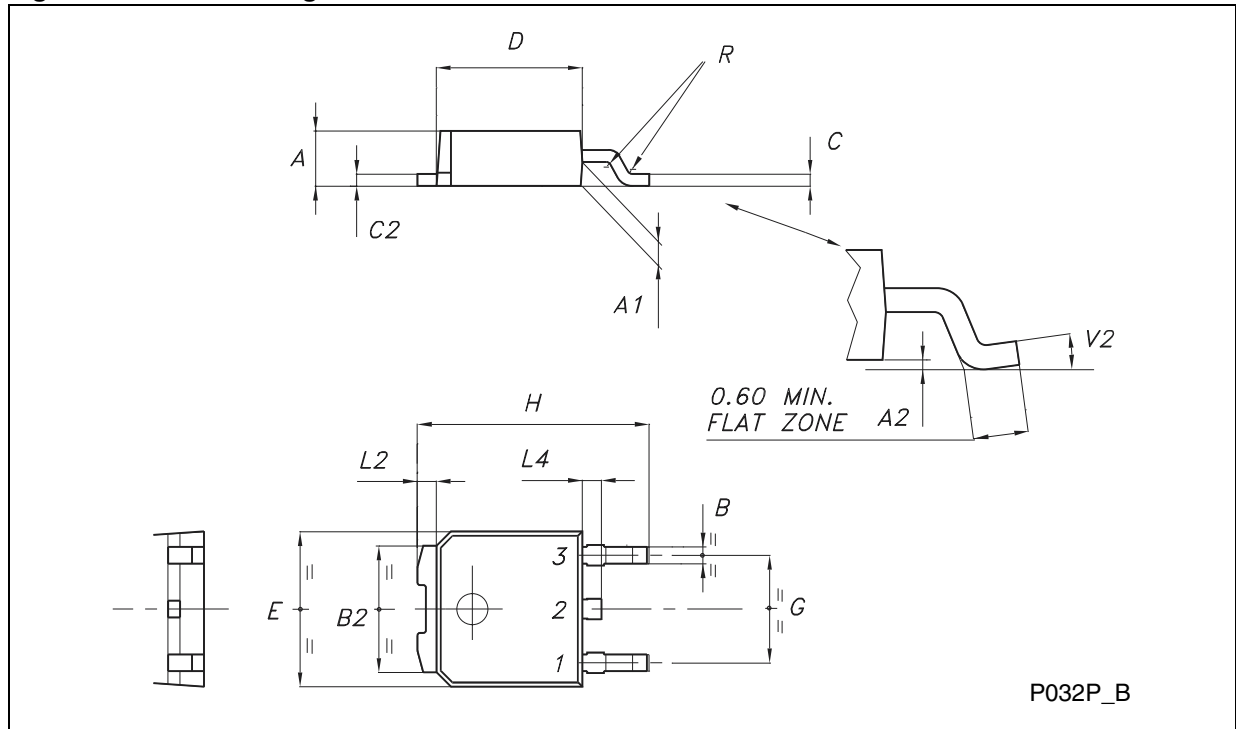


PACKAGE MECHANICAL

Table 12. DPAK Mechanical Data

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018	0.024	
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°

Figure 25. DPAK Package Dimensions



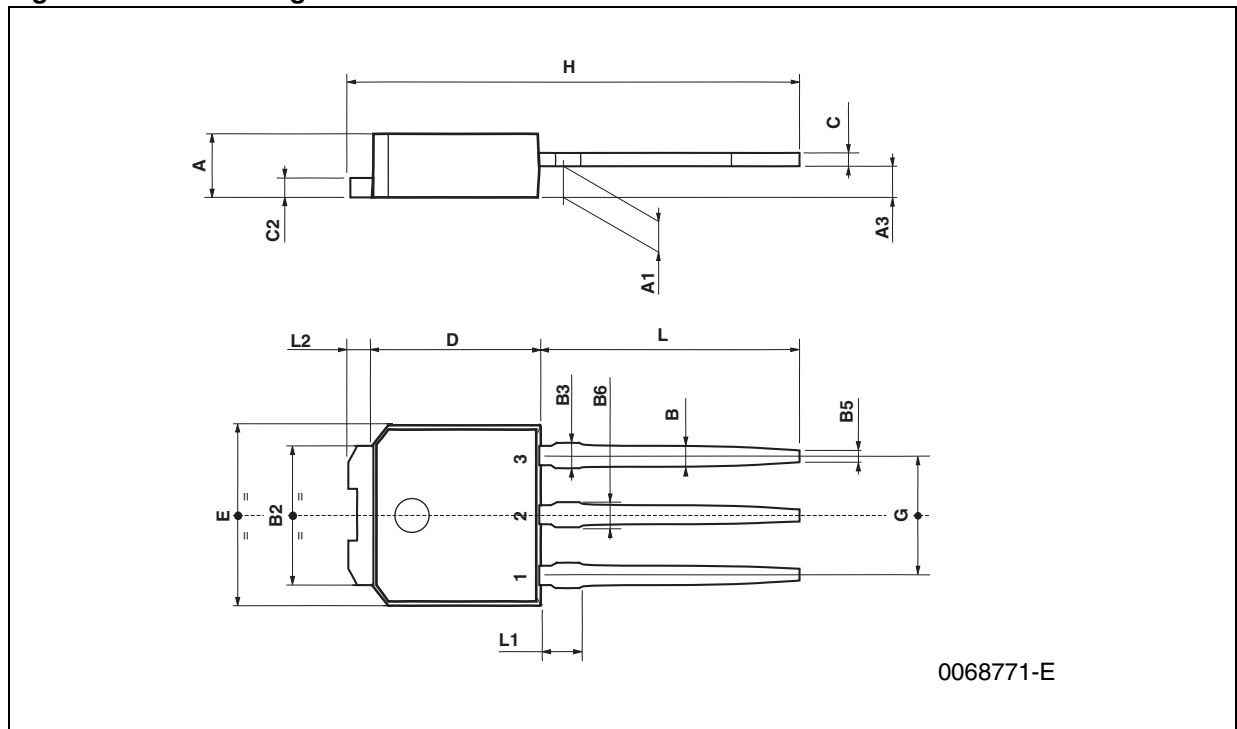
Note: Drawing is not to scale.

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**Table 13. IPAK Mechanical Data**

Symbol	millimeters			inches		
	Min	Typ	Max	Min	Typ	Max
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.63			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039

**Figure 26. IPAK Package Dimensions**



Note: Drawing is not to scale.

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**REVISION HISTORY****Table 14. Revision History**

<b>Date</b>	<b>Revision</b>	<b>Description of Changes</b>
March-1996	1	First Issue
3-May-2004	2	Stylesheet update. No content change.

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