STDP4020, STDP4010
DisplayPort receiver

Datasheet

Rev A

MegaChips

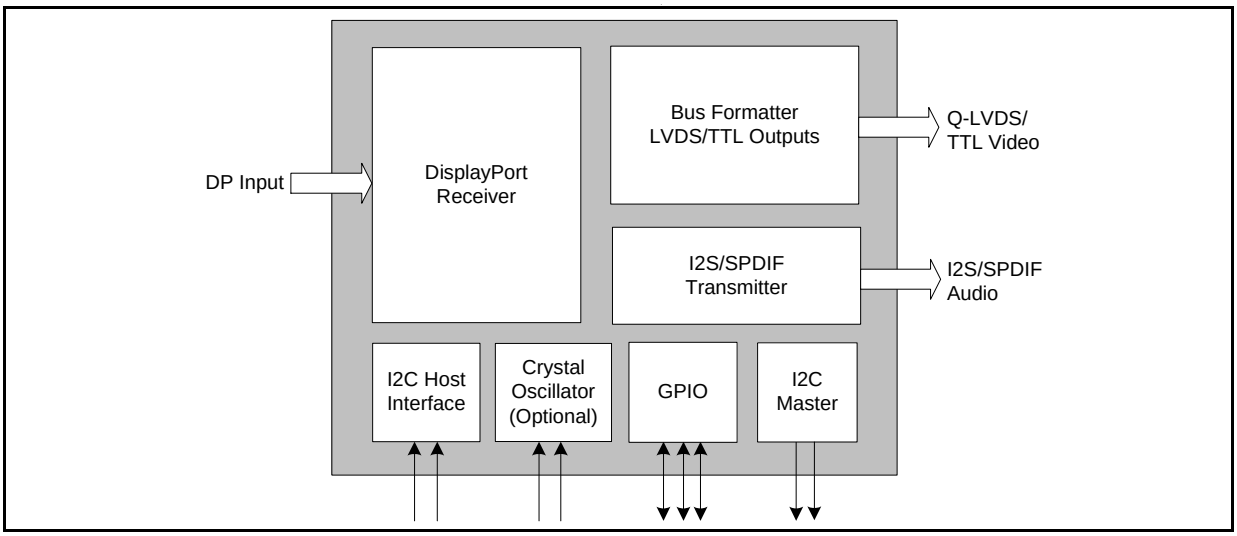
MegaChips' Proprietary Information

Features

- Enhanced DisplayPort® (DP) receiver
  - DP 1.1a compliant
  - Embedded DisplayPort (eDP) compliant
  - 1, 2, or 4 lanes
- Higher bandwidth “Turbo mode” (3.24 Gbps per lane), supports:
  - 1920 x 1080 (FHD) 120 Hz/10-bit color video standard timings and 7.1 Ch audio
  - 2560 x 1600 (WQXGA), 2560 x 2048 (QSXGA) 60 Hz/10-bit color graphics and 7.1 Ch audio
- Interface compatibility with wide range of display controller ICs
  - LVTTL (60 wide) and LVDS (quad bus) video interface
  - 8-Ch I2S and SPDIF audio interface
- Robust AUX channel
  - Link service, maintenance
  - I2C-over-AUX (MCCS, DDC)
  - IR, full duplex UART protocol
- Configurable through I2C host interface
- Supports HDCP 1.3 with on-chip keys
- HDCP repeater capability
  - Acts as upstream receiver
- AUX to I2C bridge for EDID, MCCS pass through
- Spread spectrum on DisplayPort, LVDS, and TTL interfaces for EMI reduction
- Supports deep color and color format conversion
  - RGB/YUV (4:4:4) – 10-bit color
  - YUV (4:2:2/4:2:0) – 12-bit color
  - RGB (4:4:4) to YUV (4:4:4) conversion and vice-versa
- Supports HBR/“Turbo” speed over HBR/RBR-rated long cables (15 m and more)
- Package
  - 164 LFBGA (12 x 12 mm / 0.8 mm)
- Power supply voltages
  - 3.3 V I/O; 1.2 V core

Applications

- Digital TV, LCD monitor, mobile display, projector, etc



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1. Description

The STDP4020 is a DisplayPort receiver IC for the reception of secure, high-bandwidth uncompressed digital audio-video signals targeted for applications such as DTV, LCD monitor, projector, and other types of display systems. STDP4020 is a VESA DP 1.1a and eDP compliant device, implementing a single link DisplayPort input port comprising four main lanes, auxiliary channel, and HPD. In addition to the standard HBR (2.7 Gbps) and RBR (1.62 Gbps) speeds, this device supports turbo speed of 3.24 Gbps per lane with a total link bandwidth of 12.96 Gbps. The higher bandwidth provides unique benefits to users over other commercial DP receivers for embedded applications by offering additional margin to support higher color depth, resolution, and refresh rate. For example, STDP4020 supports FHD non-reduced blanking video (1080p 30-bit color per pixel) at 120 Hz, plus 7.1 Ch audio for two-box TV applications.The advanced equalizer built in this device offers guaranteed performance over long reach cables. The auxiliary channel in STDP4020 acts as a bidirectional communication link, supporting application-specific protocols such as MCCS, DDC, UART, IR, as well as the dedicated DisplayPort link training and device management functions.

The STDP4020 supports RGB and YUV video color formats with color depth of 12 (YUV 4:2:2 only), 10, and 8 bits. This device offers LVDS and LVTTL output interfaces configurable to map a wide range of display controller products. The Quad LVDS interface supports video signals up to 400 MHz pixel rate with flexible channel and lane swapping options. The 60-bit LVTTL output ports can be mapped to transfer video data either in two pixels per clock or single pixel per clock up to 330 MHz pixel rate, which opens up possibilities for 3D applications. The STDP4020 also supports both compressed and uncompressed audio formats. The extracted audio signal is transferred on a digital audio output bus. This device comprises four I2S audio output, supporting up to 8 channel LPCM audio and a single wire S/PDIF output for encoded audio. The STDP4020 features the HDCP 1.3 content protection scheme with an embedded key option for secure reception of digital audio-video content. In addition, it also supports the HDCP repeater function and, thus acts as an upstream receiver suitable for two-box TV and HDMI/DVI converter applications.

The STDP4020 is configurable from an external host controller through I2C host interface. This IC also includes general-purpose inputs/outputs for controlling system components. The STDP4020 features a color space converter (RGB to YUV and YUV to RGB) for flexible interface with external video processing devices.

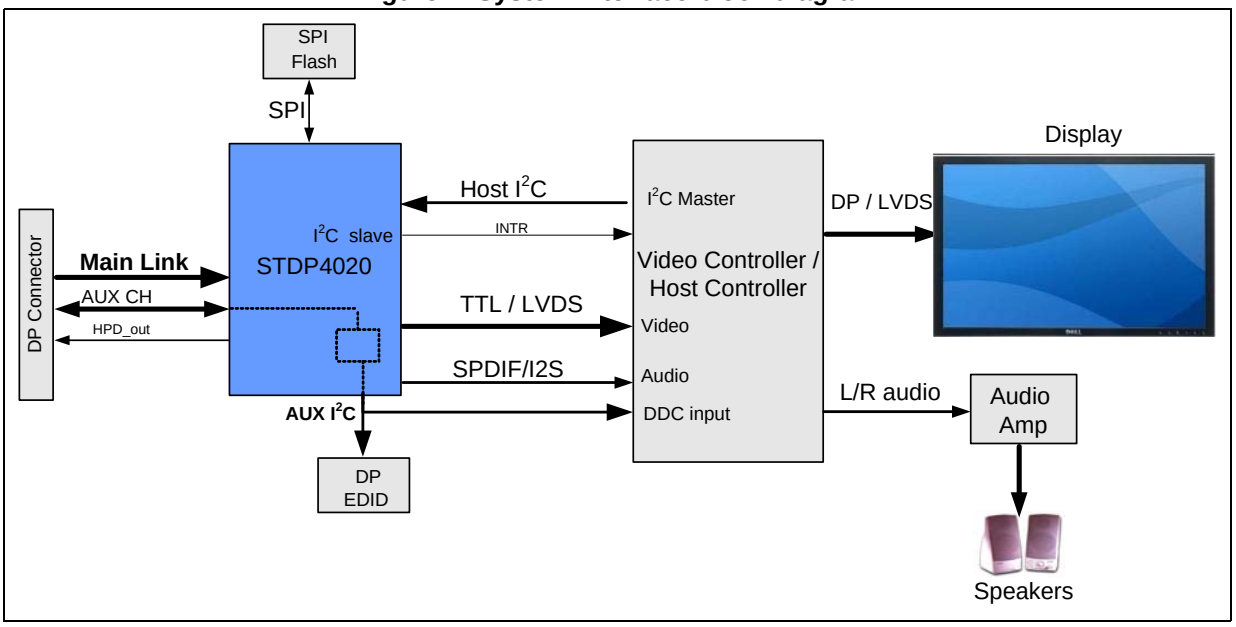
STDP4020 family product includes the following part numbers:

Part number	Video input	Video output	Max video resolution
STDP4020	4 lanes DisplayPort	4 Ch LVDS/60 LVTTL	WQXGA/FHD 120 Hz
STDP4010	2 lanes DisplayPort	2 Ch LVDS/30 LVTTL	WUXGA/FHD 60 Hz

2. Application overview

The STDP4020 is designed as a DisplayPort front-end capture device for display applications. Typical display design has a display controller (scaler) that acts as system master (host). The host controller configures STDP4020 through a 2-wire host interface. The host and STDP4020 also use interrupt mechanism whenever the slave needs attention. The STDP4020 may require an external SPI Flash to store firmware for supporting custom specific applications. The audio and video output from STDP4020 can directly interface to the host display controller for further processing. The AUX I2C bypass channel handles the I2C traffic between STDP4020 and host controller, as shown in the figure below.

Figure 1. System interface block diagram



3. Feature attributes

- Enhanced DisplayPort (DP) receiver compliant with DP1.1a and embedded (eDP) specification
- Supports higher bandwidth mode called “Turbo mode” (3.24 Gbps per lane) for embedded applications. For example, supports FHD 120 Hz-10/12-bit video or QSXGA (2560 x 2048) 60 Hz/10-bit color graphics and 7.1 Ch audio
- Interface compatibility with wide range of display products. Supports LVTTL (60 wide) and quad LVDS video interface
- Supports I2S 8 Ch and SPDIF audio output interface compliant with IEC60958 and IEC61937 audio formats.
- Robust AUX channel for Link service, maintenance and supports I2C over AUX, MCCS, DDC, IR and full duplex UART protocol
- Supports HDCP 1.3 with on-chip key storage
- Acts HDCP repeater for an upstream receiver
- Supports AUX to I2C bridge for EDID, MCCS pass through
- Spread spectrum on DisplayPort, LVDS and TTL interfaces for EMI reduction
- Supports deep color and color format conversion: RGB (4:4:4) to YUV (4:4:4) and vice-versa
- Supports TTL up to 330 MHz pixel clock, which allows 3D video applications
- Supports HBR/“Turbo” speed over HBR/RBR rated long cables (15 m and more)
- Configurable through I2C host interface
- Package: 164 LFBGA (12 x 12 mm / 0.8 mm)
- Power supply voltages: 3.3 V I/O; 1.2 V core

4. BGA footprint and pin lists

4.1 Ball grid array diagram

The ball grid array (BGA) diagrams give the allocation of pins to the package, shown from the top looking down using the PCB footprint.

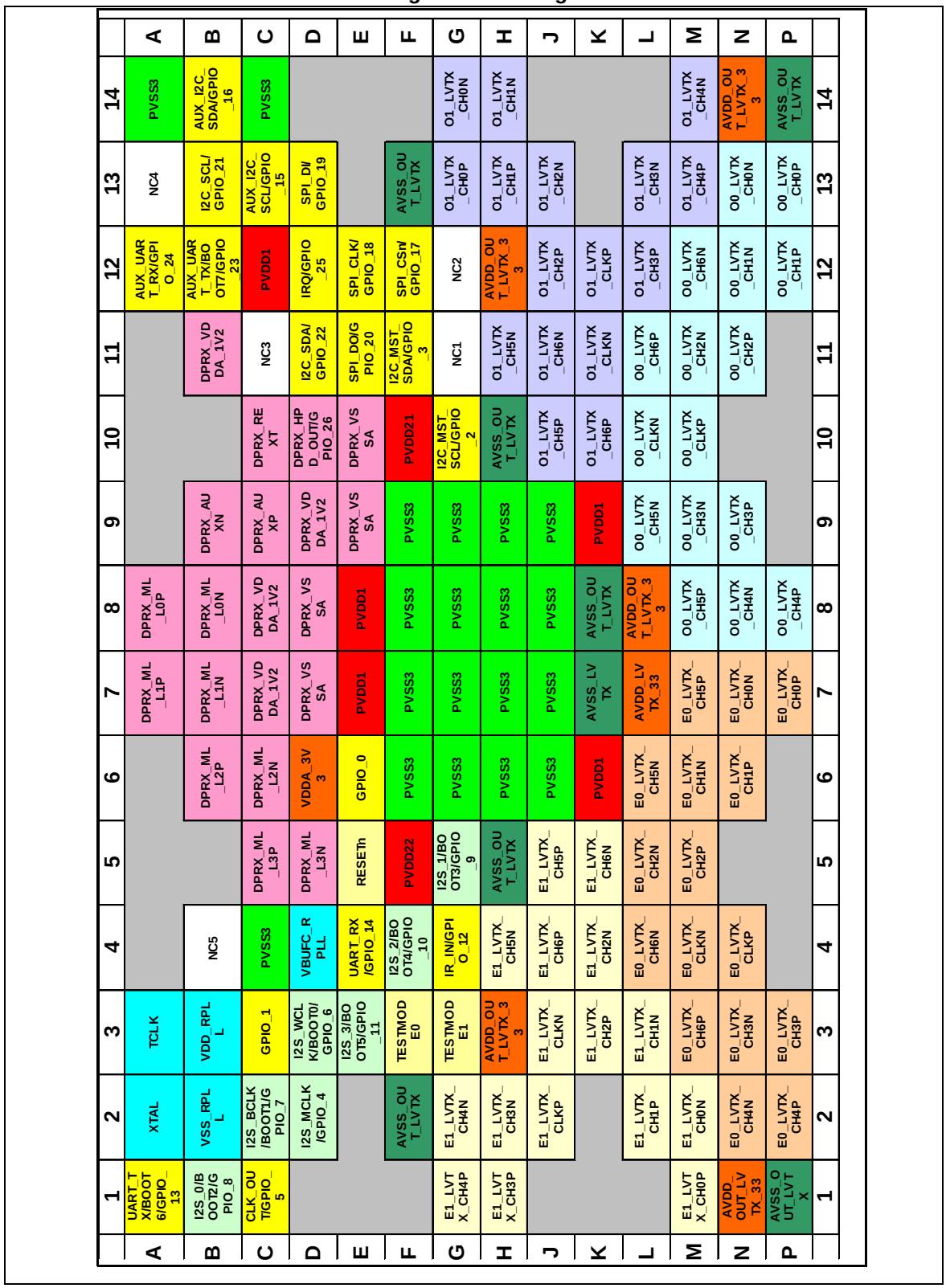
Some signal names in BGA diagrams have been abbreviated. Refer to*Table 2: Pin list on page 12* for full signal names sorted by pin number.

Table 1. Key to BGA diagrams

Function	Type	Key
DisplayPort input	SIG	
Reference clocks	SIG	
System controls	SIG	
Multi-function and system interface connections	SIG	
I2S/SPDIF audio output	SIG	
LVDS/TTL Output_Even-0	SIG	
LVDS/TTL Output_Even-1	SIG	
LVDS/TTL Output_Odd-0	SIG	
LVDS/TTL Output_Odd-1	SIG	
Analog power	VCC/VDD	
Analog ground	VSS/GND	
System power	VCC/VDD	
System ground	VSS/GND	
No connect/Do not connect	NC/DNC	
No ball		

The STDP4020 is available in a 164-pin LFBGA package.

Figure 2. Pin diagram



4.2 Full pin list sorted by pin number

Table 2. Pin list

Pin number	Net name
A1	UART_TX/BOOT[6]/GPIO_13
A2	XTAL
A3	TCLK
A7	DPRX_ML_L1P
A8	DPRX_ML_L0P
A12	AUX_UART_RX/GPIO_24
A13	NC4
A14	PVSS3
B1	I2S_0/BOOT[2]/GPIO_8
B2	VSS_RPLL
B3	VDD_RPLL
B4	NC5
B6	DPRX_ML_L2P
B7	DPRX_ML_L1N
B8	DPRX_ML_L0N
B9	DPRX_AUXN
B11	DPRX_VDDA_1V2
B12	AUX_UART_TX/BOOT[7]/GPIO_23
B13	I2C_SCL/GPIO_21
B14	AUX_I2C_SDA/GPIO_16
C1	CLK_OUT/GPIO_5
C2	I2S_BCLK/BOOT[1]/GPIO_7
C3	GPIO_1
C4	PVSS3
C5	DPRX_ML_L3P
C6	DPRX_ML_L2N
C7, C8	DPRX_VDDA_1V2
C9	DPRX_AUXP
C10	DPRX_REXT
C11	NC3
C12	PVDD1
C13	AUX_I2C_SCL/GPIO_15
C14	PVSS3

Table 2. Pin list (continued)

Pin number	Net name
D2	I2S_MCLK/GPIO_4
D3	I2S_WCLK/BOOT[0]/GPIO_6
D4	VBUFC_RPLL
D5	DPRX_ML_L3N
D6	VDDA_3V3
D7, D8	DPRX_VSSA
D9	DPRX_VDDA_1V2
D10	DPRX_HPD_OUT/GPIO_26
D11	I2C_SDA/GPIO_22
D12	IRQ/GPIO_25
D13	SPI_DI/GPIO_19
E3	I2S_3/BOOT[5]/GPIO_11
E4	UART_RX/GPIO_14
E5	RESETn
E6	GPIO_0
E7, E8	PVDD1
E9, E10	DPRX_VSSA
E11	SPI_DO/GPIO_20
E12	SPI_CLK/GPIO_18
F2	AVSS_OUT_LVTX
F3	TESTMODE0
F4	I2S_2/BOOT[4]/GPIO_10
F5	PVDD22
F6, F7, F8, F9	PVSS3
F10	PVDD21
F11	I2C_MST_SDA/GPIO_3
F12	SPI_CSn/GPIO_17
F13	AVSS_OUT_LVTX
G1	E1_LVTX_CH4P
G2	E1_LVTX_CH4N
G3	TESTMODE1
G4	IR_IN/GPIO_12
G5	I2S_1/BOOT[3]/GPIO_9
G6, G7, G8, G9	PVSS3
G10	I2C_MST_SCL/GPIO_2

Table 2. Pin list (continued)

Pin number	Net name
G11	NC1
G12	NC2
G13	O1_LVTX_CH0P
G14	O1_LVTX_CH0N
H1	E1_LVTX_CH3P
H2	E1_LVTX_CH3N
H3	AVDD_OUT_LVTX_33
H4	E1_LVTX_CH5N
H5	AVSS_OUT_LVTX
H6, H7, H8, H9	PVSS3
H10	AVSS_OUT_LVTX
H11	O1_LVTX_CH5N
H12	AVDD_OUT_LVTX_33
H13	O1_LVTX_CH1P
H14	O1_LVTX_CH1N
J2	E1_LVTX_CLKP
J3	E1_LVTX_CLKN
J4	E1_LVTX_CH6P
J5	E1_LVTX_CH5P
J6, J7, J8, J9	PVSS3
J10	O1_LVTX_CH5P
J11	O1_LVTX_CH6N
J12	O1_LVTX_CH2P
J13	O1_LVTX_CH2N
K3	E1_LVTX_CH2P
K4	E1_LVTX_CH2N
K5	E1_LVTX_CH6N
K6	PVDD1
K7	AVSS_LVTX
K8	AVSS_OUT_LVTX
K9	PVDD1
K10	O1_LVTX_CH6P
K11	O1_LVTX_CLKN
K12	O1_LVTX_CLKP
L2	E1_LVTX_CH1P

Table 2. Pin list (continued)

Pin number	Net name
L3	E1_LVTX_CH1N
L4	E0_LVTX_CH6N
L5	E0_LVTX_CH2N
L6	E0_LVTX_CH5N
L7	AVDD_LVTX_33
L8	AVDD_OUT_LVTX_33
L9	O0_LVTX_CH5N
L10	O0_LVTX_CLKN
L11	O0_LVTX_CH6P
L12	O1_LVTX_CH3P
L13	O1_LVTX_CH3N
M1	E1_LVTX_CH0P
M2	E1_LVTX_CH0N
M3	E0_LVTX_CH6P
M4	E0_LVTX_CLKN
M5	E0_LVTX_CH2P
M6	E0_LVTX_CH1N
M7	E0_LVTX_CH5P
M8	O0_LVTX_CH5P
M9	O0_LVTX_CH3N
M10	O0_LVTX_CLKP
M11	O0_LVTX_CH2N
M12	O0_LVTX_CH6N
M13	O1_LVTX_CH4P
M14	O1_LVTX_CH4N
N1	AVDD_OUT_LVTX_33
N2	E0_LVTX_CH4N
N3	E0_LVTX_CH3N
N4	E0_LVTX_CLKP
N6	E0_LVTX_CH1P
N7	E0_LVTX_CH0N
N8	O0_LVTX_CH4N
N9	O0_LVTX_CH3P
N11	O0_LVTX_CH2P
N12	O0_LVTX_CH1N

Table 2. Pin list (continued)

Pin number	Net name
N13	O0_LVTX_CH0N
N14	AVDD_OUT_LVTX_33
P1	AVSS_OUT_LVTX
P2	E0_LVTX_CH4P
P3	E0_LVTX_CH3P
P7	E0_LVTX_CH0P
P8	O0_LVTX_CH4P
P12	O0_LVTX_CH1P
P13	O0_LVTX_CH0P
P14	AVSS_OUT_LVTX

5. Connections

5.1 Pin list

I/O Legend: I = Input; O = Output; P = Power; G = Ground

Note: Some pins can have multiple functionalities, which are configured under register control. The alternate functionality for each pin is listed in the Description column.

Table 3. DisplayPort receiver pins

Pin	Assignment	I/O	Description
B8	DPRX_ML_L0N	I	DisplayPort Receiver Main Link Lane 0 Negative Analog Input
A8	DPRX_ML_L0P	I	DisplayPort Receiver Main Link Lane 0 Positive Analog Input
B7	DPRX_ML_L1N	I	DisplayPort Receiver Main Link Lane 1 Negative Analog Input
A7	DPRX_ML_L1P	I	DisplayPort Receiver Main Link Lane 1 Positive Analog Input
C6	DPRX_ML_L2N	I	DisplayPort Receiver Main Link Lane 2 Negative Analog Input
B6	DPRX_ML_L2P	I	DisplayPort Receiver Main Link Lane 2 Positive Analog Input
D5	DPRX_ML_L3N	I	DisplayPort Receiver Main Link Lane 3 Negative Analog Input
C5	DPRX_ML_L3P	I	DisplayPort Receiver Main Link Lane 3 Positive Analog Input
B9	DPRX_AUXN	I/O	DisplayPort Receiver Auxiliary Channel Negative Analog Input/Output
C9	DPRX_AUXP	I/O	DisplayPort Receiver Auxiliary Channel Positive Analog Input/Output
D10	DPRX_HPD_OUT/GPIO_26	I/O	DisplayPort Receiver Hot Plug Detect Output
			General Purpose Schmitt Trigger Input / Tri-state Output 26 [5 V Tolerant]
C10	DPRX_REXT	I	Termination calibration reference resistor; 240 ohm 1% resistor should be connected from this pin to 1.2 V analog power supply.

Table 4. Reference clocks

Pin	Assignment	I/O	Description
A2	XTAL	I/O	Crystal Oscillator Input. Connect to external crystal.
A3	TCLK	I/O	Reference Clock (TCLK) from a 27MHz Crystal or TTL Oscillator. Connect to external crystal or oscillator.
D4	VBUFC_RPLL	O	Analog Test Pin for Internal Clocks.

Table 5. Digital video outputs - LVDS & TTL (suggested mapping)

Pin	Assignment	I/O	Description
M3	E0_LVTX_CH6P	O	Positive output of LVDS TX E0 Channel 6
			Even Green Channel Data 8
L4	E0_LVTX_CH6N	O	Negative output of LVDS TX E0 Channel 6
			Even Green Channel Data 9
M7	E0_LVTX_CH5P	O	Positive output of LVDS TX E0 Channel 5
			Even Red Channel Data 8
L6	E0_LVTX_CH5N	O	Negative output of LVDS TX E0 Channel 5
			Even Red Channel Data 9
P2	E0_LVTX_CH4P	O	Positive output of LVDS TX E0 Channel 4
			Even Blue Channel Data 0
N2	E0_LVTX_CH4N	O	Negative output of LVDS TX E0 Channel 4
			Even Blue Channel Data 1
P3	E0_LVTX_CH3P	O	Positive output of LVDS TX E0 Channel 3
			Even Blue Channel Data 4
N3	E0_LVTX_CH3N	O	Negative output of LVDS TX E0 Channel 3
			Even Blue Channel Data 5
N4	E0_LVTX_CLKP	O	Positive output of LVDS TX E0 Clock Channel
			Even Blue Channel Data 6
M4	E0_LVTX_CLKN	O	Negative output of LVDS TX E0 Clock Channel
			Even Blue Channel Data 7
M5	E0_LVTX_CH2P	O	Positive output of LVDS TX E0 Channel 2
			Even Green Channel Data 0
L5	E0_LVTX_CH2N	O	Negative output of LVDS TX E0 Channel 2
			Even Green Channel Data 1
N6	E0_LVTX_CH1P	O	Positive output of LVDS TX E0 Channel 1
			Even Green Channel Data 2

Table 5. Digital video outputs - LVDS & TTL (suggested mapping)

Pin	Assignment	I/O	Description
M6	E0_LVTX_CH1N	O	Negative output of LVDS TX E0 Channel 1
			Even Green Channel Data 3
P7	E0_LVTX_CH0P	O	Positive output of LVDS TX E0 Channel 0
			Even Green Channel Data 4
N7	E0_LVTX_CH0N	O	Negative output of LVDS TX E0 Channel 0
			Even Green Channel Data 5
J4	E1_LVTX_CH6P	O	Positive output of LVDS TX E1 Channel 6
			Odd Green Channel Data 8
K5	E1_LVTX_CH6N	O	Negative output of LVDS TX E1 Channel 6
			Odd Green Channel Data 9
J5	E1_LVTX_CH5P	O	Positive output of LVDS TX E1 Channel 5
			Odd Red Channel Data 8
H4	E1_LVTX_CH5N	O	Negative output of LVDS TX E1 Channel 5
			Odd Red Channel Data 9
G1	E1_LVTX_CH4P	O	Positive output of LVDS TX E1 Channel 4
			Odd Blue Channel Data 0
G2	E1_LVTX_CH4N	O	Negative output of LVDS TX E1 Channel 4
			Odd Blue Channel Data 1
H1	E1_LVTX_CH3P	O	Positive output of LVDS TX E1 Channel 3
			Odd Blue Channel Data 4
H2	E1_LVTX_CH3N	O	Negative output of LVDS TX E1 Channel 3
			Odd Blue Channel Data 5
J2	E1_LVTX_CLKP	O	Positive output of LVDS TX E1 Clock Channel
			Odd Blue Channel Data 6
J3	E1_LVTX_CLKN	O	Negative output of LVDS TX E1 Clock Channel
			Odd Blue Channel Data 7
K3	E1_LVTX_CH2P	O	Positive output of LVDS TX E1 Channel 2
			Odd Green Channel Data 0
K4	E1_LVTX_CH2N	O	Negative output of LVDS TX E1 Channel 2
			Odd Green Channel Data 1
L2	E1_LVTX_CH1P	O	Positive output of LVDS TX E1 Channel 1
			Odd Green Channel Data 2
L3	E1_LVTX_CH1N	O	Negative output of LVDS TX E1 Channel 1
			Odd Green Channel Data 3

Table 5. Digital video outputs - LVDS & TTL (suggested mapping)

Pin	Assignment	I/O	Description
M1	E1_LVTX_CH0P	O	Positive output of LVDS TX E1 Channel 0
			Odd Green Channel Data 4
M2	E1_LVTX_CH0N	O	Negative output of LVDS TX O1 Channel 3
			Odd Green Channel Data 5
L11	O0_LVTX_CH6P	O	Positive output of LVDS TX O0 Channel 6
			Data Enable Output. Default status HIGH.
M12	O0_LVTX_CH6N	O	Negative output of LVDS TX O0 Channel 6
			Data Clock Output. Default status HIGH.
M8	O0_LVTX_CH5P	O	Positive output of LVDS TX O0 Channel 5
			Even Blue Channel Data 8
L9	O0_LVTX_CH5N	O	Negative output of LVDS TX O0 Channel 5
			Even Blue Channel Data 9
P8	O0_LVTX_CH4P	O	Positive output of LVDS TX O0 Channel 4
			Even Blue Channel Data 2
N8	O0_LVTX_CH4N	O	Negative output of LVDS TX O0 Channel 4
			Even Blue Channel Data 3
N9	O0_LVTX_CH3P	O	Positive output of LVDS TX O0 Channel 3
			Even Green Channel Data 6
M9	O0_LVTX_CH3N	O	Negative output of LVDS TX O0 Channel 3
			Even Green Channel Data 7
M10	O0_LVTX_CLKP	O	Positive output of LVDS TX O0 Clock Channel
			Even Red Channel Data 0
L10	O0_LVTX_CLKN	O	Negative output of LVDS TX O0 Clock Channel
			Even Red Channel Data 1
N11	O0_LVTX_CH2P	O	Positive output of LVDS TX O0 Channel 2
			Even Red Channel Data 2
M11	O0_LVTX_CH2N	O	Negative output of LVDS TX O0 Channel 2
			Even Red Channel Data 3
P12	O0_LVTX_CH1P	O	Positive output of LVDS TX O0 Channel 1
			Even Red Channel Data 4
N12	O0_LVTX_CH1N	O	Negative output of LVDS TX O0 Channel 1
			Even Red Channel Data 5
P13	O0_LVTX_CH0P	O	Positive output of LVDS TX O0 Channel 0
			Even Red Channel Data 6

Table 5. Digital video outputs - LVDS & TTL (suggested mapping)

Pin	Assignment	I/O	Description
N13	O0_LVTX_CH0N	O	Negative output of LVDS TX O0 Channel 0
			Even Red Channel Data 7
K10	O1_LVTX_CH6P	O	Positive output of LVDS TX O1 Channel 1
			Vertical Sync Output. Default status HIGH.
J11	O1_LVTX_CH6N	O	Negative output of LVDS TX O1 Channel 6
			Horizontal Sync Output. Default status HIGH.
J10	O1_LVTX_CH5P	O	Positive output of LVDS TX O1 Channel 5
			Odd Blue Channel Data 8
H11	O1_LVTX_CH5N	O	Negative output of LVDS TX O1 Channel 5
			Odd Blue Channel Data 9
M13	O1_LVTX_CH4P	O	Positive output of LVDS TX O1 Channel 4
			Odd Blue Channel Data 2
M14	O1_LVTX_CH4N	O	Negative output of LVDS TX O1 Channel 4
			Odd Blue Channel Data 3
L12	O1_LVTX_CH3P	O	Positive output of LVDS TX O1 Channel 3
			Odd Green Channel Data 6
L13	O1_LVTX_CH3N	O	Negative output of LVDS TX O1 Channel 3
			Odd Green Channel Data 7
K12	O1_LVTX_CLKP	O	Positive output of LVDS TX O1 Clock Channel
			Odd Red Channel Data 0
K11	O1_LVTX_CLKN	O	Negative output of LVDS TX O1 Clock Channel
			Odd Red Channel Data 1
J12	O1_LVTX_CH2P	O	Positive output of LVDS TX O1 Channel 2
			Odd Red Channel Data 2
J13	O1_LVTX_CH2N	O	Negative output of LVDS TX O1 Channel 2
			Odd Red Channel Data 3
H13	O1_LVTX_CH1P	O	Positive output of LVDS TX O1 Channel 1
			Odd Red Channel Data 4
H14	O1_LVTX_CH1N	O	Negative output of LVDS TX O1 Channel 1
			Odd Red Channel Data 5
G13	O1_LVTX_CH0P	O	Positive output of LVDS TX O1 Channel 0
			Odd Red Channel Data 6
G14	O1_LVTX_CH0N	O	Negative output of LVDS TX O1 Channel 0
			Odd Red Channel Data 7

Table 6. Multi-function - digital audio output, general purpose input/output, bootstrap pins

Pin	Assignment	I/O	Description
D2	I2S_MCLK/GPIO_4	I/O	I²S Audio Master Clock
			General Purpose Schmitt Trigger Input / Tri-state Output 4 [5V Tolerant]
D3	I2S_WCLK/BOOT[0]/GPIO_6	I/O	I²S Audio Word Select
			Bootstrap 0. Please refer to Bootstrap Configuration Table for description.
			General Purpose Schmitt Trigger Input / Tri-state Output 6 [5V Tolerant]
C2	I2S_BCLK/BOOT[1]/GPIO_7	I/O	I²S Audio Bit Clock
			Bootstrap 1. Please refer to Bootstrap Configuration Table for description.
			General Purpose Schmitt Trigger Input / Tri-state Output 7 [5V Tolerant]
B1	I2S_0/BOOT[2]/GPIO_8	I/O	I²S Audio Data 0 / SPDIF output
			Bootstrap 2. Please refer to Bootstrap Configuration Table for description.
			General Purpose Schmitt Trigger Input / Tri-state Output 8 [5V Tolerant]
G5	I2S_1/BOOT[3]/GPIO_9	I/O	I²S Audio Data 1 / SPDIF output
			Bootstrap 3. Please refer to Bootstrap Configuration Table for description.
			General Purpose Schmitt Trigger Input / Tri-state Output 9 [5V Tolerant]
F4	I2S_2/BOOT[4]/GPIO_10	I/O	I²S Audio Data 2 / SPDIF output
			Bootstrap 4. Please refer to Bootstrap Configuration Table for description.
			General Purpose Schmitt Trigger Input / Tri-state Output 10 [5V Tolerant]
E3	I2S_3/BOOT[5]/GPIO_11	I/O	I²S Audio Data 3 / SPDIF output
			Bootstrap 5. Please refer to Bootstrap Configuration Table for description.
			General Purpose Schmitt Trigger Input / Tri-state Output 11 [5V Tolerant]

Table 7. Multi-function and system interface connections

Pin	Assignment	I/O	Description
E5	RESETn	I/O	Reset (active low) signal. Connect to digital 3.3 V with a 2.7 K ohm pull-up resistor.
F3	TESTMODE0	I	Reserve for testing. Must be connected to system ground (GND)
G3	TESTMODE1	I	

Table 7. Multi-function and system interface connections

Pin	Assignment	I/O	Description
D13	SPI_DI/GPIO_19	I/O	SPI ROM Data Input.
			General Purpose Schmitt Trigger Input / Tri-state Output 19 [5V Tolerant]
E11	SPI_DO/GPIO_20	I/O	SPI ROM Data Output.
			General Purpose Schmitt Trigger Input / Tri-state Output 20 [5V Tolerant]
E12	SPI_CLK/GPIO_18	I/O	SPI ROM Clock
			General Purpose Schmitt Trigger Input / Tri-state Output 18 [5V Tolerant]
F12	SPI_CSn/GPIO_17	I/O	SPI ROM Chip Select.
			General Purpose Schmitt Trigger Input / Tri-state Output 17 [5V Tolerant]
E6	GPIO_0	I/O	General Purpose Schmitt Trigger Input / Tri-state Output 0 [5V Tolerant]
C3	GPIO_1	I/O	General Purpose Schmitt Trigger Input / Tri-state Output 1 [5V Tolerant]
G10	I2C_MST_SCL/GPIO_2	I/O	Master I²C Serial Clock (for accessing external I²C devices). Pull up with 4.7K ohm resistor.
			General Purpose Schmitt Trigger Input / Tri-state Output 2 [5V Tolerant]
F11	I2C_MST_SDA/GPIO_3	I/O	Master I²C Serial Data (for accessing external I²C devices). Pull up with 4.7K ohm resistor.
			General Purpose Schmitt Trigger Input / Tri-state Output 3 [5V Tolerant]
C1	CLK_OUT/GPIO_5	I/O	Clock Output
			General Purpose Schmitt Trigger Input / Tri-state Output 5 [5V Tolerant]
G4	IR_IN/GPIO_12	I/O	Infra-red Receiver Data Input
			General Purpose Schmitt Trigger Input / Tri-state Output 12 [5V Tolerant]
A1	UART_TX/BOOT[6]/GPIO_13	I/O	UART Transmit Data Output.
			Bootstrap 6. Please refer to Bootstrap Configuration Table for description.
			General Purpose Schmitt Trigger Input / Tri-state Output 13 [5V Tolerant]
E4	UART_RX/GPIO_14	I/O	UART Receive Data Input. Pull up with 4.7K ohm resistor.
			General Purpose Schmitt Trigger Input / Tri-state Output 14 [5V Tolerant]

Table 7. Multi-function and system interface connections

Pin	Assignment	I/O	Description
C13	AUX_I2C_SCL/GPIO_15	I/O	I²C Serial Clock for DP AUX channel. This pin, along with AUX_I2C_SDA, creates external serial interface for DP AUX channel. Connect to digital 3.3V with 4.7K ohm resistor.
			General Purpose Schmitt Trigger Input / Tri-state Output 15 [5V Tolerant]
B14	AUX_I2C_SDA/GPIO_16	I/O	I²C Data Clock for DP AUX channel. This pin, along with AUX_I2C_SCL, creates external serial interface for DP AUX channel. Connect to digital 3.3V with 4.7K ohm resistor.
			General Purpose Schmitt Trigger Input / Tri-state Output 16 [5V Tolerant]
B13	I2C_SCL/GPIO_21	I/O	I²C_SCL. Pull up to 3.3V with 4.7K ohm resistor.
			General Purpose Schmitt Trigger Input / Tri-state Output 21 [5V Tolerant]
D11	I2C_SDA/GPIO_22	I/O	I²C_SDA. Pull up to 3.3V with 4.7K ohm resistor.
			General Purpose Schmitt Trigger Input / Tri-state Output 22 [5V Tolerant]
B12	AUX_UART_TX/BOOT[7]/ GPIO_23	I/O	UART Transmit Data Output for DP AUX channel.
			Bootstrap 7. Please refer to Bootstrap Configuration Table for description.
			General Purpose Schmitt Trigger Input / Tri-state Output 23 [5V Tolerant]
A12	AUX_UART_RX/GPIO_24	I/O	UART Receive Data Input for DP AUX channel. Pull up with 4.7K ohm resistor.
			General Purpose Schmitt Trigger Input / Tri-state Output 24 [5V Tolerant]
D12	IRQ/GPIO_25	I/O	IRQ. Interrupt Output.
			General Purpose Schmitt Trigger Input / Tri-state Output 25 [5V Tolerant]

Table 8. No connects

Pin	Assignment	I/O	Description
G11	NC1	-	No connection.
G12	NC2	-	
C11	NC3	-	
A13	NC4	-	
B4	NC5	-	

Table 9. System power and ground

Pin	Assignment	I/O	Description
C12, E7, E8, K6, K9	PVDD1	P	Digital 1.2V VDD. Connect to digital 1.2V with 0.1µF bypass capacitor.
F10	PVDD21	P	Digital 3.3V VDD. Connect to digital 3.3V with 0.1µF bypass capacitor. Must be connected at same voltage level.
F5	PVDD22		
A14, C4, C14, F6, F7, F8, F9, G6, G7, G8, G9, H6, H7, H8, H9, J6, J7, J8, J9	PVSS3	G	Digital Ground. Each pin must be connected directly to digital ground plane.
B11, C7, C8, D9	DPRX_VDDA_1V2	P	DisplayPort Receiver Analog 1.2V Power Supply. Must be bypassed with a 0.1µF capacitor to analog ground plane on board.
D7, D8, E9, E10	DPRX_VSSA	G	DisplayPort Receiver VSS. Must be directly connected to analog ground plane on board.
B2	VSS_RPLL	G	Analog Ground for the DDS Reference PLL and Digital Core. Must be directly connected to analog ground plane on board.
B3	VDD_RPLL	P	Analog 1.2V Power Supply for RCLK PLL and Digital Core. Must be bypassed with a 0.1µF capacitor to analog ground plane on board.
D6	VDDA_3V3	P	Analog 3.3V VDD. Connect to analog 3.3V with 0.1µF bypass capacitor to analog ground plane on board.
H3, H12, L8, N1, N14	AVDD_OUT_LVTX_33	P	Analog 3.3V VDD. Connect to analog 3.3V with 0.1µF bypass capacitor to analog ground plane on board.
L7	AVDD_LVTX_33	P	Analog 3.3V VDD. Connect to analog 3.3V with 0.1µF bypass capacitor to analog ground plane on board.
F2, F13, H5, H10, K8, P1, P14	AVSS_OUT_LVTX	G	Analog ground. Must connect directly to analog ground plane on board.
K7	AVSS_LVTX	G	Analog ground. Must connect directly to analog ground plane on board.

5.2 Bootstrap configuration

During hardware reset, on the rising edge of RESETn, logic high or low configuration on bootstrap pins are latched and stored. 4.7K pull-up or pull-down resistors must be installed to indicate logic '1' or '0'

status on the bootstrap pins. Bootstrap operation is only guaranteed with external pull-up or pull-down resistors. There are 8 bootstrap pins available on STDP4020. Some bootstraps may not be available for normal use.

Table 10. Bootstrap configuration

Pin #	Assignment	Function
D3	BOOT[0]	Set to 0 (Pull Low to GND)
C2	BOOT[1]	Set to 0 (Pull Low to GND)
B1	BOOT[2]	IC_OSC_SEL Selects clock source between external clock source and internal ring oscillator 0 = TCLK is from external source (XTAL or ext oscillator) 1 = TCLK is from internal ring oscillator (Strap to VDD)
G5	BOOT[3]	TTL_LVDS_OUT TTL/LVDS output mode selection 0 = Output is in LVDS format 1 = Output is in TTL format
F4	BOOT[4]	OCM_BOOT_SEL Selects OCM boot option 0 = OCM boot will be from internal ROM code 1 = OCM boot is from external ROM/Flash code
E3	BOOT[5]	WIDE_NARROW_BUS Selects wide or narrow LVDS or TTL bus LVDS 0 = DUAL LVDS 1 = QUAD LVDS TTL 0 = Single 1 = Dual
A1	BOOT[6]	Set to 0 (Pull Low to GND) for normal operation
B12	BOOT[7]	I2C_DEV_ID[0] Selects I2C slave Device ID for RD/WR access 001 = 0xE4, 0xE5; 000 = 0xE6, 0xE7

Table 11. Software implemented bootstrap configuration

Pin #	Assignment	Function
C1	CLK_OUT/GPIO_5	ASSR_ENABLE Selects whether ASSR is enabled 0 = Disabled 1 = Enabled

5.3 General purpose input/output (GPIO) pins

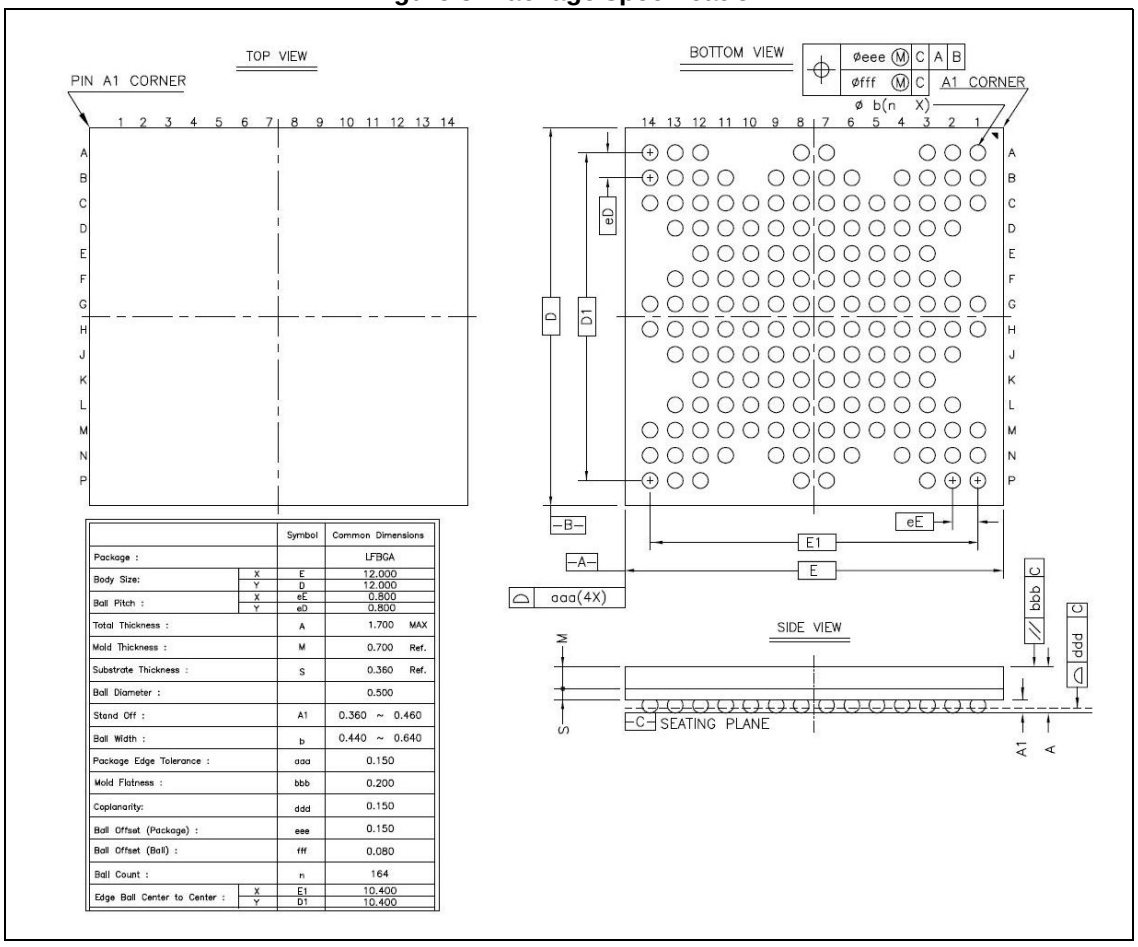
The STDP4020 contains 27 general-purpose input/output (GPIO) pins for system configuration purpose. GPIO_0, GPIO_1 are dedicated general-purpose IO pins and the rest have shared functionality. Each GPIO has independent direction control and open drain enable for reading and writing.

Note: The GPIO functionality is available only for custom applications. Default settings allow configuration of dedicated GPIO pins (GPIO_0 and GPIO_1) through host interface and the rest of the GPIO configuration requires over-riding the default feature using external firmware.

6. Package

Package type: 164 LFBGA (12 x 12 mm / ball pitch 0.8 mm)

Figure 3. Package specification

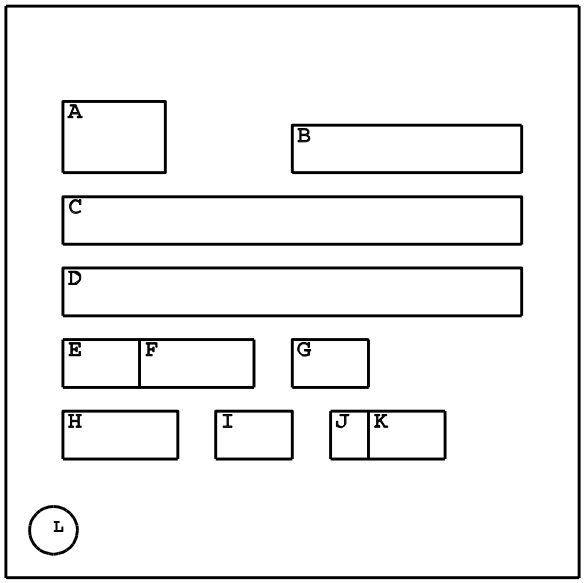


		Symbol	Common Dimensions
Package :			LFBGA
Body Size:	X	E	12.000
	Y	D	12.000
Ball Pitch :	X	eE	0.800
	Y	eD	0.800
Total Thickness :		A	1.700 MAX
Mold Thickness :		M	0.700 Ref.
Substrate Thickness :		S	0.360 Ref.
Ball Diameter :			0.500
Stand Off :		A1	0.360 ~ 0.460
Ball Width :		b	0.440 ~ 0.640
Package Edge Tolerance :		aaa	0.150
Mold Flatness :		bbb	0.200
Coplanarity:		ddd	0.150
Ball Offset (Package) :		eee	0.150
Ball Offset (Ball) :		fff	0.080
Ball Count :		n	164
Edge Ball Center to Center :	X	E1	10.400
	Y	D1	10.400

6.1 Marking field template and descriptors

The STDP4020 marking template is shown below.

Figure 4. Marking template



Field descriptors are shown below.

Table 12.Field descriptors

Field	Description	Marking
A	Standard MegaChips logo	M
B	2-character version code	AD
C	Product code	STDP4020 or STDP4010
D	8-character diffusion code	9R”ABCDEF”
E	2-character assembly plant code	AA
F	3-character BE sequence code	“XYZ”
G	2-character diffusion plant code	9R
H	3-character country of origin code	TWN
I	2-character test plant code	AA
J	1-digit assembly year	“Y”
K	2-digit assembly week	“WW”
L	Ball A1 identifier	a DOT

7. Electrical specification

7.1 Absolute maximum ratings

Applied conditions greater than those listed under “Absolute maximum ratings” may cause permanent damage to the device. The device should never exceed absolute maximum conditions since it may affect device reliability.

Table 13. Absolute maximum ratings

Parameter	Symbol	Min	Typ	Max	Units
3.3 V supply voltages (1,2)	$V_{VDD\_3.3}$	-0.3	3.3	3.6	V
1.2 V supply voltages (1.2)	$V_{VDD\_1.2}$	-0.3	1.2	1.26	V
Input voltage (5V tolerant inputs) (1,2)	$V_{IN5Vtol}$	-0.3		5.5	V
Input voltage (non 5V tolerant inputs) (1,2)	V_{IN}	-0.3		3.6	V
ESD - Human Body Model (HBM)(4)	V_{ESD}			±2.0	kV
ESD - Machine Model (MM)(4)	V_{ESD}			±200	V
ESD - Charged Device Model (CDM)(4)	V_{ESD}			±500	V
Latch-up	I_{LA}			±100	mA
Ambient operating temperature	T_A	0		70	°C
Storage temperature	T_{STG}	-40		150	°C
Operating junction temperature	T_J	0		125	°C
Thermal resistance (Junction to Ambient)(3)	θ_{JA}			36.6	°C/W
Thermal resistance (Junction to Case)(3)	θ_{JC}			18.1	°C/W
Peak IR reflow soldering temperature (<10 sec.)	T_{SOL}			260	°C

Note (1): All voltages are measured with respect to GND.

Note (2): Absolute maximum voltage ranges are for transient voltage excursions.

Note (3): These are simulated results under the following conditions - Four layer JEDEC PCB, no heat spreader, Air flow = 0 m/s

Note (4): The ESD result shown is not applicable for reserved pins.

7.2 Maximum speed of operation

LVTTL output clocks

Video output: Single bus clocking

165 MHz max

Video output: Dual bus clocking

165 MHz max

LVDS output clocks

Single LVDS channel

150 MHz max

Dual LVDS channel

150 MHz max

Quad LVDS channel

100 MHz max

Audio output

SPDIF 192 kHz 32 bits

I2S WS output = 192 kHz

I2S SCLK output = 12.288 MHz

System clocks

Crystal Clock = 27 MHz

SPI_CLK = 50 MHz

I2C CLK = 400 kHz

Internal OCM Clock = 100 MHz max

DisplayPort receiver bit rate

Main link

Min: 1.62 Gbps/lane

Max: 3.2 Gbps/lane

Auxiliary channel: 1 Mbps

7.3 DC characteristics

Table 14. DC characteristics

Parameter	Symbol	Min	Typ	Max	Units
3.3 V supply voltages (analog and digital)	$V_{VDD\_3.3}$	3.0	3.3	3.6	V
1.2 V supply voltages (analog and digital)	$V_{VDD\_1.2}$	1.14	1.2	1.26	V
Power					
TTL output					
Power consumption: 2560 x 1600 / 60 Hz test pattern: ON-OFF dot Moire	4L		610		mW
Power consumption: 1920 x 1200 / 60 Hz test pattern: ON-OFF dot Moire	2L		520		mW
Power consumption: 1440 x 900 / 60 Hz test pattern: ON-OFF dot Moire	1L		360		mW
Sleep **Power down**			24		mW
Supply current					
Measurement conditions: 2560 x 1600 / 60 Hz test pattern: ON-OFF dot Moire VDD (analog and digital power) = 3.3V DDA (analog and digital power) =1.2V In all configuration, 8 bits output is used.			115 190		mA
Power					
LVDS output					
Power consumption: 1920 x 1080 / 120 Hz test pattern: ON-OFF dot Moire	4L		615		mW
Power consumption: 1920 x 1200 / 60 Hz test pattern: ON-OFF dot Moire	2L		371		mW
Power consumption: 1440 x 900 / 60 Hz test pattern: ON-OFF dot Moire	1L		263		mW
Sleep **Power down**			24		mW
Supply Current					
Measurement conditions: 1920 x 1080 / 120 Hz test pattern: ON-OFF dot Moire VDD (analog and digital power) = 3.3V DDA (analog and digital power) =1.2V In all configuration, 8 bits output is used.			110 210		mA
Inputs					
High voltage	V_{IH}	2.0		VDD	V
Low voltage	V_{IL}	GND		0.8	V

Table 14. DC characteristics

Parameter	Symbol	Min	Typ	Max	Units
High current (V_{IN} = 5.0 V)	I_{IH}	-25		25	µA
Low current (V_{IN} = 0.8 V)	I_{IL}	-25		25	µA
Capacitance (V_{IN} = 2.4 V)	C_{IN}			8	pF
Outputs					
High voltage (I_{OH} = 7 mA)	V_{OH}	2.4		VDD	V
Low voltage (I_{OL} = -7 mA)	V_{OL}	GND		0.4	V
Tri-state leakage current	I_{OZ}	-25		25	µA

7.4 AC characteristics

7.4.1 DisplayPort receiver

Table 15. DisplayPort receiver characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comments
UI_High_Rate	Unit interval for high bit rate (2.7 Gbps/lane)		370		ps	DisplayPort link RX does not require local crystal for link clock generation.
UI_Low_Rate	Unit interval for reduced bit rate (1.62 Gbps/lane)		617		ps	
UI_Rate_3.24	Unit interval for high bit rate (3.24 Gbps/lane)		3.24		Gbps	DisplayPort link RX does not require local crystal for link clock generation.
Down Spread Amplitude	Link clock down spreading	0.5			%	Modulation frequency range of 30 kHz to 33 kHz
$V_{RX-DIFFp-p}$	Differential peak-to-peak input voltage at package pins	120			mV	
Rx horizontal eye specification for high bit rate						
T_{RX-EYE_CHIP}	Minimum receiver eye width at Rx package pins	0.47			UI	
$T_{RX-EYE-MEDIAN-to-MAX-JITTER\_CHIP}$	Maximum time between the jitter median and maximum deviation from the median at Rx package pins			0.265	UI	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specifies the total allowable DJ
Rx horizontal eye specification for reduced bit rate						
T_{RX-EYE_CHIP}	Minimum receiver eye width at Rx package pins	0.42			UI	(1- T_{RX-EYE_CONN}) specifies the allowable TJ

Table 15. DisplayPort receiver characteristics

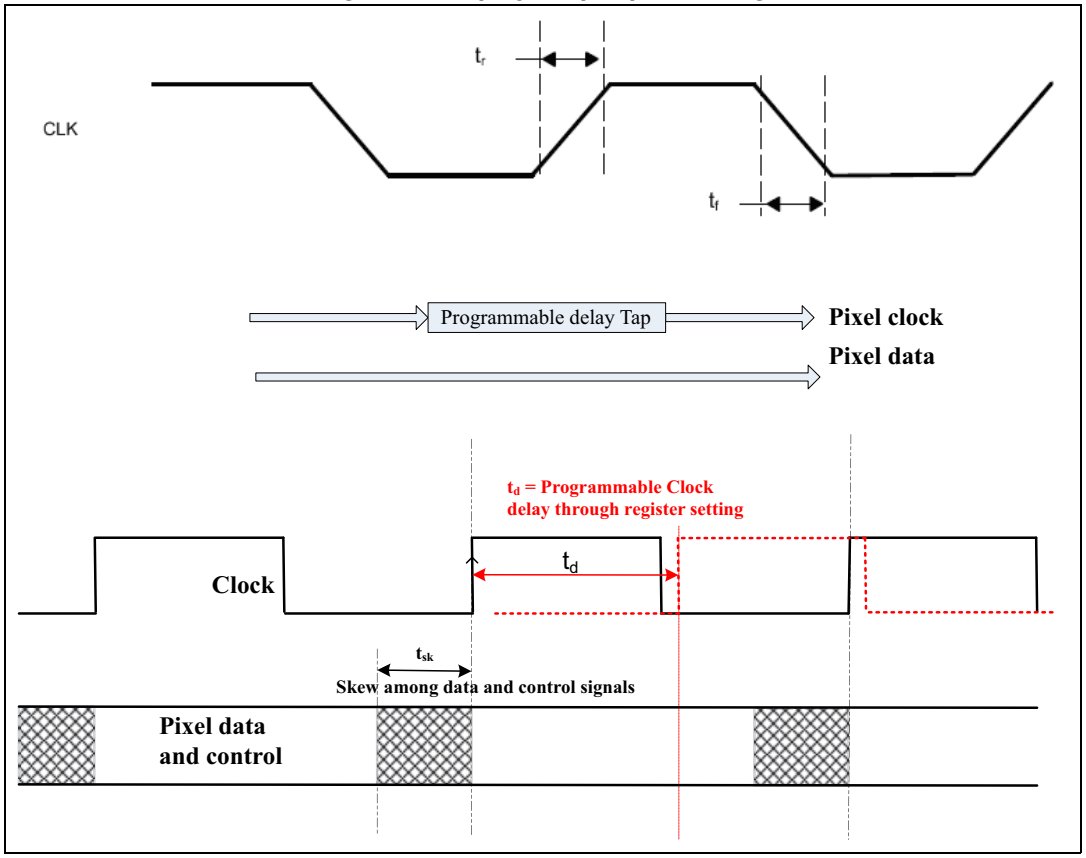
Symbol	Parameter	Min	Typ	Max	Unit	Comments
$T_{RX-EYE-MEDIAN-to-MAX-JITTER\_CHIP}$	Maximum time between the jitter median and maximum deviation from the median at Rx package pins			0.29	UI	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specifies the total allowable DJ
$V_{RX-DC-CM}$	RX DC common mode voltage	0		3.60	V	Common mode voltage is equal to Vbias_Rx voltage. VDD is the receiver input power supply voltage and 3.6 V maximum.
$I_{RX-SHORT}$	RX short circuit current limit			90	mA	Total drive current of the transmitter when it is shorted to its ground.
$RL_{RX-DIFF}$	Differential return loss at 0.675 GHz			12	dB	Straight loss line between 0.675 GHz and 1.35 GHz
	Differential loss at 1.35 GHz			9	dB	
$R_{RX-HIGH-IMP-DC}$	Powered down DC input resistance	200 k			Ω	
$L_{RX-SKEW-INTER\_CHIP}$	Lane-to-lane skew at RX package pins			5200	ps	Maximum skew limit between different RX lanes of a DisplayPort link.
Intra-pair skew specification for high bit rate						
$L_{RX-SKEW-INTRA\_CHIP\_High-Bit-Rate}$	Lane intra-pair skew at RX package pins			100	ps	Maximum skew limit between D+ and D- of the same lane.
Intra-pair skew specification for reduced bit rate						
$L_{RX-SKEW-INTRA\_CHIP\_Reduced-Bit-Rate}$	Lane intra-pair skew at RX package pins			300	ps	Maximum skew limit between D+ and D- of the same lane.
$F_{RX-TRACKING-BW}$	Jitter tracking bandwidth	30			MHz	Minimum CDR tracking bandwidth at the receiver. BW as measured with a D10.2 clock pattern

7.4.2 Digital video output port

Table 16. Digital video output port timing

Symbol	Parameter	Conditions (@ 15 pF load)	Min	Typ	Max	Unit
t_{cyc}	Display output clock cycle time	8 MHz to 165 MHz	6	-	125	ns
f_{clk}	Display output clock frequency		-	-	165	MHz
	Duty cycle for f_{clk}		40	50	60	%
t_r	Clock rise time	10% to 90%	-	1	-	ns
t_f	Clock fall time	10% to 90%	-	1	-	ns
t_d	Clock delay from pixel data and control *Note*: Clock delay is programmable using TTL_CLK_TIMING register. Each delay tap setting increases delay by approximately 1 ns.		0	-	3	ns
t_{sk}	Skew between different data and control signals	For 165 MHz clock, one ON - One OFF pattern	0	600	650	ps

Figure 5. Display output port timing



7.4.3 LVDS transmitter

Figure 6. LVDS transmitter switching characteristics

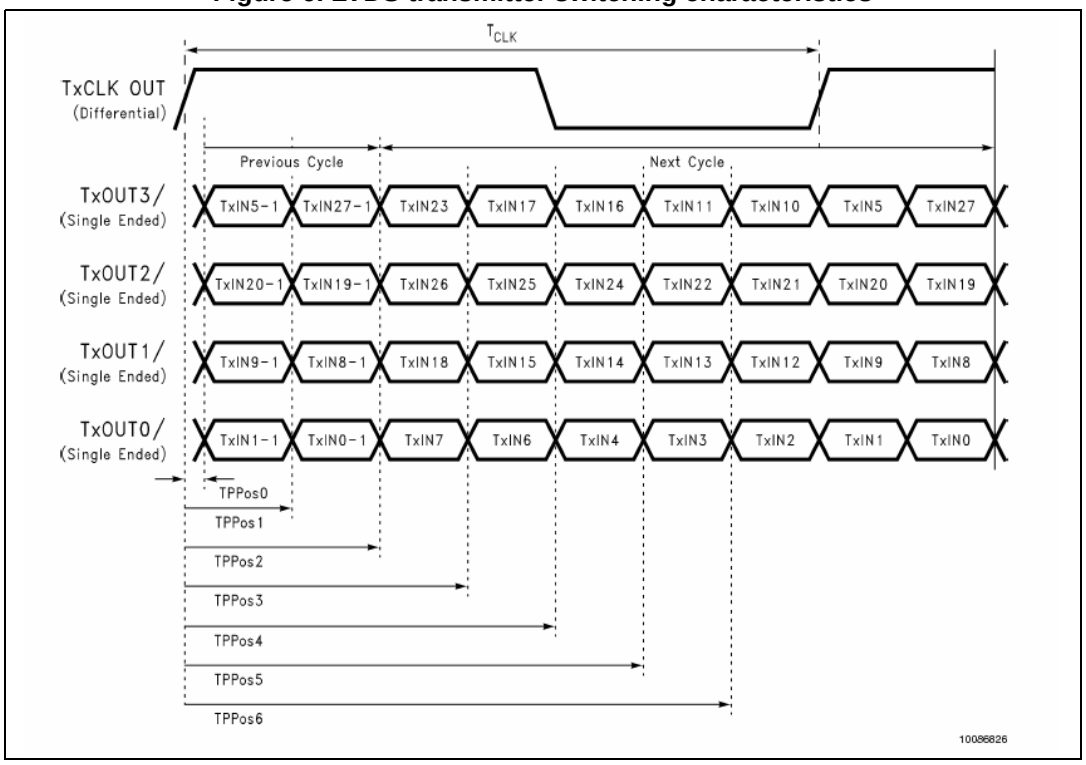


Table 17. LVDS TX1 even channels

Symbol	Parameters	E_CH0 ~ E_CH3	Typical	Units
TPPos0	T/X output pulse position for bit 0	F= 150 MHz	0	ns
TPPos1	T/X output pulse position for bit 1		0.95	ns
TPPos2	T/X output pulse position for bit 2		1.9	ns
TPPos3	T/X output pulse position for bit 3		2.85	ns
TPPos4	T/X output pulse position for bit 4		3.8	ns
TPPos5	T/X output pulse position for bit 5		4.76	ns
TPPos6	T/X output pulse position for bit 6		5.71	ns

Table 18. LVDS TX1 odd channels

Symbol	Parameters	O_CH0 ~ O_CH3	Typical	Units
TPPos0	T/X output pulse position for bit 0	F= 150 MHz	0	ns
TPPos1	T/X output pulse position for bit 1		0.95	ns
TPPos2	T/X output pulse position for bit 2		1.9	ns
TPPos3	T/X output pulse position for bit 3		2.85	ns
TPPos4	T/X output pulse position for bit 4		3.8	ns

Table 18. LVDS TX1 odd channels

Symbol	Parameters	O_CH0 ~ O_CH3	Typical	Units
TPPos5	T/X output pulse position for bit 5		4.76	ns
TPPos6	T/X output pulse position for bit 6		5.71	ns

Table 19. LVDS TX2 even channels

Symbol	Parameters	E_CH0 ~ E_CH3	Typical	Units
TPPos0	T/X output pulse position for bit 0	F= 150 MHz	0	ns
TPPos1	T/X output pulse position for bit 1		0.95	ns
TPPos2	T/X output pulse position for bit 2		1.9	ns
TPPos3	T/X output pulse position for bit 3		2.85	ns
TPPos4	T/X output pulse position for bit 4		3.8	ns
TPPos5	T/X output pulse position for bit 5		4.76	ns
TPPos6	T/X output pulse position for bit 6		5.71	ns

Table 20. LVDS TX2 odd channels

Symbol	Parameters	O_CH0 ~ O_CH3	Typical	Units
TPPos0	T/X output pulse position for bit 0	F= 150 MHz	0	ns
TPPos1	T/X output pulse position for bit 1		0.95	ns
TPPos2	T/X output pulse position for bit 2		1.9	ns
TPPos3	T/X output pulse position for bit 3		2.85	ns
TPPos4	T/X output pulse position for bit 4		3.8	ns
TPPos5	T/X output pulse position for bit 5		4.76	ns
TPPos6	T/X output pulse position for bit 6		5.71	ns

Note: There is +/- 200 ps variation for the measurements for even and odd channels

7.4.4 I2C interface timing

Table 21. I2C interface timing

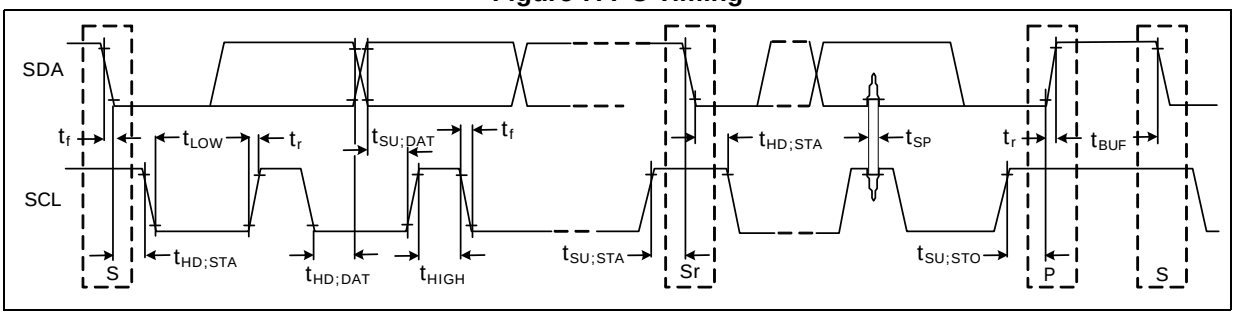
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	SCL clock rate	Fast mode	0	-	400	kHz
$t_{HD\text{-}STA}$	Hold time START	After this period, the 1st clock starts	1.2	-		µs
t_{LOW}	Low period of clock	SCL	1.3	-		µs
t_{HIGH}	High period of clock	SCL	1.2	-		µs

Table 21. I2C interface timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{su;STA}$	Setup time for a repeated START		1.2	-		µs
$t_{HD;DAT}$	Data hold time	For master	0.7	-	0.9(1)	µs
$t_{SU;DAT}$	Data setup time		380			ns
T_{BUF}	Bus free time between STOP and START		1.3			µs
C_b	Capacitance load for each bus line			100	400	pF
t_r	Rise time		220		300	ns
t_f	Fall time		60		300	ns
V_{nh}	Noise margin at high level		0.25VDD			V
V_{nl}	Noise margin at low level		0.2VDD			

Note: *The maximum $t_{HD;DAT}$ only has to be met if the device does not stretch the low period t_{LOW} of the SCL signal. In the diagram below, S = start, P = stop, Sr = Repeated start, and SP= Repeated stop conditions.*

Figure 7. I²C Timing



7.4.5 SPI interface timing

Table 22. SPI interface timing, VDD = 3.3V

Symbol	Parameter	Min	Max	Units
F_{CLK}	Serial clock frequency		50	MHz
T_{SCKH}	Serial clock high time	9		ns
T_{SCKL}	Serial clock low time	9		ns
T_{SCKR}	Serial clock rise time (slew rate)	0.1		V/ns
T_{SCKF}	Serial clock fall time (slew rate)	0.1		V/ns
T_{CES}	CE# active setup time	5		ns
T_{CEH}	CE# active hold time	5		ns
T_{CHS}	CE# not active setup time	5		ns
T_{CHH}	CE# not active hold time	5		ns
T_{CPH}	CE# high time	50		ns
T_{CHZ}	CE# high to high-Z output		8	ns
T_{CLZ}	SCK low to low-Z output	0		ns
T_{DS}	Data in setup time	5		ns
T_{DH}	Data in hold time	5		ns
T_{OH}	Output hold from SCK change	0		ns
T_V	Output valid from SCK		8	ns

Figure 8. SPI output or serial interface SPI ROM input timing

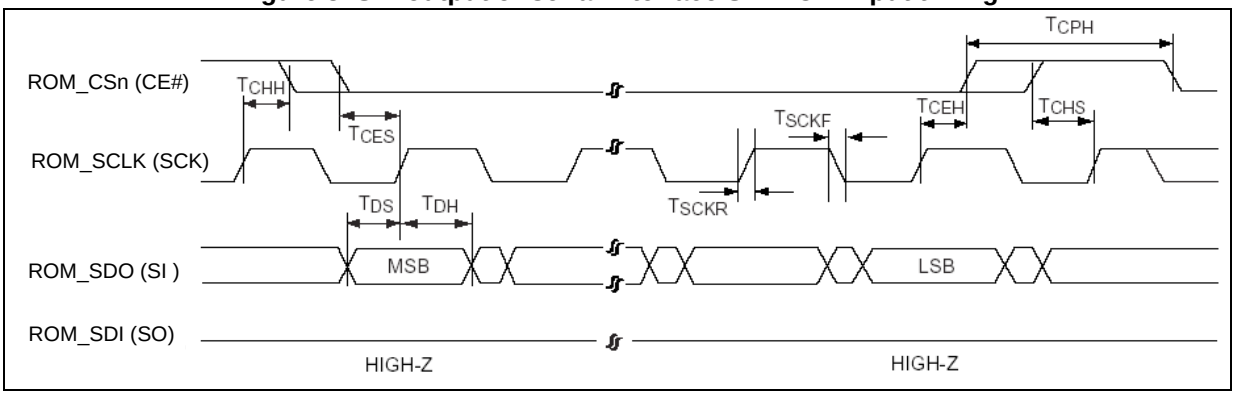
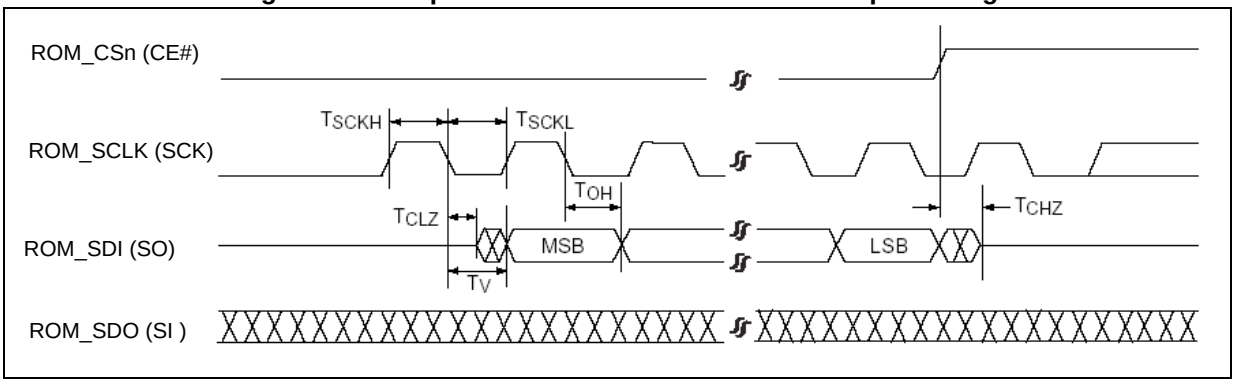


Figure 9. SPI input or serial interface SPI ROM output timing



8. Ordering information

Table 23. Order codes

Part number	Description
STDP4020-AD	164 LFBGA (12 x 12 mm)
STDP4010-AD	164 LFBGA (12 x 12 mm)

9. Revision history

Table 24. Document revision history

Date	Revision	Changes
03-Mar-2016	A	Initial release.

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