

## Adaptive 3.4 Gbps 3:1 TMDS/HDMI signal equalizer

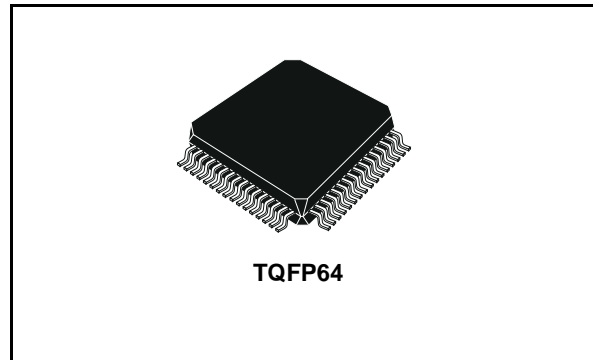
Preliminary Data

### Features

- Digital video signal equalizer with 3:1 HDMI switch
- Compatible with the high-definition multimedia interface (HDMI) v1.3 digital interface
- 340 MHz maximum clock speed operation supports all video formats with deep color at maximum refresh rates
- 3.4 Gbps data rate per channel
- Fully automatic adaptive equalizer for cable lengths up to 25 m
- Selectable 50  $\Omega$  input termination to  $V_{CC}$ : 3.135 to 3.465 V
- Low speed control lines supply to  $V_{DD}$  : 5 V (typ)
- ESD HBM model :  $> \pm 5$  KV for all I/Os
- Integrated open-drain I<sup>2</sup>C buffer for display data channel (DDC)
- 5.3 V tolerant DDC and HPD I/Os
- Lock-up free operation of I<sup>2</sup>C bus
- 0 to 400 kHz clock frequency for I<sup>2</sup>C bus
- Low capacitance TMDS channels
- Equalizer for signal regeneration
- Low output skew and jitter

### Applications

- Advanced TVs supporting the HDMI/DVI standard
- Front projectors, LCD TVs and PDPs
- Monitors and notebooks
- Set-top box and DVD players



### Description

The STDVE103A integrates a 4-channel 3.4 Gbps TMDS equalizer and a 3:1 switch to select one of the three HDMI ports. The high-speed data paths and flow-through pinout minimize the internal device jitter and simplify the board layout. The equalizer overcomes the jitter effects from lossy cables. The buffer/driver on the output can drive the TMDS output signals over long distances.

Also, STDVE103A integrates the 50  $\Omega$  termination resistor on all the input channels to improve performance and reduce board space. The device can be placed in a low-power mode by disabling the output current drivers.

The differential signal from the HDMI/DVI ports can be routed through the STDVE103A to guarantee good signal quality at the HDMI receiver.

Designed for very low skew, jitter and low I/O capacitance, the switch preserves the signal integrity to pass the stringent HDMI compliance requirements.

**Table 1. Device summary**

Order code	Operating temperature	Package	Packaging
STDVE103A	-40°C to 85°C	TQFP64	Tape and reel

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# 1 General description

The STDVE103A is a TMDS/HDMI 3:1 switch with signal equalizer. The device is a HDMI switch featuring an integrated 4-channel 3.4 Gbps TMDS equalizer and 3:1 switch to select one of the three HDMI ports (either external ports or internal sources).

The high-speed data paths and flow-through pinout minimize the internal device jitter and simplify the board layout.

The equalizer provides compensation to overcome the intersymbol interference (ISI) jitter effects from lossy cables.

The output driver buffers the TMDS output signals over long distances.

Also, the STDVE103A integrates the 50  $\Omega$  termination resistor on all the input channels to improve performance and reduce board space.

The device can operate in a low-power mode by disabling the output current drivers.

The STDVE103A is ideal for advanced TV and STB applications supporting the HDMI/DVI standard. The differential signal from the HDMI/DVI ports can be routed through the STDVE103A to guarantee good signal quality at the HDMI receiver. Designed for very low skew, jitter and low I/O capacitance, the switch preserves the signal integrity to pass the stringent HDMI compliance requirements.

The STDVE103A provides the ability to boost the incoming TMDS signal and drive it to a level which allows efficient signal recovery at the HDMI receiver. It is especially useful for boosting signals for longer distance transmission when the HDMI receiver is physically distant from the HDMI input port.

## 2 Block diagram

Figure 1. STDVE103A block diagram

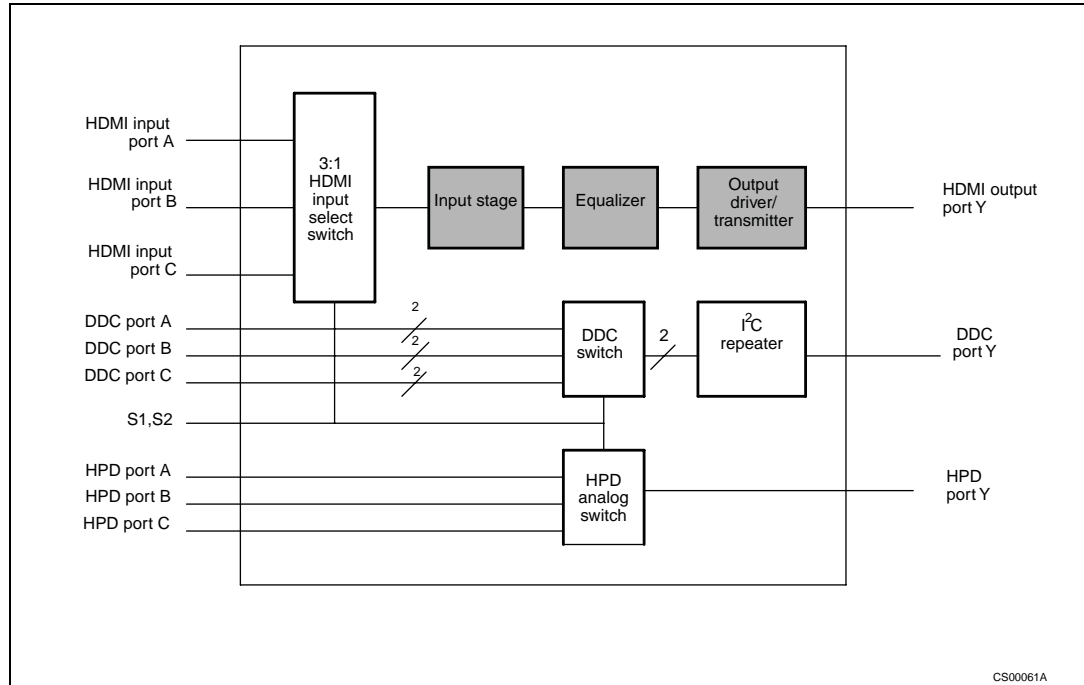


Figure 2. Equalizer functional diagram (one signal pair)

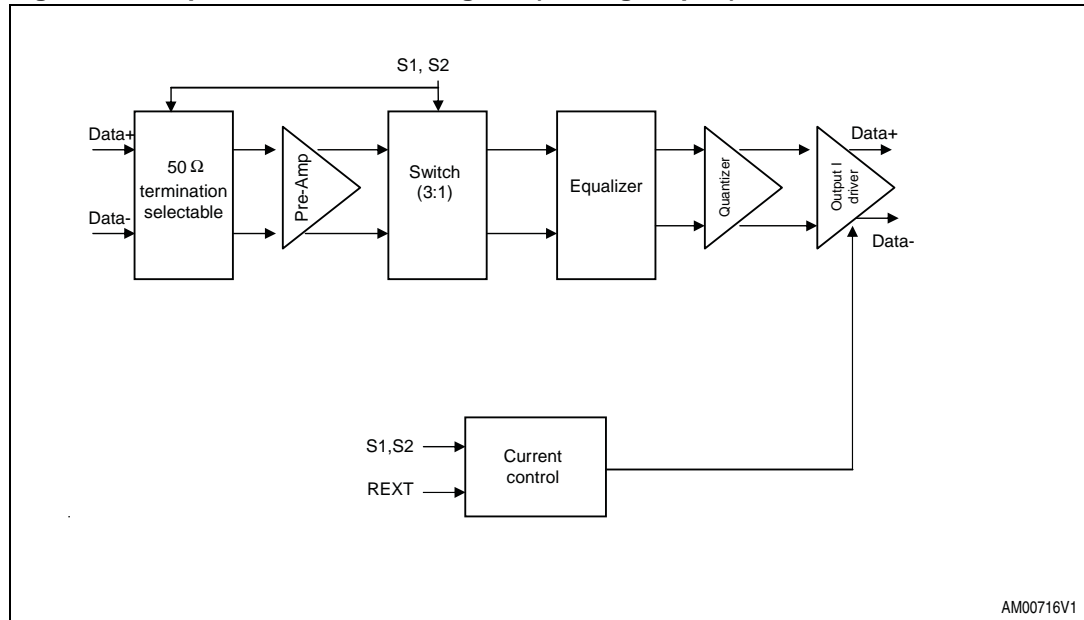
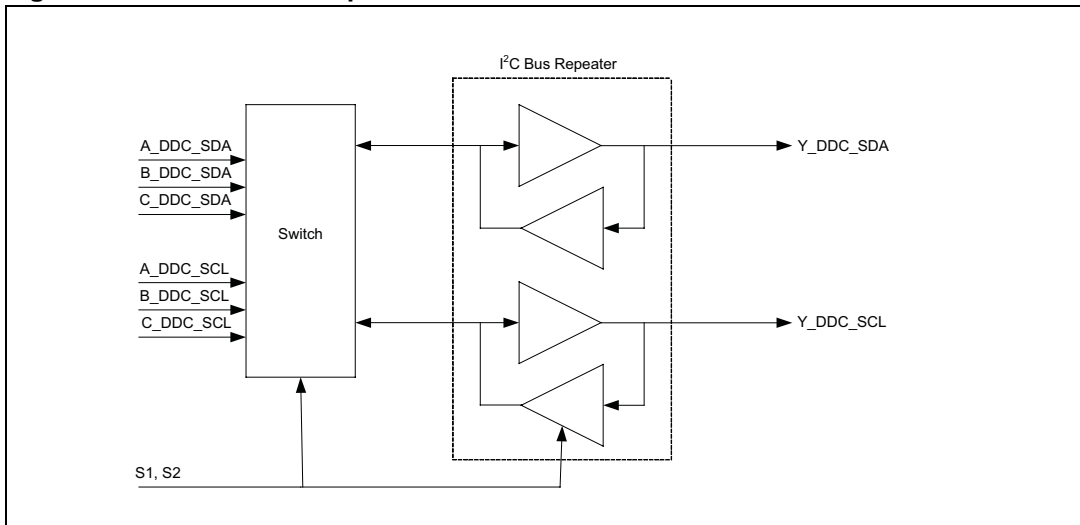
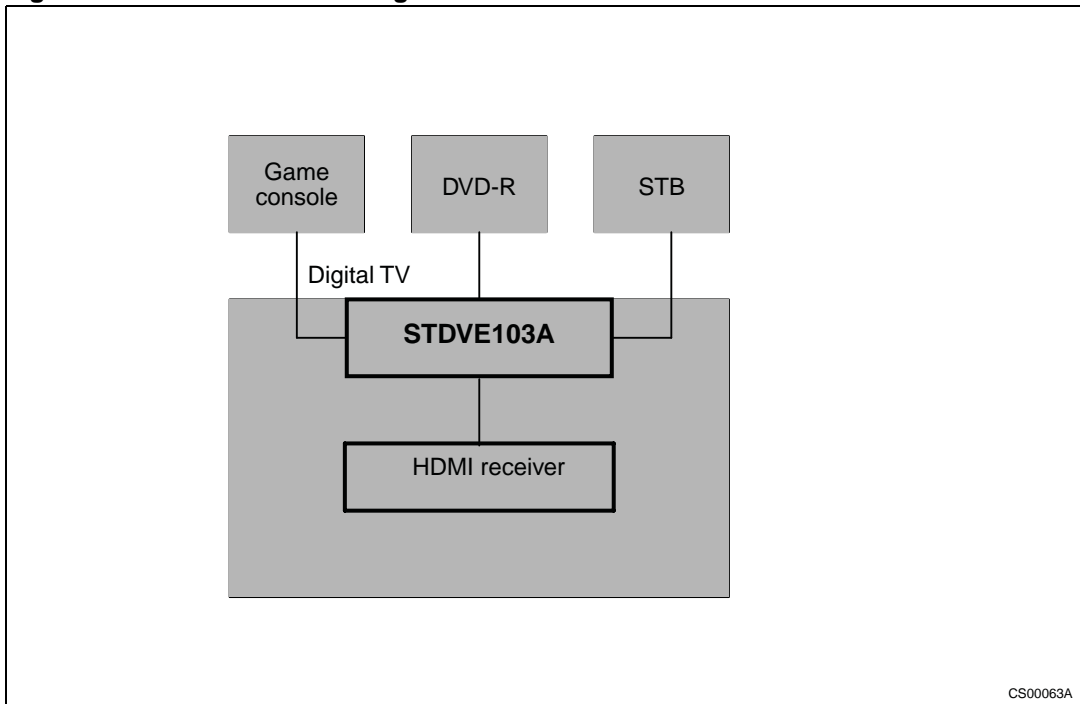


Figure 3. DDC I<sup>2</sup>C bus repeater



## 2.1 Application diagrams

Figure 4. STDVE103A in a digital TV





### 3 Pin configuration

Figure 5. Pin configuration (TQFP64 package)

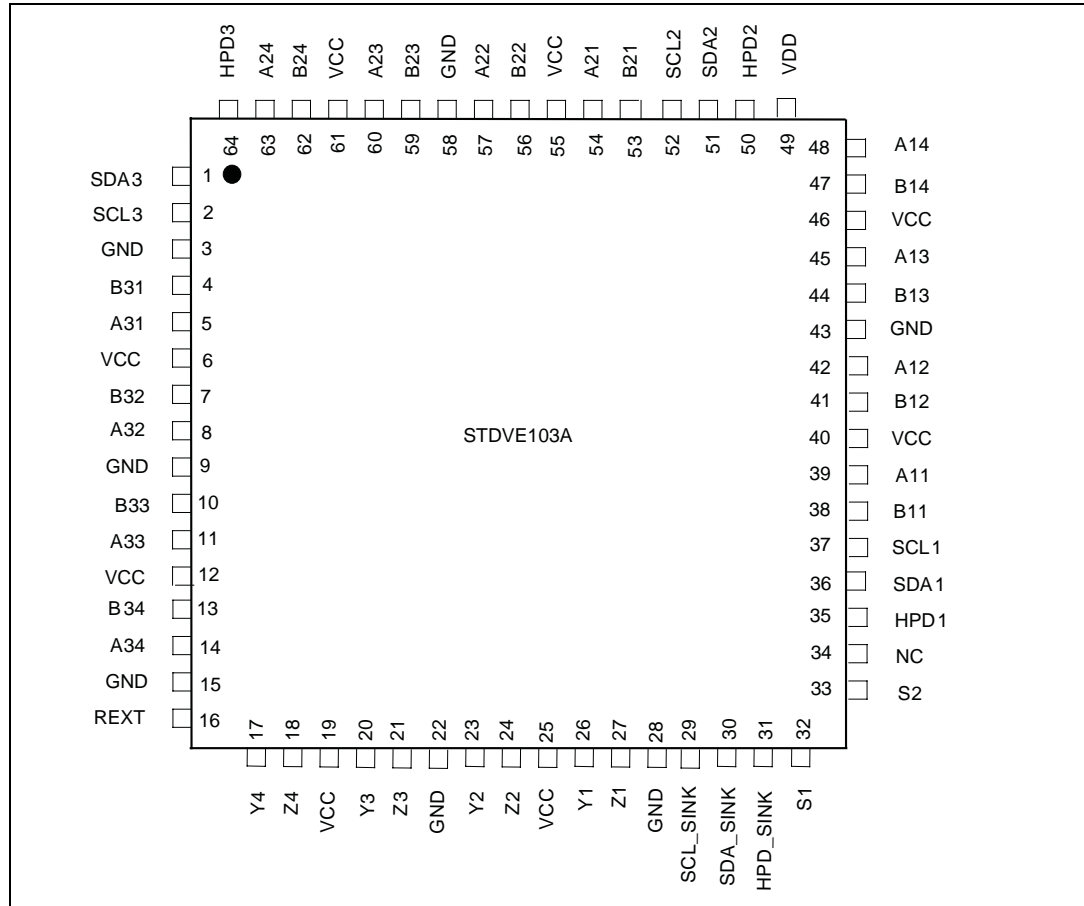


Table 2. Pin description

Pin number	Pin name	Type	Function
1-2	SDA3, SCL3	I/O	Port3 DDC bus data and clock lines
3	GND	Power	Ground
4-5	B31, A31	Input, TMDS	Port 3 differential inputs for channel 1
6	V <sub>CC</sub>	Power	Supply voltage (3.3 V ± 5%)
7-8	B32, A32	Input, TMDS	Port 3 differential inputs for channel 2
9	GND	Power	Ground
10-11	B33, A33	Input, TMDS	Port 3 differential inputs for channel 3
12	V <sub>CC</sub>	Power	Supply voltage (3.3 V ± 5%)
13-14	B34, A34	Input, TMDS	Port 3 differential inputs for channel 4
15	GND	Power	Ground

Table 2. Pin description (continued)

Pin number	Pin name	Type	Function
16	R <sub>EXT</sub>	Analog	Connect to GND through a 4.7 K $\pm$ 1% precision reference resistor. Sets the output current to generate the output voltage compliant with TMDS
17-18	Y4, Z4	Output, TMDS	Channel 4 differential outputs
19	V <sub>CC</sub>	Power	Supply voltage (3.3 V $\pm$ 5%)
20-21	Y3, Z3	Output, TMDS	Channel 3 differential outputs
22	GND	Power	Ground
23-24	Y2, Z2	Output, TMDS	Channel 2 differential outputs
25	V <sub>CC</sub>	Power	Supply voltage (3.3 V $\pm$ 5%)
26-27	Y1, Z1	Output, TMDS	Channel 1 differential outputs
28	GND	Power	Ground
29	SCL_SINK	I/O	Sink side DDC bus clock line
30	SDA_SINK	I/O	Sink side DDC bus data line
31	HPD_SINK	Input	Sink side hot plug detector input High: 5 V power signal asserted from source to sink and EDID is ready Low: No 5 V power signal is asserted from source to sink or EDID is not ready
32-33	S1,S2	Input	Source select inputs
34	NC		No connect
35	HPD1	Output	Port 1 hot plug detector output.
36	SDA1	I/O	Port 1 DDC bus data line
37	SCL1	I/O	Port 1 DDC bus clock line
38-39	B11, A11	Input, TMDS	Port 1 differential inputs for channel 1
40	V <sub>CC</sub>	Power	Supply voltage (3.3 V $\pm$ 5%)
41-42	B12, A12	Input, TMDS	Port 1 differential inputs for channel 2
43	GND	Power	Ground
44-45	B13, A13	Input, TMDS	Port 1 differential inputs for channel 3
46	V <sub>CC</sub>	Power	Supply voltage (3.3 V $\pm$ 5%)
47-48	B14, A14	Input, TMDS	Port 1 differential inputs for channel 4
49	V <sub>DD</sub>	Power	Supply voltage (5.0 V $\pm$ 10%) for DDC, HPD and source selector pins
50	HPD2	Output	Port 2 hot plug detector output
51	SDA2	I/O	Port 2 DDC bus data line

**Table 2. Pin description (continued)**

Pin number	Pin name	Type	Function
52	SCL2	I/O	Port 2 DDC bus clock line
53-54	B21, A21	Input, TMDS	Port 2 differential inputs for channel 1
55	V <sub>CC</sub>	Power	Supply voltage (3.3 V ± 5%)
56-57	B22, A22	Input, TMDS	Port 2 differential inputs for channel 2
58	GND	Power	Ground
59-60	B23, A23	Input, TMDS	Port 2 differential inputs for channel 3
61	V <sub>CC</sub>	Power	Supply voltage (3.3 V ± 5%)
62-63	B24, A24	Input, TMDS	Port 2 differential inputs for channel 4
64	HPD3		Port 3 hot plug detector output.

## 4 Functional description

The STDVE103A routes physical layer signals for high bandwidth digital video and is compatible with low voltage differential signaling standards such as the TMDS. The device passes the differential inputs from a video source to a common display when it is in the active mode of operation. The device conforms to the TMDS standard on both inputs and outputs.

The low on-resistance and low I/O capacitance of the switch in STDVE103A result in a very small propagation delay. The device integrates SPDT-type switches for 3 differential data TMDS channels and 1 differential clock channel. Additionally, it integrates the switches for DDC and HPD line switching with I<sup>2</sup>C repeater on the DDC lines.

The I<sup>2</sup>C interface of the selected input port is linked to the I<sup>2</sup>C interface of the output port, and the hot plug detector (HPD) of the selected input port is output to HPD\_SINK. For the unused ports, the I<sup>2</sup>C interfaces are isolated and the HPD pins are driven to L state.

### 4.1 Adaptive equalizer

The equalizer dramatically reduces the intersymbol interference (ISI) jitter and attenuation from long or lossy transmission media. The inputs present high impedance when the device is not active or when V<sub>CC</sub> is absent or 0 V. In all other cases, the 50 Ω termination resistors on input channels are present.

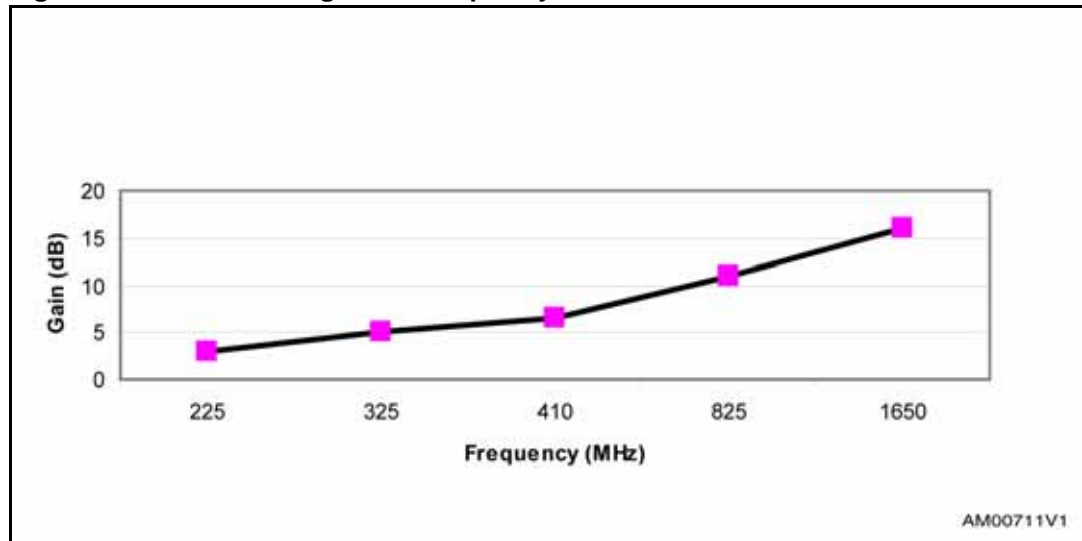
This circuit helps to improve the signal eye pattern significantly. Shaping is performed by the gain stage of the equalizer to compensate the signal degradation and then the signals are driven on to the output ports.

The equalizer is fully adaptive and automatic in function providing smaller gain at low frequencies and higher gain at high frequencies. The equalizer is optimized internally for an adaptive operation.

**Table 3. Gain frequency response**

Frequency (MHz)	Gain in dB
225	3
325	5
410	6.5
825	11
1650	16

Figure 6. STDVE103A gain vs. frequency



The STDVE103A equalizer is fully adaptive and automatic in function. The equalizer's performance is optimized for all frequencies over the cable lengths from 1 m to 25 m.

### Input termination

The STDVE103A integrates precise  $50 \Omega \pm 5\%$  termination resistors, pulled up to  $V_{CC}$ , on all its differential input channels. External terminations are not required. This gives better performance and also minimizes the PCB board space. These on-chip termination resistors should match the differential characteristic impedance of the transmission line. Since the output driver consists of current steering devices, an output voltage is not generated without a termination resistor. Output voltage levels are dependent on the value of the total termination resistance. The STDVE103A produces TMD5 output levels for point-to-point links that are doubly terminated ( $100 \Omega$  at each end). With the typical 10 mA output current, the STDVE103A produces an output voltage of  $3.3 - 0.5 V = 2.8 V$  when driving a termination line terminated at each end. The input terminations are selectable thus saving power for the unselected ports.

### Output buffers

Each differential output of the STDVE103A drives external  $50 \Omega$  load (pull-up resistor) and conforms to the TMD5 voltage standard. The output drivers consist of 10 mA differential current-steering devices.

The driver outputs are short-circuit current limited and are high-impedance to ground when  $S1, S2 = HL$  or the device is not powered. The current steering architecture requires a resistive load to terminate the signal to complete the transmission loop from  $V_{CC}$  to GND through the termination resistor. Because the device switches the direction of the current flow and not voltage levels, the output voltage swing is determined by  $V_{CC}$  minus the voltage drop across the termination resistor. The output current drivers are controlled by the  $S1, S2$  pin and are turned off when  $S1, S2$  is a HL. A stable 10 mA current is derived by accurate internal current mirrors of a stable reference current which is generated by band-gap voltage across the REXT. The differential output driver provides a typical 10 mA current sink capability, which provides a typical 500 mV voltage drop across a  $50 \Omega$  termination resistor.

**TMDS voltage levels**

The TMDS interface standard is a signaling method intended for point-to-point communication over a tightly controlled impedance medium. The TMDS standard uses a lower voltage swing than other common communication standards, achieving higher data rates with reduced power consumption while reducing EMI emissions and system susceptibility to noise. The device is capable of detecting differential signals as low as 100 mV within the entire common mode voltage range.

## 4.2 Operating modes

### 4.2.1 SEL operating modes

The active source is selected by configuring source select inputs, S1 and S2. The selected TMDS inputs from each port are switched through a 3-to-1 multiplexer. The I<sup>2</sup>C interface of the selected input port is linked to the I<sup>2</sup>C interface of the output port, and the hot plug detector (HPD) of the selected input port is output to HPD\_SINK.

**Table 4. SEL operating modes**

Control pins			I/O selected	Hot-plug detect status		
S2	S1	Y/Z	SCL_SINK SDA_SINK	HPD1	HPD2	HPD3
H	H	A1/B1 terminations of A2/B2 and A3/B3 are disconnected	SCL1 SDA1	HPD_SINK	L	L
H	L	A2/B2 terminations of A1/B1 and A3/B3 are disconnected	SCL2 SDA2	L	HPD_SINK	L
L	L	A3/B3 terminations of A1/B1 and A2/B2 are disconnected	SCL3 SDA3	L	L	HPD_SINK
L	H	None (Z). All terminations are disconnected	None (Z) Are pulled high by external pullup termination	L	L	L

H: logic high; L: logic low; X: don't care; Z: high impedance

## 4.3 HPD pins

The input pin HPD\_SINK is 5 V tolerant, allowing direct connection to 5 V signals. The switch is able to pass both 0 V and 5 V signal levels. The HPD\_SINK is an input pin while the HPD1, HPD2 and HPD3 are outputs.

## 4.4 DDC channels

The DDC channels are designed with a bi-directional NMOS gate, providing 5 V signal tolerance. The 5 V tolerance allows direct connection to a standard I<sup>2</sup>C bus, thus eliminating the need for a level shifter. There should be external pull-up resistors on either side of the device on both the SCL and SDA lines.

## 4.5 I<sup>2</sup>C DDC line repeater

The device contains two identical bi-directional open-drain, non-inverting buffer circuits that enable I<sup>2</sup>C DDC bus lines to be extended without degradation in system performance. The STDVE103A buffers both the serial data (DDC SDA) and serial clock (DDC SCL) on the I<sup>2</sup>C bus, while retaining all the operating modes and features of the I<sup>2</sup>C system. This enables two buses of 400 pF bus capacitance to be connected in an I<sup>2</sup>C application. These buffers are operational from a supply voltage of 3.0 to 3.6 V.

The I<sup>2</sup>C bus capacitance limit of 400 pF restricts the number of devices and bus length. The STDVE103A enables the system designer to isolate the two halves of a bus, accommodating more I<sup>2</sup>C devices or longer trace lengths. It can also be used to run two buses, one at 5 V and the other at 3.3 V or a 400 kHz and 100 kHz bus, where the 100 kHz bus is isolated when 400 kHz operation of the other bus is required. The STDVE103A can be used to run the I<sup>2</sup>C bus at both 5 V and 3.3 V interface levels.

Two or more STDVE103As cannot be connected in series. The STDVE103A design does not allow this configuration. Since there is no direction pin, slightly different “legal” low voltage levels are used to avoid lock-up conditions between the input and output. A valid low applied at the input of STDVE103A is propagated as a buffered low with a slightly higher value on the enabled outputs.

When this buffered low is applied to another STDVE103A in series, the second STDVE103A will not recognize it as a valid low and will not propagate it as a buffered low again.

The S1 and S2 (SEL) lines act as control signals for the corresponding A, B or C ports. Note that the SEL line has an internal pull-down resistor. The SEL line should not change state during an I<sup>2</sup>C operation, because disabling during bus operation hangs the bus and enabling part way through a bus cycle could confuse the I<sup>2</sup>C parts being enabled. The SEL input should change state only when the global bus and the repeater port are in idle state, to prevent system failures.

The output low levels for each internal buffer are approximately 0.5 V, but the input voltage of each internal buffer must be 70 mV or more below the output low level, when the output internally is driven low. This prevents a lock-up condition from occurring when the input low condition is released.

As with the standard I<sup>2</sup>C system, pull up resistors are required to provide the logic high levels on the buffered bus. The STDVE103A has standard open collector configuration of the I<sup>2</sup>C bus. The size of the pull up resistors depends on the system, but each side of the repeater must have a pull up resistor.

This part is designed to work with standard mode and fast mode I<sup>2</sup>C devices. Standard mode I<sup>2</sup>C devices only specify 3 mA output drive, this limits the termination current to 3 mA in a generic I<sup>2</sup>C system where standard mode devices and multiple masters are possible. Under certain conditions, higher termination currents can be used.

## 4.6 Power-down condition

The HL combination of S1, S2 is used to disable most of the internal circuitry of STDVE103A that puts the device in a low power mode of operation.



## 4.7 Bias

The bandgap reference voltage over the external  $R_{EXT}$  reference resistor sets the internal bias reference current. This current and its factors (achieved by employing highly accurate and well matched current mirror circuit topologies) are generated on-chip and used by several internal modules. The 10 mA current used by the transmitter block is also generated using this reference current. It is important to ensure that the  $R_{EXT}$  value is within the  $\pm 1\%$  tolerance range of its typical value.

**Table 5. Bias parameter**

Parameter	Min	Typ	Max	Unit
Bandgap voltage		1.2		V

The output voltage swing depends on 3 components: supply voltage ( $V_{supply}$ ), termination resistor ( $R_T$ ) and current drive ( $I_{drive}$ ). The supply voltage can vary from  $3.3\text{ V} \pm 5\%$ , termination resistor can vary from  $50\ \Omega \pm 10\%$ .

The voltage on the output is given by:

$$V_{supply} - I_{drive} \times R_T$$

The variation on  $I_{drive}$  must be controlled to ensure that the voltage on HDMI output is within the HDMI specification under all conditions.

This is achieved when:

$$400\text{mV} \leq I_{drive} \times R_T \leq 600\text{mV}$$

with typical value centered at 500 mV.

## 4.8 Timing between HPD and DDC

It is important to ensure that the I<sup>2</sup>C DDC interface is ready by the time the HPD detection is complete.

As soon as the discovery is finished by the HPD detection, the configuration data is exchanged between a source and sink through the I<sup>2</sup>C DDC interface. The STDVE003's DDC interface is ready for communication as soon as the power supply to the chip is present and stable. When the desired port is enabled and the chip is out of shutdown mode, the I<sup>2</sup>C DDC lines can be used for communication.

Thus, as soon as the HPD detection sequence is complete, the DDC interface can be readily used. There is no delay between the HPD detection and I<sup>2</sup>C DDC interface to be ready.

## 5 Maximum rating

Stressing the device above the rating listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

**Table 6. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Supply voltage to ground	-0.5 to +4.0	V
V <sub>DD</sub>	Supply voltage to Ground (DDC, HPD, S1, S2)	-0.5 to +6.0	
V <sub>I</sub>	DC input voltage (TMDS ports)	1.7 to +4.0	V
	SDA1, SCL1, SDA2, SCL2, SDA3, SCL3, SDA_SINK, SCL_SINK, HPD_SINK, HPD1, HPD2, HPD3, S1, S2	-0.5 to +6.0	V
I <sub>O</sub>	DC output current	120	mA
T <sub>STG</sub>	Storage temperature	-65 to +150	°C
T <sub>L</sub>	Lead temperature (10 sec)	300	°C
V <sub>ESD</sub>	Electrostatic discharge voltage on all IOs	Human body model	-5 to +5 kV

**Table 7. Thermal data**

Symbol	Parameter	TQFP-64	Unit
Θ <sub>JA</sub>	Thermal coefficient (junction-ambient)	TBD	°C/W

## 5.1 Recommended operating conditions

## 5.2 DC electrical characteristics

$T_A = -40$  to  $+85$  °C,  $V_{CC} = 3.3$  V  $\pm$  5% <sup>(a)</sup>

**Table 8. Power supply characteristics**

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
$V_{CC}$	Supply voltage		3.135	3.3	3.465	V
$V_{DD}$	Supply voltage		4.5	5.0	5.5	V
$I_{CC}$	Supply current	All inputs/outputs are enabled. Inputs are terminated with 50 $\Omega$ to $V_{CC}$ . $V_{CC} = 3.465$ V Data rate = 3.4 Gbps			300	mA
$I_{CC}$	Supply current	S1, S2 = HL			20	mA
$I_{DD}$	Supply current ( $V_{DD}$ supply)			2	5	mA

**Table 9. DC specifications for TMD5 differential inputs**

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
$V_{TH}$	Differential input high threshold (peak-to-peak)	$V_{CC} = 3.465$ V over the entire $V_{CMR}$		0	150	mV
$V_{TL}$	Differential input low threshold	$V_{CC} = 3.465$ V over the entire $V_{CMR}$	-150	0		mV
$V_{ID}$	Differential input voltage (peak-to-peak) <sup>(1)</sup>	$V_{CC} = 3.465$ V	150		1560	mV
$V_{CMR}$	Common mode voltage range		$V_{CC} - 0.3$		$V_{CC} - 0.04$	V
$C_{IN}$	Input capacitance	IN+ or IN- to GND F = 1 MHz		3.5		pF

1. Differential output voltage is defined as  $|(OUT+ - OUT-)|$ .  
Differential input voltage is defined as  $|(IN+ - IN-)|$ .

a. Typical parameters are measured at  $V_{CC} = 3.3$  V,  $T_A = +25$  °C.

Table 10. DC specifications for TMD5 differential outputs

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
$V_{OH}$	Single-ended high level output voltage		$V_{CC}-10$		$V_{CC}+10$	mV
$V_{OL}$	Single-ended low level output voltage		$V_{CC}-600$		$V_{CC}-400$	mV
$V_{swing}$	Single ended output swing voltage	$V_{CC} = 3.3\text{ V}$ $R_{TERM} = 50\ \Omega$	400	500	600	mV
$V_{OD}$	Differential output voltage (peak-to-peak) <sup>(1)</sup>	$V_{CC} = 3.3\text{ V}$ $R_{TERM} = 50\ \Omega$	800	1000	1200	mV
$I_{OH}$	Differential output high level current		0		50	$\mu\text{A}$
$I_{OL}$	Differential output low level current		8	10	12	mA
$I_{sc}$	Output driver short-circuit current (continuous)	$OUT_{\pm} = \text{GND}$ through a $50\ \Omega$ resistor. See <a href="#">Figure 11</a>			12	mA
$C_{OUT}$	Output capacitance	$OUT+$ or $OUT-$ to GND when tri-state $F = 1\text{ MHz}$		5.5		pF

1. Differential output voltage is defined as  $|(OUT+ - OUT-)|$ . Differential input voltage is defined as  $|(IN+ - IN-)|$

Table 11. DC specifications for SEL (S1, S2) inputs

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
$V_{IH}$	HIGH level input voltage	High level guaranteed	2.0			V
$V_{IL}$	LOW level input voltage	Low level guaranteed	-0.5		0.8	V
$V_{IK}$	Clamp diode voltage	$V_{CC} = 3.465\text{ V}$ $I_{IN} = -18\text{ mA}$	-1.2	-0.8		V
$I_{IH}$	Input high current	$V_{CC} = 3.465\text{ V}$ $V_{IN} = V_{CC}$	-5		+5	$\mu\text{A}$
$I_{IL}$	Input low current	$V_{CC} = 3.465\text{ V}$ $V_{IN} = \text{GND}$	-5		+5	$\mu\text{A}$
$C_{IN}$	Input capacitance	Pin to GND $F = 1\text{ MHz}$		3.5		pF

Table 12. Input termination resistor

Symbol	Parameter	Test condition	Value			Unit
$R_{TERM}$	Differential input termination resistor on $IN_{\pm}$ channels relative to $V_{CC}$	$I_{IN} = -10\text{ mA}$	45	50	55	$\Omega$

Table 13. External reference resistor

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
$R_{EXT}$	Resistor for TMDS compliant voltage swing range	Tolerance for $R = \pm 1\%$		4.7		$\text{K}\Omega$

**Table 14. DDC I/O pins (switch)**

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
$V_{I(DDC)}$	Input voltage		GND		5.3	V
$I_{I(leak)}$	Input leakage current	$V_{CC} = 3.465\text{ V}$ A, B, C ports = 5.3 V Y port = 0.0 V Switch is isolated			6	$\mu\text{A}$
		$V_{CC} = 3.465\text{ V}$ A, B, C ports = 3.3 V Y port = 0.0 V Switch is isolated			2	$\mu\text{A}$
$C_{I/O}$	Input/output capacitance	$V_I = 0\text{ V}$ F = 1 MHz Switch disabled		5		pF
		$V_I = 0\text{ V}$ F = 1 MHz Switch enabled		9		pF

**Table 15. Status pins (HPD\_SINK)**

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
$V_{IH}$	High level input voltage	$V_{CC} = 3.3\text{ V}$ High level guaranteed	2.0		5.3	V
$V_{IL}$	Low level input voltage	$V_{CC} = 3.3\text{ V}$ Low level guaranteed	GND		0.8	V
$I_{I(leak)}$	Input leakage current	$V_{CC} = 3.465\text{ V}$ Y = 5.3 V			4	$\mu\text{A}$
		$V_{CC} = 3.465\text{ V}$ Y = 3.3 V			2	$\mu\text{A}$

Table 16. Status pins (HPD1, HPD2, HPD3)<sup>(1)</sup>

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
V	Voltage		GND		5.3	V
C <sub>I/O</sub>	Input/output capacitance	V <sub>I</sub> = 0 V F = 1 MHz Switch disabled		5		pF
		V <sub>I</sub> = 0 V F = 1 MHz Switch enabled		9		pF
V <sub>OL</sub>	Output low voltage (open drain I/Os)	V <sub>CC</sub> = 3.3 V I <sub>OL</sub> = 8 mA			0.4	V

1. Typical parameters are measured at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = +25 °C.

### 5.3 DC electrical characteristics (I<sup>2</sup>C repeater)

(T<sub>A</sub> = -40 to +85 °C, V<sub>CC</sub> = 3.3 V ± 5%, GND = 0 V; unless otherwise specified)

**Table 17. Supplies**

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
V <sub>CC</sub>	DC supply voltage		3.135	3.3	3.465	V

**Table 18. Input/output SDA, SCL**

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
V <sub>IH</sub>	High level input voltage		0.7 V <sub>CC</sub>		5.3	V
V <sub>IL</sub>	Low level input voltage <sup>(1)</sup>		-0.5		0.3 V <sub>CC</sub>	V
V <sub>ILc</sub>	Low level input voltage contention <sup>(1)</sup>		-0.5		0.4	V
V <sub>IK</sub>	Input clamp voltage	I <sub>I</sub> = -18 mA	–	–	-1.2	V
I <sub>IL</sub>	Input current low (SDA, SCL)	Input current low (SDA, SCL)	–	–	1	μA
I <sub>IH</sub>	Input current high (SDA, SCL)	V <sub>I</sub> = 3.465 V (SDA, SCL)	–	–	10	μA
		V <sub>I</sub> = 5.3 V (SDA, SCL)	–	–	10	μA
V <sub>OL</sub>	LOW-level output voltage	I <sub>OL</sub> = 3 mA			0.4	V
		I <sub>OL</sub> = 6 mA			0.65	V
I <sub>OH</sub>	Output high level leakage current	V <sub>O</sub> = 3.6 V; driver disabled	–	–	10	μA
		V <sub>O</sub> = 5.3 V; driver disabled	–	–	10	μA
C <sub>I</sub>	Input capacitance	V <sub>I</sub> = 3 V or 0 V	–	6	7 <sup>(2)</sup>	pF

1. V<sub>IL</sub> specification is for the first low level seen by the SDA/SCL lines. V<sub>ILc</sub> is for the second and subsequent low levels seen by the SDA/SCL lines.
2. The SCL/SDA C<sub>I</sub> is about 200 pF when V<sub>CC</sub> = 0 V. The STDVE103A should be used in applications where power is secured to the repeater but an active bus remains on either set of the SDA/SCL pins.



## 5.4 Dynamic switching characteristics<sup>(b)</sup>

$T_A = -40$  to  $+85$  °C,  $V_{CC} = 3.3$  V  $\pm$  5%,  $R_{TERM} = 50$   $\Omega$   $\pm$  5%,  $C_L = 5$  pF).

Typical values are at  $T_A = +25$  °C and  $V_{CC} = 3.3$  V.

**Table 19. Clock and data rate**

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
$f_{CK}$	Clock frequency (1/10th of the differential data rate)		25		340	MHz
$D_{rate}$	Signaling rate				3.4	Gbps

**Table 20. Equalizer gain**

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
G_EQ	Equalizer gain	At 225 MHz		10		dB
		At 340 MHz		15		dB

**Table 21. Differential output timings**

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
$t_r$	Differential data and clock output rise/fall times	20% to 80% of $V_{OD}$	75	150	240	ps
$t_f$		80% to 20% of $V_{OD}$	75	150	240	ps
$t_{PLH}$	Differential low to high propagation delay	Alternating 1 and 0 pattern at slow and fast data rates	250		800	ps
$t_{PHL}$	Differential high to low propagation delay	Measure at 50% $V_{OD}$ between input to output	250		800	ps

b. *The timing values in this section are tested during characterization and are guaranteed by design and simulation. Not tested in production.*

**Table 22. Skew times**

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
$t_{SK(O)}$	Inter-pair channel-to-channel output skew				100	ps
$t_{SK(P)}$	Pulse skew	$ t_{PLH} - t_{PHL} $		25	80	ps
$t_{SK(D)}$	Intra-pair differential skew				50	ps
$t_{SK(CC)}$	Output channel to channel skew	Difference in propagation delay ( $t_{PLH}$ or $t_{PHL}$ ) among all output channels		50	125	ps

**Table 23. Turn-on and turn-off times**

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
$t_{ON}$	TMDS output enable time	Time from OE_N to OUT± change from tri-state to active		12	20	ns
$t_{OFF}$	TMDS output disable time	Time from OE_N to OUT± change from active to tri-state		6	10	ns

**Table 24. DDC I/O pins**

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
Refer to <a href="#">Section 5.5</a>						

**Table 25. Status pins (HPD\_SINK, HPD1, HPD2, HPD3, S1, S2)**

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
$t_{PD(HPD)}$	Propagation delay (from Y_HPDP to the active port of HPD)	$C_L = 10 \text{ pF}$ , $R_{PU} = 1 \text{ K}\Omega$		150		ns
$T_{ON/OFF}$	Switch time (from port select to the latest valid status of HPD)	$C_L = 10 \text{ pF}$		50		ns

Table 26. Jitter

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
$t_{JIT}$	Total jitter <sup>(1)</sup>	PRBS pattern at 1.6 Gbps (800 MHz)		35		ps (p-p)

1. Total jitter is measured peak-to-peak with a histogram including 3500 window hits. Stimulus and fixture jitter has been subtracted. Input differential voltage =  $V_{ID} = 500$  mV, PRBS random pattern at 1.65 Gbps,  $t_r=t_f=50$  ps (20% to 80%). Jitter parameter is not production-tested but guaranteed through characterization on a sample-to-sample basis.

## 5.5 Dynamic switching characteristics (I<sup>2</sup>C repeater)

$T_A = -40$  to  $+85$  °C,  $V_{CC} = 3.3$  V  $\pm$  5%.

Typical values are at  $T_A = +25$  °C and  $V_{CC} = 3.3$  V.

Table 27. I<sup>2</sup>C repeater<sup>(1)</sup>

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
f <sub>SCL</sub>	I <sup>2</sup> C clock frequency	Standard mode			100	kHz
		Fast mode			400	kHz
t <sub>LOW</sub>	Low duration on SCL pin	100 KHz See <a href="#">Figure 19</a> Voltage on line = 5V C <sub>max</sub> =400 pF, R <sub>max</sub> = 2 K Depends on input signal rise time. Includes the 20 % time intervals on both transitions.	4.7			μs
		400 KHz See <a href="#">Figure 19</a> Voltage on line = 5V C <sub>max</sub> = 400 pF, R <sub>max</sub> = 2 K Depends on input signal rise time. Includes the 20 % time intervals on both transitions.	1.3			μs
t <sub>LOW</sub>	Low duration on SCL pin	100 KHz See <a href="#">Figure 19</a> Voltage on line = 3.3 V C <sub>max</sub> = 400 pF, R <sub>max</sub> = 2 K Depends on input signal rise time. Includes the 20 % time intervals on both transitions.	4.7			μs
		400 KHz See <a href="#">Figure 19</a> Voltage on line = 3.3 V, C <sub>max</sub> = 400 pF, R <sub>max</sub> = 2 K Depends on input signal rise time. Includes the 20 % time intervals on both transitions.	1.3			μs

Table 27. I<sup>2</sup>C repeater<sup>(1)</sup> (continued)

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
t <sub>HIGH</sub>	High duration on SCL pin	100 KHz See <a href="#">Figure 19</a> Voltage on line = 5 V C <sub>max</sub> = 400 pF, R <sub>max</sub> = 2 K Depends on input signal rise time. Includes the 20 % time intervals on both transitions	4.0			μs
		400 KHz See <a href="#">Figure 19</a> Voltage on line = 5 V C <sub>max</sub> = 400 pF, R <sub>max</sub> =2 K Depends on input signal rise time. Includes the 20 % time intervals on both transitions	0.6			μs
t <sub>HIGH</sub>	High duration on SCL pin	100 KHz Refer section 14.12, Voltage on line = 3.3 V C <sub>max</sub> = 400 pF, R <sub>max</sub> = 2 K Depends on input signal rise time. Includes the 20 % time intervals on both transitions	4.0			μs
		400 KHz See <a href="#">Figure 19</a> Voltage on line = 3.3 V, C <sub>max</sub> =400 pF, R <sub>max</sub> = 2 K Depends on input signal rise time. Includes the 20 % time intervals on both transitions	0.6			μs
t <sub>PHL</sub>	Propagation delay	400 KHz Waveform 1 ( <a href="#">Figure 17</a> ) Voltage on line = 5 V, C <sub>max</sub> = 400 pF, R <sub>max</sub> = 2 K			250	μs
t <sub>PLH</sub>	Propagation delay	400 KHz Waveform 1 ( <a href="#">Figure 17</a> ) Voltage on line = 5 V, C <sub>max</sub> = 400 pF, R <sub>max</sub> = 2 K			300	μs
t <sub>PHL</sub>	Propagation delay	400 KHz Waveform 1 ( <a href="#">Figure 17</a> ) Voltage on line = 3.3 V, C <sub>max</sub> = 400 pF, R <sub>max</sub> = 2 K			250	ns

Table 27. I<sup>2</sup>C repeater<sup>(1)</sup> (continued)

Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
t <sub>PLH</sub>	Propagation delay	400 KHz Waveform 1 (Figure 17) Voltage on line = 3.3 V, C <sub>max</sub> = 400 pF, R <sub>max</sub> = 2 K			450	ns
t <sub>PHL</sub>	Propagation delay	100 KHz Waveform 1 (Figure 17) Voltage on line = 5 V, C <sub>max</sub> = 400 pF, R <sub>max</sub> = 2 K			250	ns
t <sub>PLH</sub>	Propagation delay	100 KHz Waveform 1 (Figure 17) Voltage on line = 5 V, C <sub>max</sub> = 400 pF, R <sub>max</sub> = 2 K			300	ns
t <sub>PHL</sub>	Propagation delay	100 KHz Waveform 1 (Figure 17) Voltage on line = 3.3 V, C <sub>max</sub> = 400 pF, R <sub>max</sub> = 2 K			250	ns
t <sub>PLH</sub>	Propagation delay	100 KHz Waveform 1 (Figure 17) Voltage on line = 3.3 V, C <sub>max</sub> = 400 pF, R <sub>max</sub> = 2 K			450	ns
t <sub>f</sub>	Output fall time	400 KHz Waveform 1 (Figure 17) <sup>(2)</sup> Voltage on line = 5 V C <sub>max</sub> = 400 pF, R <sub>max</sub> = 2 K			300	ns
		400 KHz Waveform 1 <sup>(2)</sup> Voltage on line = 3.3 V C <sub>max</sub> = 400pF, R <sub>max</sub> = 2 K			300	ns
t <sub>f</sub>	Output fall time	100 KHz Waveform 1 (Figure 17) <sup>(2)</sup> Voltage on line = 5 V C <sub>max</sub> = 400 pF, R <sub>max</sub> = 2 K			300	ns
		100 KHz Waveform 1 (Figure 17) <sup>(2)</sup> Voltage on line = 3.3 V C <sub>max</sub> = 400 pF, R <sub>max</sub> = 2 K			300	ns

Table 27. I<sup>2</sup>C repeater<sup>(1)</sup> (continued)

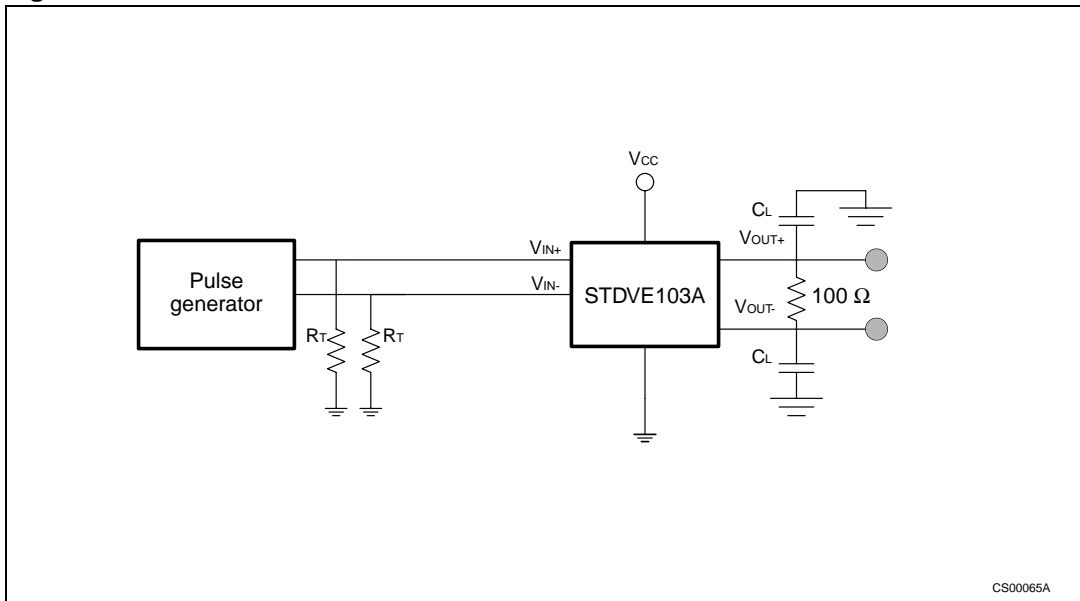
Symbol	Parameter	Test condition	Value			Unit
			Min	Typ	Max	
t <sub>r</sub>	Output rise time	400 KHz Waveform 1 (Figure 17) <sup>(2)</sup> Voltage on line = 5 V Cmax = 400 pF, Rmax = 2 K			300	ns
		400 KHz Waveform 1 (Figure 17) <sup>(2)</sup> Voltage on line = 3.3 V Cmax = 400 pF, Rmax = 2 K			300	ns
t <sub>r</sub>	Output rise time	100 KHz Waveform 1, <sup>(2)</sup> Voltage on line = 5 V Cmax = 400 pF, Rmax = 2 K			1000	ns
		100 KHz Waveform 1 (Figure 17) <sup>(2)</sup> Voltage on line = 3.3 V Cmax = 400 pF, Rmax = 2 K			1000	ns

1. All the timing values are tested during characterization and are guaranteed by design and simulation. Not tested in production.
2. The t<sub>r</sub> transition time is specified with maximum load of 2 kΩ pull-up resistance and 400 pF load capacitance. Different load resistance and capacitance will alter the RC time constant, thereby changing the propagation delay and transition times. Refer to Figure 9.

Table 28. ESD performance

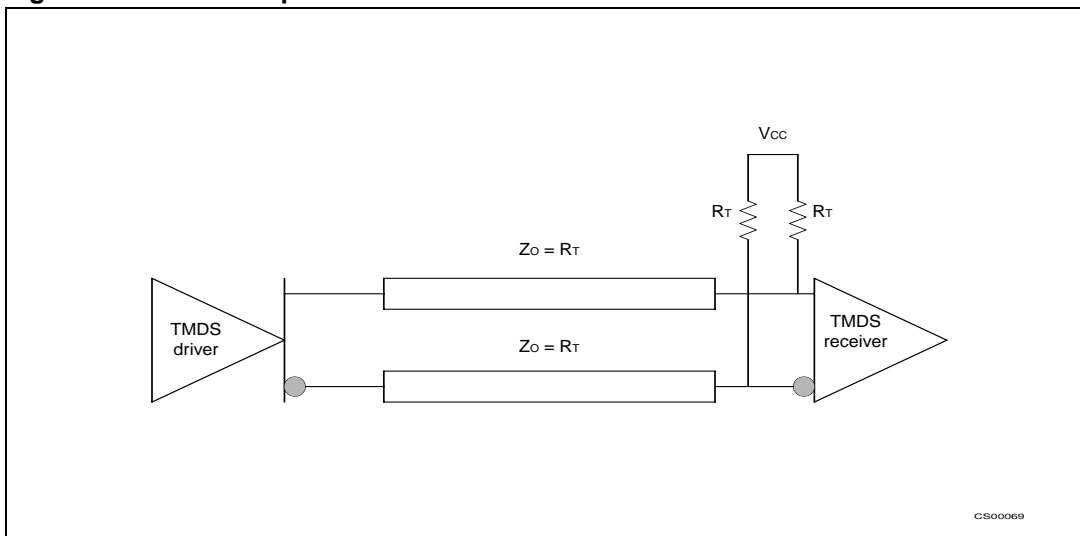
Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
ESD (HBM)	All I/Os	Human body model		±5		kV

Figure 7. Test circuit for electrical characteristics



1.  $C_L$  = load capacitance: include jig and probe capacitance.
2.  $R_T$  = termination resistance; should be equal to  $Z_{OUT}$  of the pulse generator.

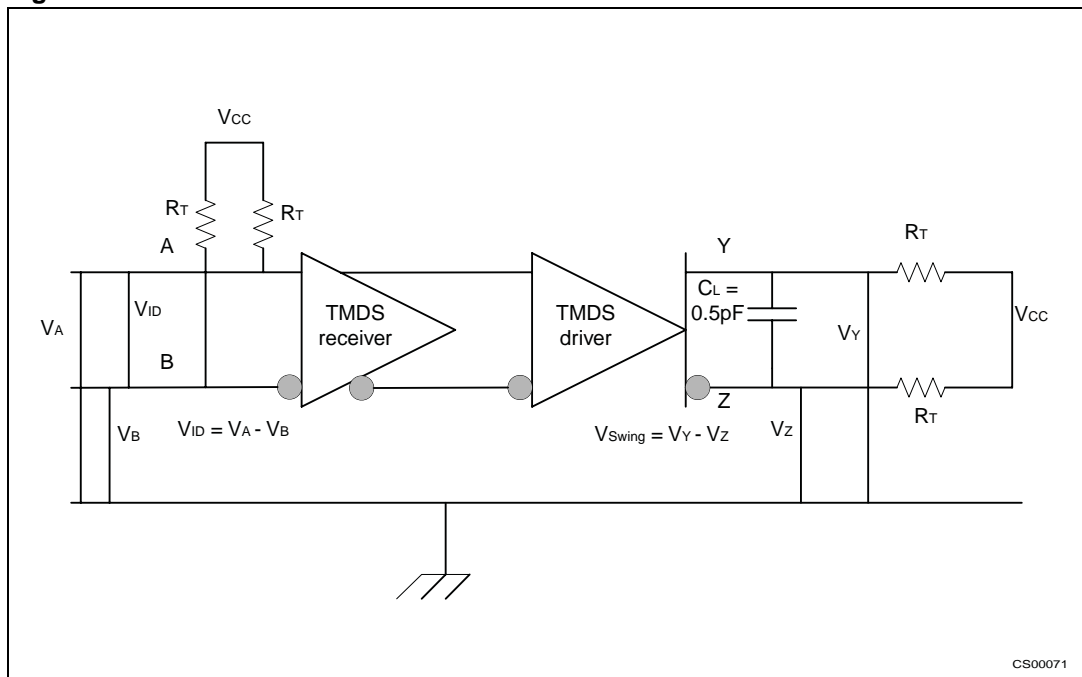
Figure 8. TMDS output driver



1.  $Z_O$  = characteristic impedance of the cable.
2.  $R_T$  = termination resistance: should be equal to  $Z_O$  of the cable. Both are equal to  $50\Omega$ .

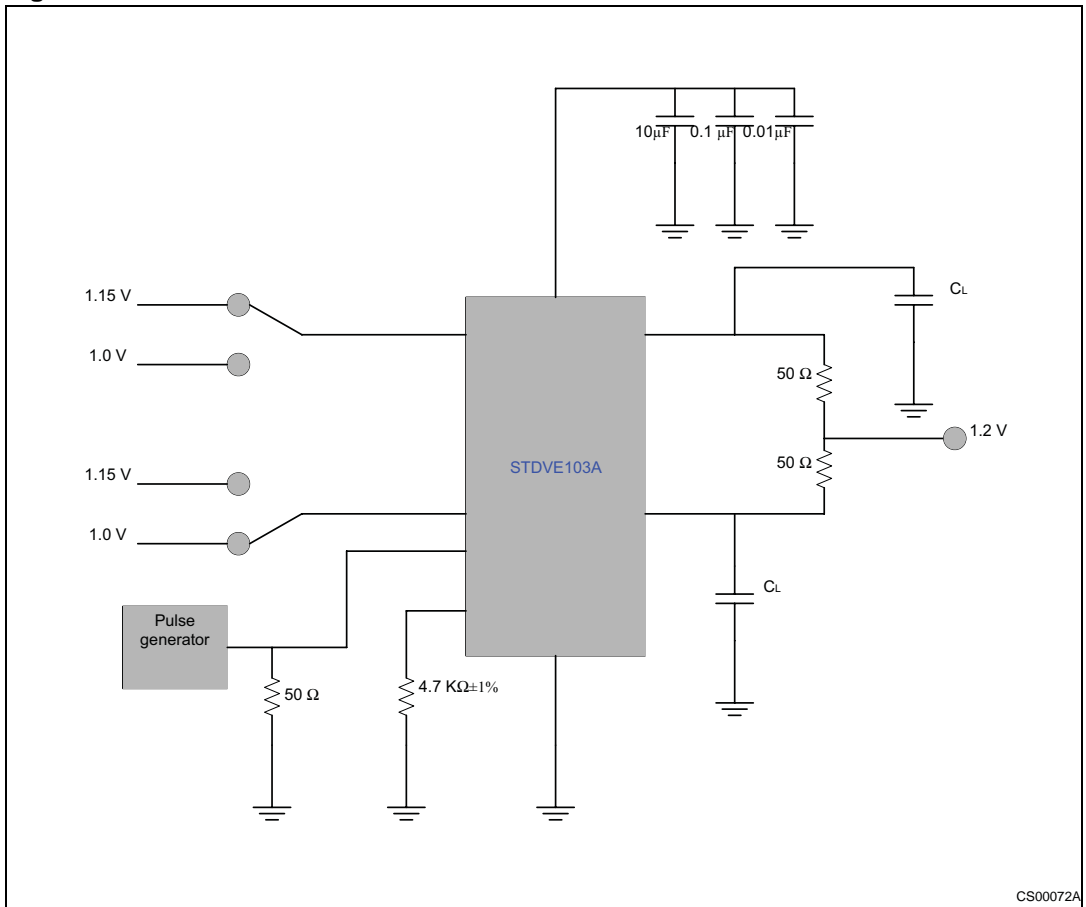


Figure 9. Test circuit for HDMI receiver and driver



1.  $R_T = 50 \Omega$

Figure 10. Test circuit for turn off and turn off times



1.  $C_L = 5 \text{ pF}$

Figure 11. Test circuit for short circuit output current

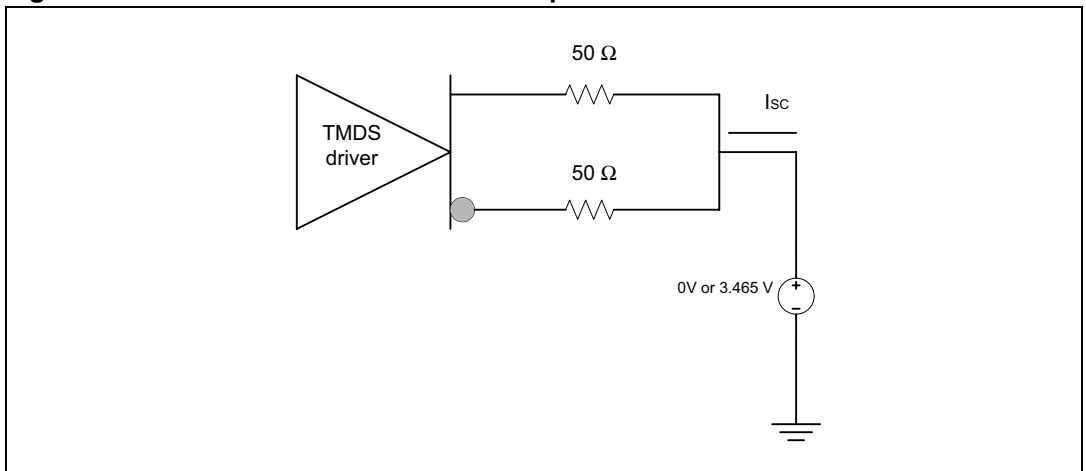


Figure 12. Propagation delays

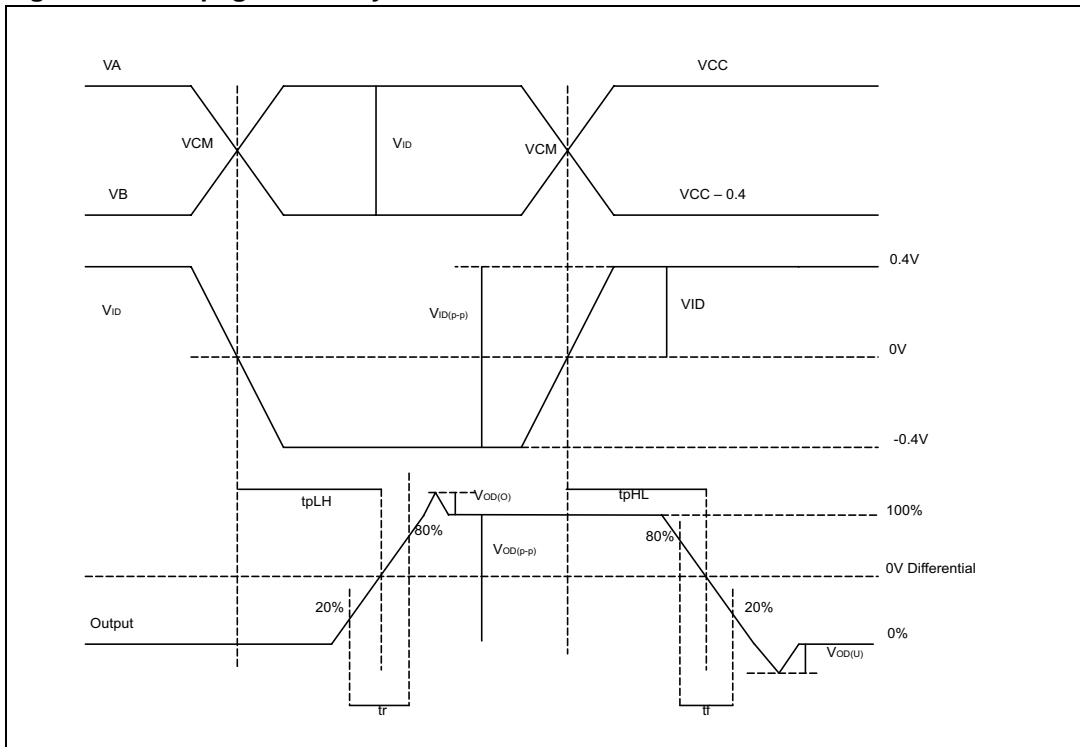


Figure 13. Turn-on and turn-off times

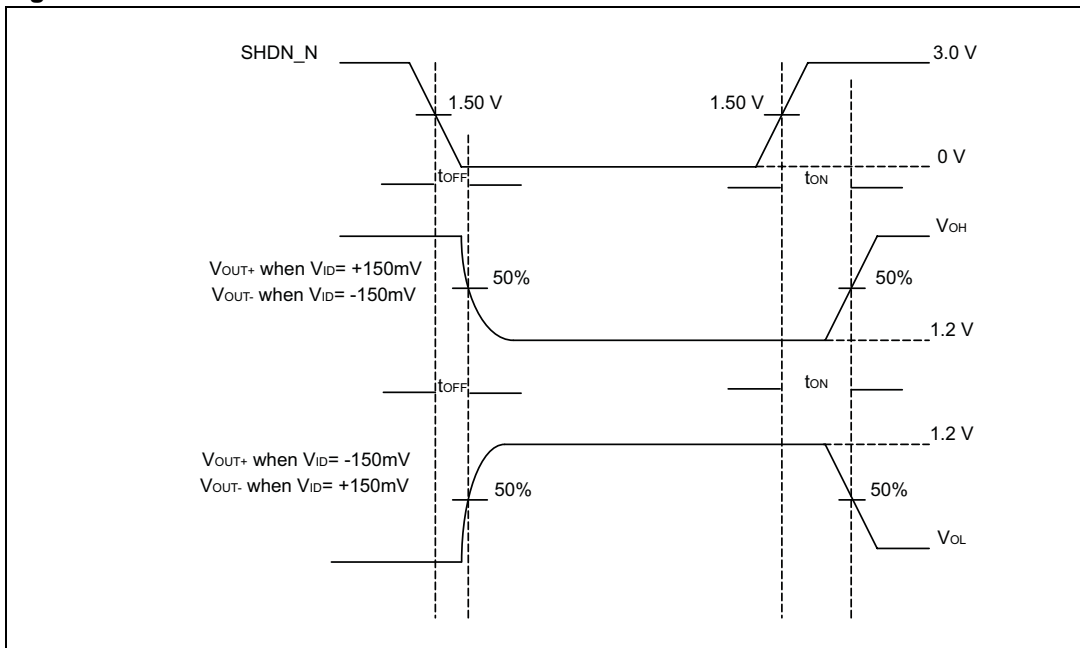


Figure 14. TSK(O)

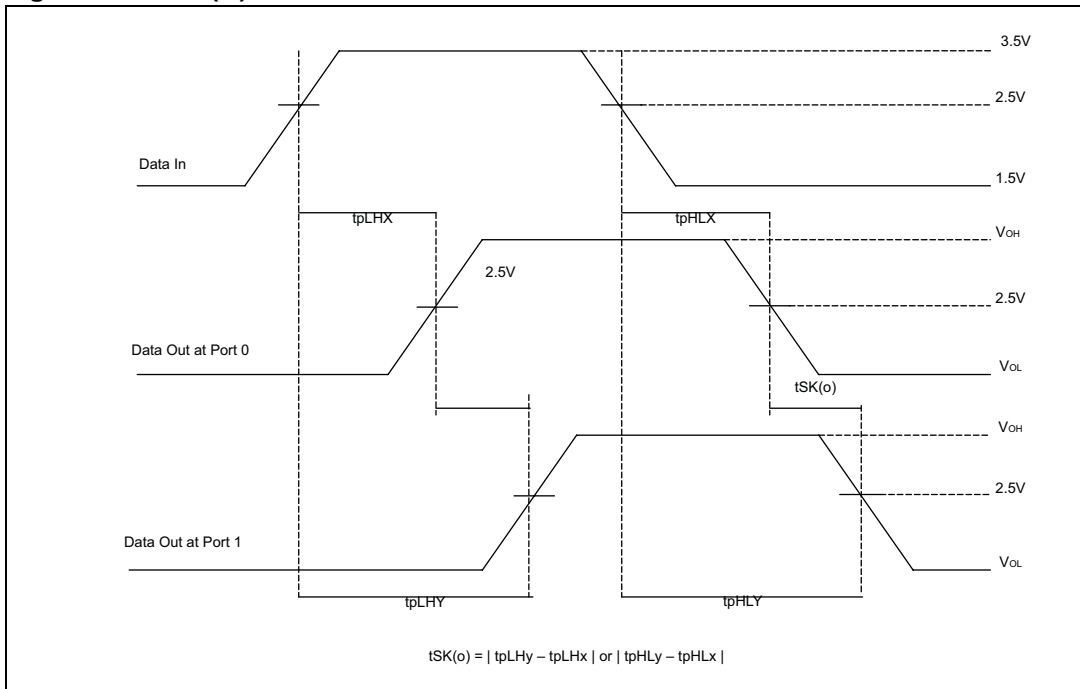


Figure 15. TSK(P)

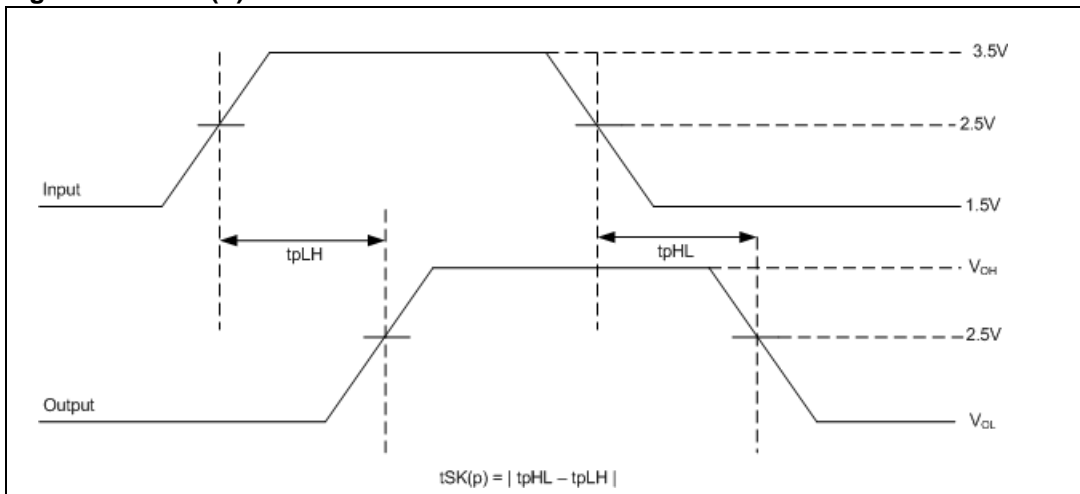


Figure 16. TSK(D)

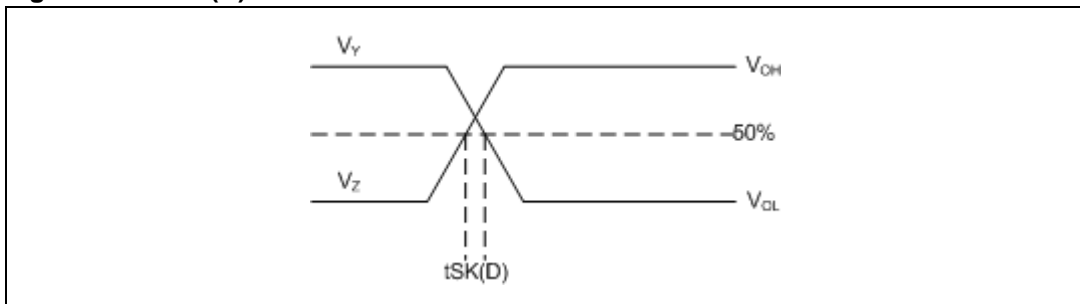


Figure 17. AC waveform 1 (I<sup>2</sup>C lines)

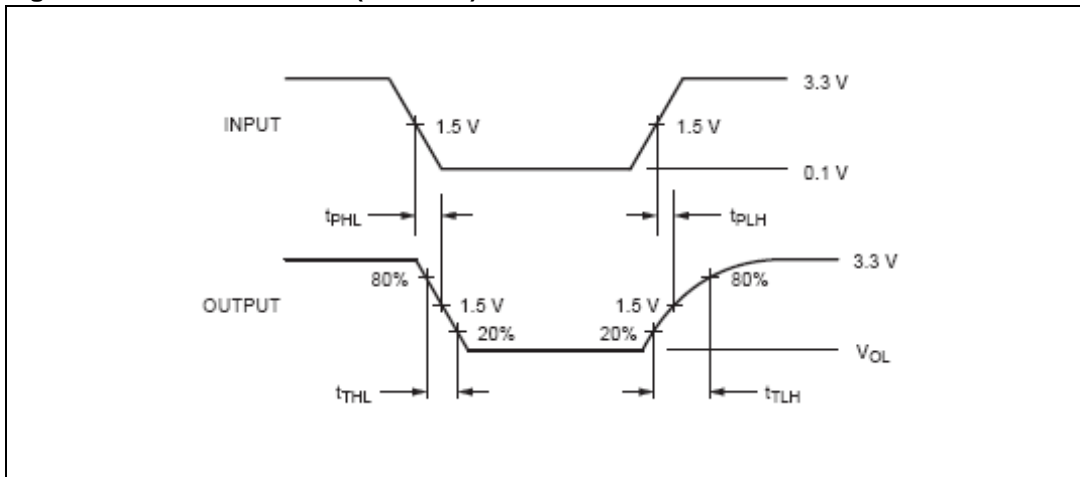


Figure 18. Test circuit for AC measurements (I<sup>2</sup>C lines)

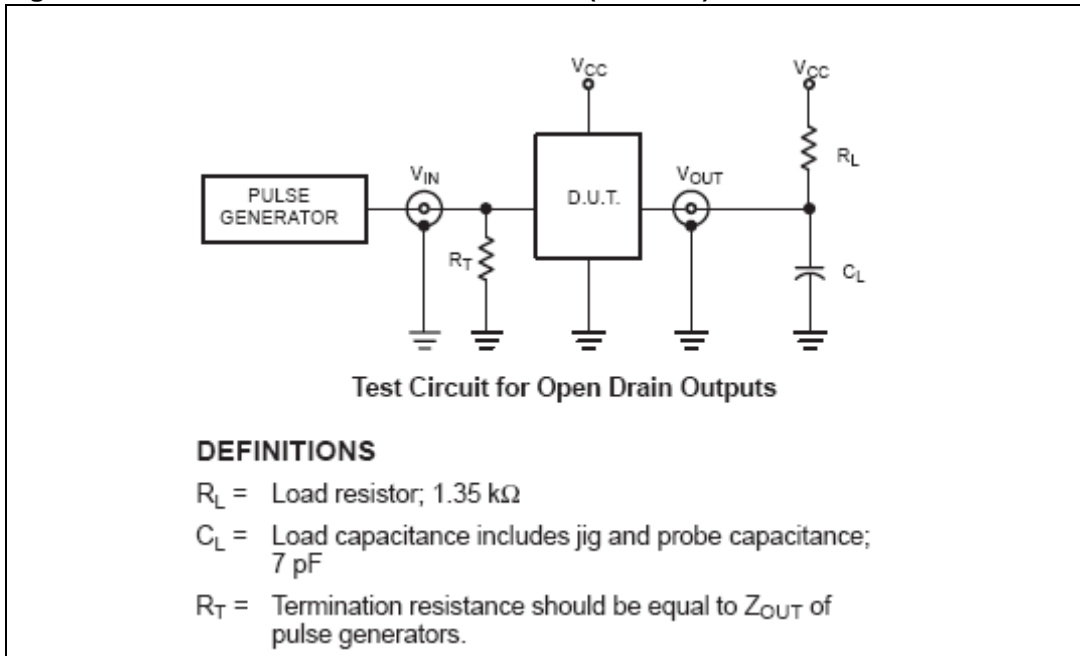
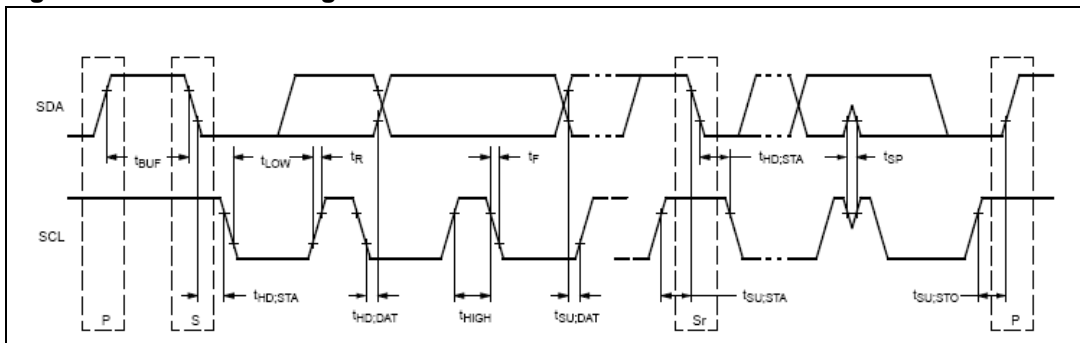


Figure 19. I<sup>2</sup>C bus timing



## 6 Application information

### 6.1 Power supply sequencing

Proper power-supply sequencing is advised for all CMOS devices. It is recommended to always apply  $V_{CC}$  before applying any signals to the input/output or control pins.

### 6.2 Power supply requirements

Bypass each of the  $V_{CC}$  pins with 0.1  $\mu\text{F}$  and 1 nF capacitors in parallel as close to the device as possible, with the smaller-valued capacitor as close to the  $V_{CC}$  pin of the device as possible.

All  $V_{CC}$  pins can be tied to a single 3.3 V power source. A 0.01  $\mu\text{F}$  capacitor is connected from each  $V_{CC}$  pin directly to ground to filter supply noise. The maximum power supply variation can only be  $\pm 5\%$  as per the HDMI specifications.

The maximum tolerable noise ripple on 3.3 V supply must be within a specified limit.

### 6.3 Differential traces

The high-speed TMDS inputs are the most critical parts for the device. There are several considerations to minimize discontinuities on these transmission lines between the connectors and the device.

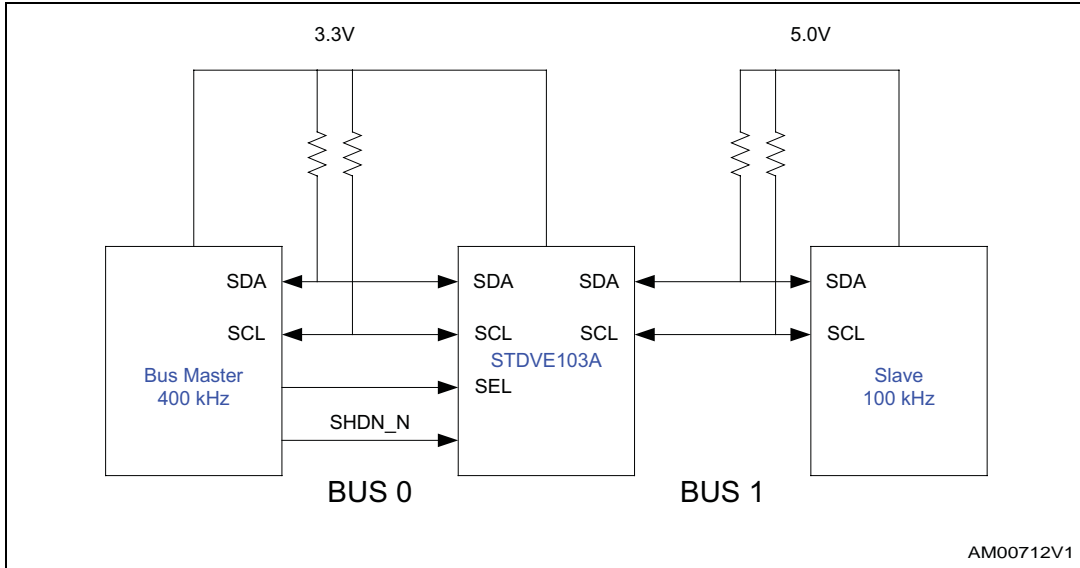
- (a) Maintain 100- $\Omega$  differential transmission line impedance into and out of the STDVE103A.
- (b) Keep an uninterrupted ground plane below the high-speed I/Os.
- (c) Keep the ground-path vias to the device as close as possible to allow the shortest return current path.
- (d) Layout of the TMDS differential inputs should be with the shortest stubs from the connectors.

Output trace characteristics affect the performance of the STDVE103A. Use controlled impedance traces to match trace impedance to both the transmission medium impedance and termination resistor. Run the differential traces close together to minimize the effects of the noise. Reduce skew by matching the electrical length of the traces. Avoid discontinuities in the differential trace layout. Avoid 90 degree turns and minimize the number of vias to further prevent impedance discontinuities.

### 6.3.1 I<sup>2</sup>C lines application information

A typical application is shown in the figure below. In the example, the system master is running on a 3.3 V I<sup>2</sup>C-bus while the slave is connected to a 5 V bus. Both buses run at 100 kHz unless the slave bus is isolated and then the master bus can run at 400 kHz. Master devices can be placed on either bus.

**Figure 20. Typical application of I<sup>2</sup>C bus system**



The STDVE103A DDC lines are 5 V tolerant; so it does not require any extra circuitry to translate between the different bus voltages.

# 7 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK<sup>®</sup> packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

Figure 21. TQFP64 package outline

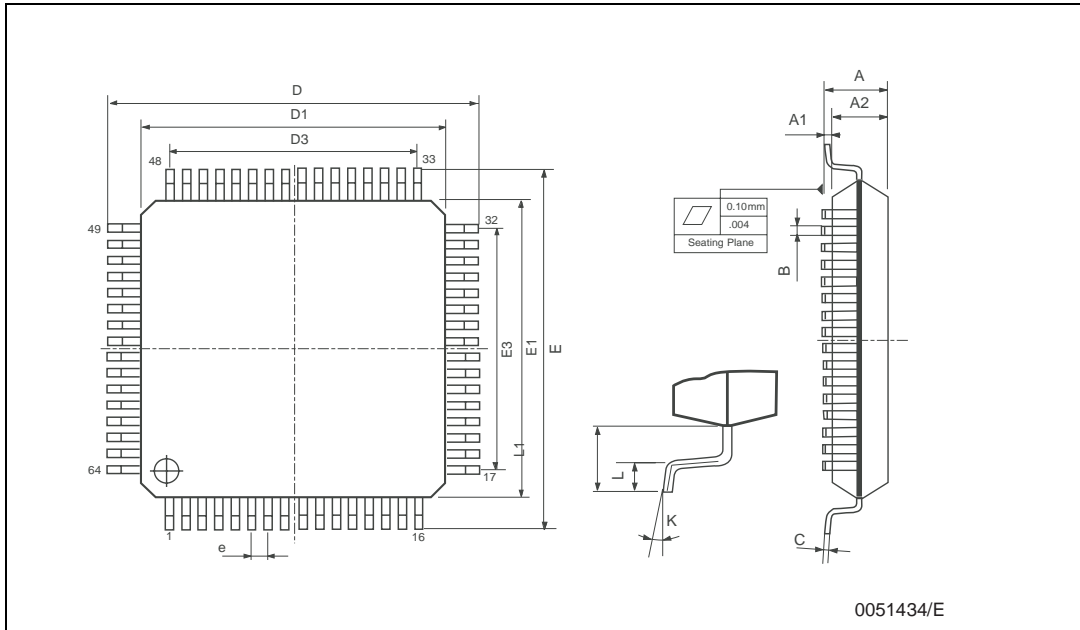
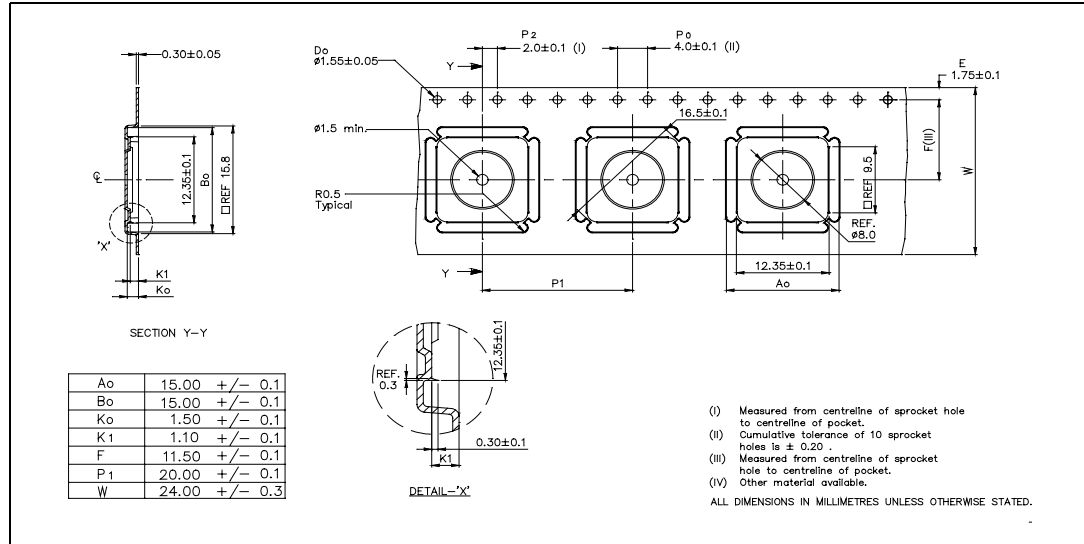




Table 29. TQFP64 mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A			1.20
A1	0.05	0.10	0.15
A2	0.95	1	1.05
b	0.17	0.22	0.27
c	0.09	0.15	0.20
D	11.80	12	12.20
D1	9.80	10	10.20
D3		7.50	
E	11.80	12	12.20
E1	9.80	10	10.20
E3		7.50	
e		0.50	
L	0.45	0.60	0.75
L1		1	
K	0°		7°

Figure 22. TQFP64 tape and reel information



## 8 Revision history

**Table 30. Document revision history**

Date	Revision	Changes
21-Jul-2008	1	Initial release.

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