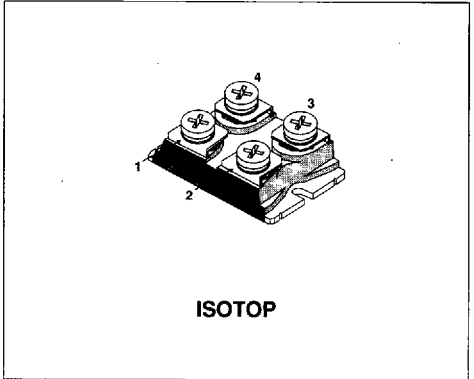


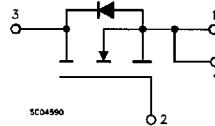
**N - CHANNEL ENHANCEMENT MODE
POWER MOS TRANSISTOR IN ISOTOP PACKAGE**

| TYPE | V _{DSS} | R _{DS(on)} | I _D |
|-----------|------------------|---------------------|----------------|
| STE180N05 | 50 V | < 0.006 Ω | 180 A |

- HIGH CURRENT POWER MODULE
- AVALANCHE RUGGED TECHNOLOGY (SEE STH65N05 FOR RATING)
- VERY LARGE SOA - LARGE PEAK POWER CAPABILITY
- EASY TO MOUNT
- SAME CURRENT CAPABILITY FOR THE TWO SOURCE TERMINALS
- EXTREMELY LOW R_{th} JUNCTION TO CASE
- VERY LOW DRAIN TO CASE CAPACITANCE
- VERY LOW INTERNAL PARASITIC INDUCTANCE (TYPICALLY < 5 nH)
- ISOLATED PACKAGE UL RECOGNIZED (FILE No E81743)



INTERNAL SCHEMATIC DIAGRAM



INDUSTRIAL APPLICATIONS:

- SMPS & UPS
- MOTOR CONTROL
- WELDING EQUIPMENT
- OUTPUT STAGE FOR PWM, ULTRASONIC CIRCUITS

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---------------------|---|------------|------|
| V _{DS} | Drain-Source Voltage (V _{GS} = 0) | 50 | V |
| V _{DGR} | Drain-Gate Voltage (R _{GS} = 20 kΩ) | 50 | V |
| V _{GS} | Gate-Source Voltage | ± 20 | V |
| I _D | Drain Current (continuous) at T _c = 25 °C | 180 | A |
| I _D | Drain Current (continuous) at T _c = 100 °C | 115.5 | A |
| I _{DM} (*) | Drain Current (pulsed) | 540 | A |
| P _{tot} | Total Dissipation at T _c = 25 °C | 360 | W |
| | Derating Factor | 2.9 | W/°C |
| T _{stg} | Storage Temperature | -55 to 150 | °C |
| T _j | Max. Operating Junction Temperature | 150 | °C |
| V _{ISO} | Insulation Withstand Voltage (AC-RMS) | 2500 | V |

(*) Pulse width limited by safe operating area

THERMAL DATA

| | | | | |
|----------------|---|-----|------|------|
| $R_{thj-case}$ | Thermal Resistance Junction-case | Max | 0.35 | °C/W |
| R_{thc-h} | Thermal Resistance Case-heatsink With Conductive Grease Applied | Max | 0.05 | °C/W |

ELECTRICAL CHARACTERISTICS ($T_{case} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

OFF

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---------------|--|---|------|------|-----------|---------------------|
| $V_{(BR)DSS}$ | Drain-source Breakdown Voltage | $I_D = 1\text{ mA}$ $V_{GS} = 0\text{ V}$ | 50 | | | V |
| I_{DSS} | Zero Gate Voltage Drain Current ($V_{GS} = 0$) | $V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating} \times 0.8$ $T_c = 125\text{ }^{\circ}\text{C}$ | | | 400 2 | μA mA |
| I_{GSS} | Gate-body Leakage Current ($V_{DS} = 0$) | $V_{GS} = \pm 20\text{ V}$ | | | ± 400 | nA |

ON (*)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|--------------|-----------------------------------|--|------|-------|-------|----------|
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS} = V_{GS}$ $I_D = 1\text{ mA}$ | 2 | | 4 | V |
| $R_{DS(on)}$ | Static Drain-source On Resistance | $V_{GS} = 10\text{ V}$ $I_D = 90\text{ A}$ | | 0.004 | 0.006 | Ω |

DYNAMIC

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|-------------------------------------|---|---|------|------|--------------------|----------------|
| $g_{fs} (*)$ | Forward Transconductance | $V_{DS} = 15\text{ V}$ $I_D = 90\text{ A}$ | | 100 | | S |
| C_{iss} C_{oss} C_{rss} | Input Capacitance Output Capacitance Reverse Transfer Capacitance | $V_{DS} = 25\text{ V}$ $f = 1\text{ MHz}$ $V_{GS} = 0\text{ V}$ | | | 12 5200 1200 | nF pF pF |

SWITCHING ON

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|----------------------|---------------------------|---|------|-----------|------|------------------|
| $t_{d(on)}$ t_r | Turn-on Time Rise Time | $V_{DD} = 25\text{ V}$ $I_D = 90\text{ A}$ $R_G = 4.7\text{ }\Omega$ $V_{GS} = 10\text{ V}$ (see test circuit, figure 1) | | 55 210 | | ns ns |
| $(di/dt)_{on}$ | Turn-on Current Slope | $V_{DD} = 40\text{ V}$ $I_D = 180\text{ A}$ $R_G = 4.7\text{ }\Omega$ $V_{GS} = 10\text{ V}$ (see test circuit, figure 3) | | 900 | | A/ μs |
| Q_g | Total Gate Charge | $V_{DD} = 40\text{ V}$ $I_D = 180\text{ A}$ $V_{GS} = 10\text{ V}$ | | 270 | | nC |

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING OFF

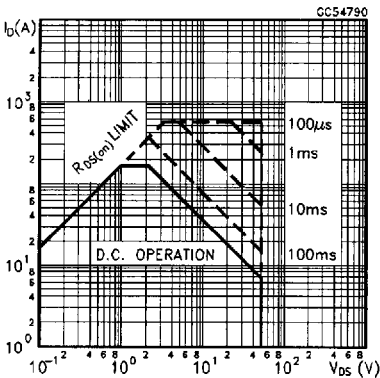
| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---------------|-----------------------|---|------|------|------|------|
| $t_{r(voff)}$ | Off-voltage Rise Time | $V_{DD} = 40\text{ V}$ $I_D = 180\text{ A}$ | | 40 | | ns |
| t_f | Fall Time | $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ | | 315 | | ns |
| t_c | Cross-over Time | (see test circuit, figure 3) | | 440 | | ns |

SOURCE DRAIN DIODE

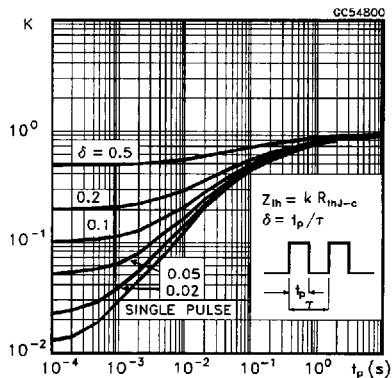
| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|--------------------|-------------------------------|--|------|------|------|------|
| I_{SD} | Source-drain Current | | | | 180 | A |
| $I_{SDM}(\bullet)$ | Source-drain Current (pulsed) | | | | 540 | A |
| $V_{SD}(\ast)$ | Forward On Voltage | $I_{SD} = 180\text{ A}$ $V_{GS} = 0$ | | | 1.6 | V |
| t_{rr} | Reverse Recovery Time | $I_{SD} = 180\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 25\text{ V}$ $T_j = 150\text{ }^\circ\text{C}$ (see test circuit, figure 3) | | 160 | | ns |
| Q_{rr} | Reverse Recovery Charge | | | 480 | | nC |
| I_{RRM} | Reverse Recovery Current | | | 6 | | A |

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %
 (•) Pulse width limited by safe operating area

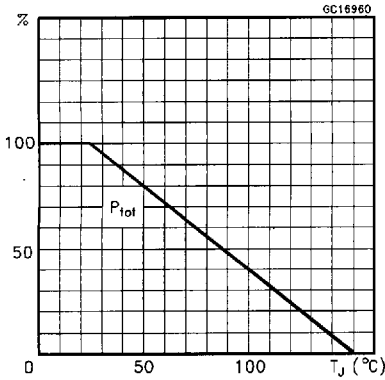
Safe Operating Area



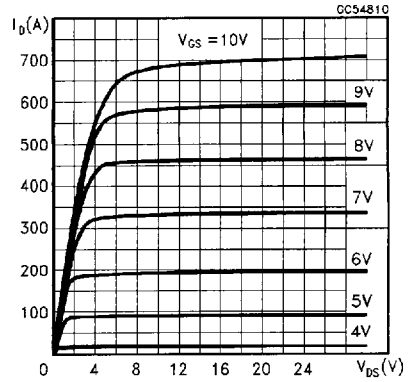
Thermal Impedance



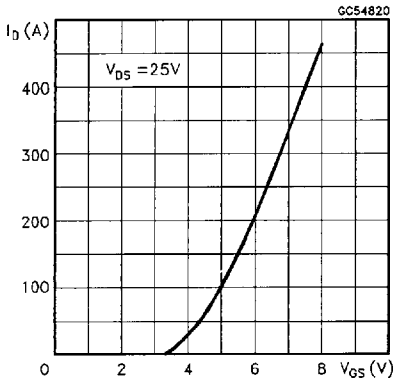
Derating Curve



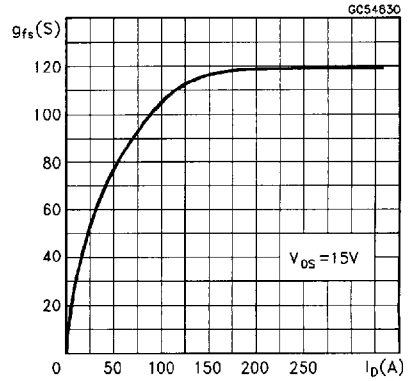
Output Characteristics



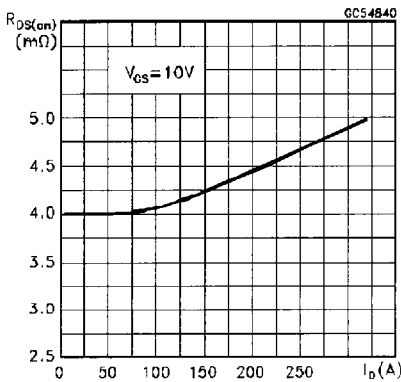
Transfer Characteristics



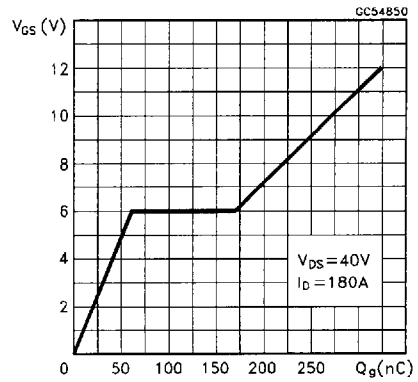
Transconductance



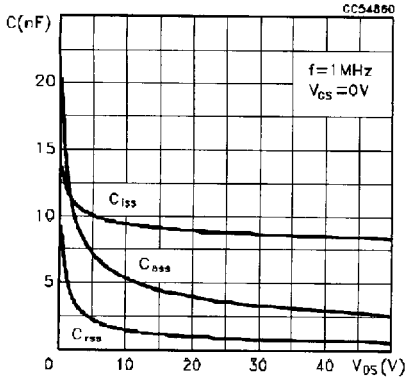
Static Drain-source On Resistance



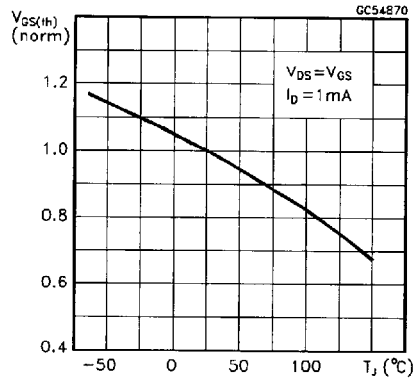
Gate Charge vs Gate-source Voltage



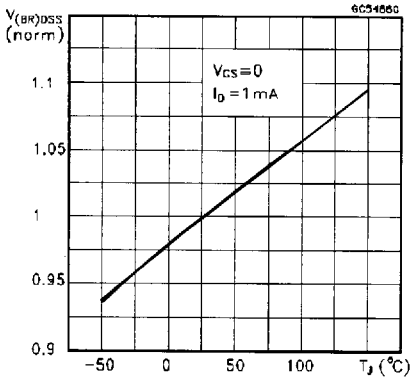
Capacitance Variations



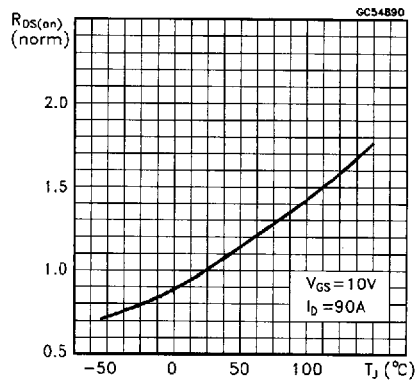
Normalized Gate Threshold Voltage vs Temperature



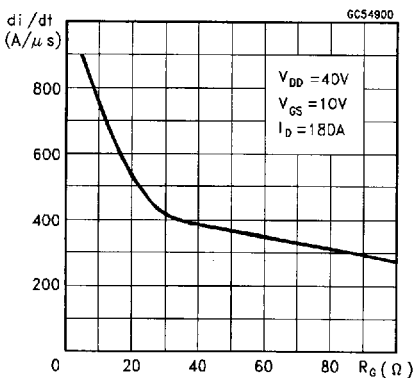
Normalized Breakdown Voltage vs Temperature



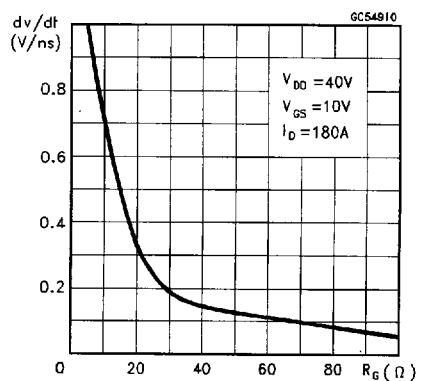
Normalized On Resistance vs Temperature



Turn-on Current Slope



Turn-off Drain-source Voltage Slope



Cross-over Time

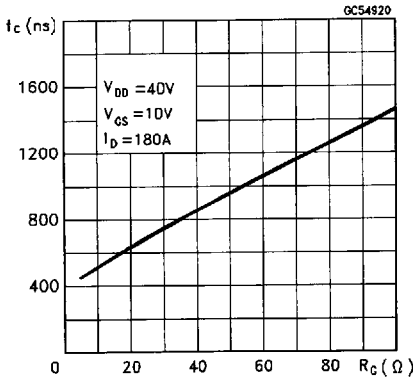
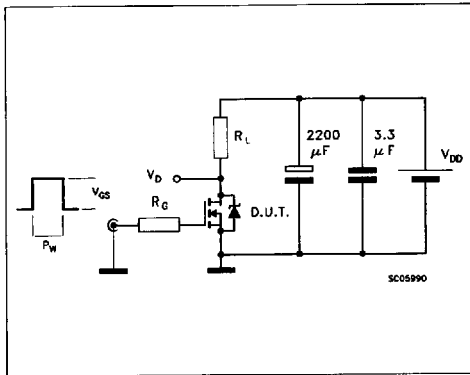


Fig. 1: Switching Times Test Circuits For Resistive Load



Source-drain Diode Forward Characteristics

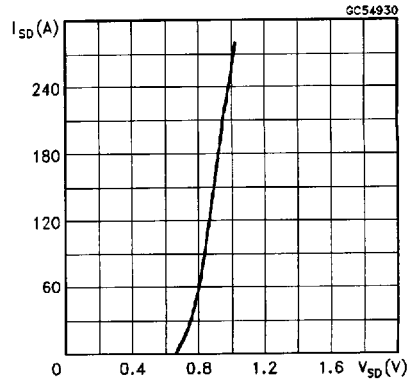


Fig. 2: Gate Charge Test Circuit

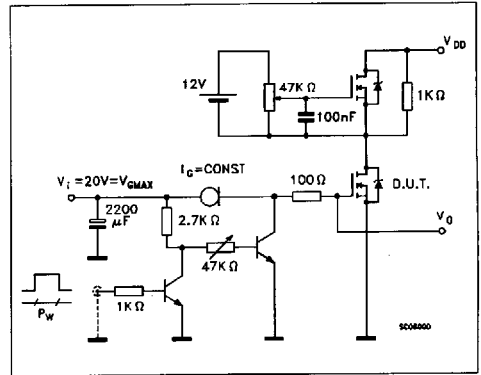


Fig. 3: Test Circuit For Inductive Load Switching And Diode Recovery Times

