



STE2001

65 X 128 SINGLE CHIP LCD CONTROLLER / DRIVER

PRODUCT PREVIEW

- 65 x 128 bits Display Data RAM
- Configurable matrix: 65 x 128 or 33 x 128
- Programmable (65/33) MUX rate
- Row by Row Scrolling
- Automatic data RAM Blanking procedure
- Selectable Input Interface:
 - I²C Bus Fast and Hs-mode (read and write)
 - Parallel Interface (write only)
 - Serial Interface (write only)
- Fully Integrated Oscillator requires no external components
- Fully Integrated Configurable LCD bias voltages generator with:
 - Selectable (5X, 4X, 3X, 2X) multiplication factor
 - Effective sensing for High Precision Output
 - Four selectable temperature compensation coefficients
- Designed for chip-on-glass (COG) applications
- Programmable bottom row pads mirroring and top row pads mirroring for compatible with both TCP and COG applications

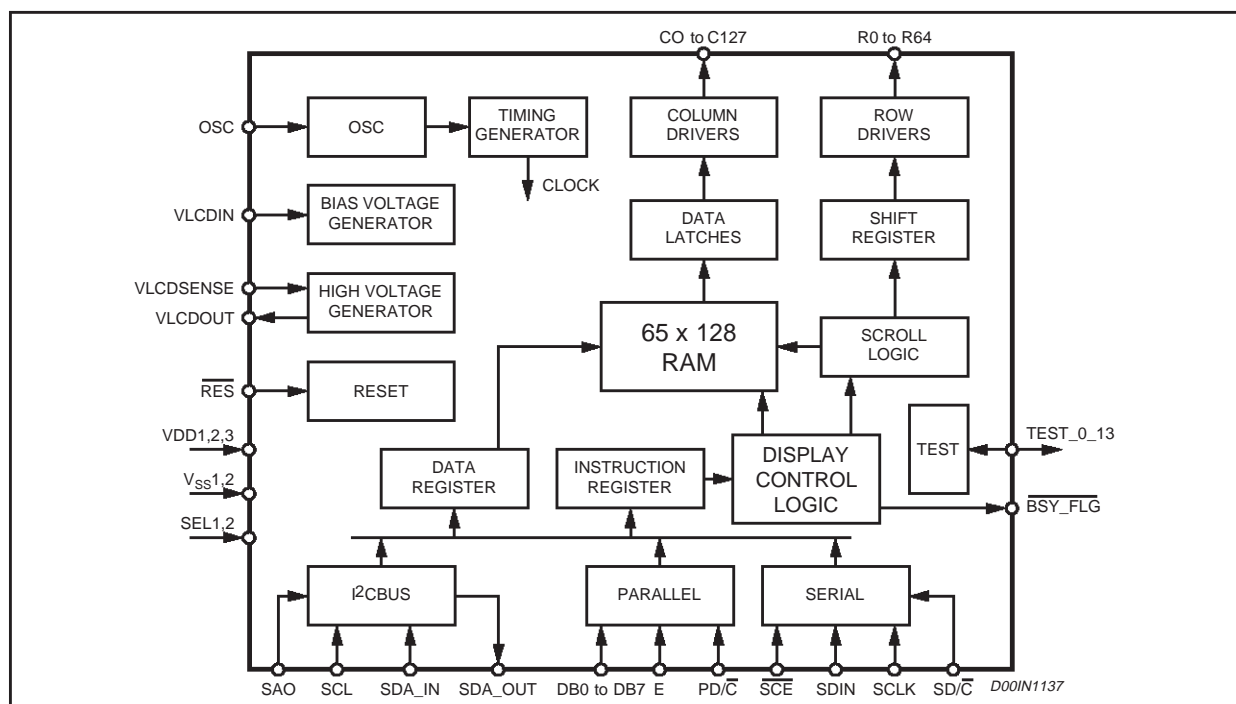
- Low Power Consumption, suitable for battery operated systems
- Logic Supply Voltage range from 1.9 to 5V
- High Voltage Generator Supply Voltage range from 2.4 to 4.5V
- Display Supply Voltage range from 4.5 to 9V

DESCRIPTION

The STE2001 is a low power CMOS LCD controller driver. Designed to drive a 65 rows by 128 columns graphic display, provides all necessary functions in a single chip, including on-chip LCD supply and bias voltages generators, resulting in a minimum of external components and in a very low power consumption. The STE2001 features three standard interfaces (Serial, parallel, I²C) for ease of interfacing with the host μ controller.

| Type | Ordering Number |
|----------------------------|-----------------|
| Bumped Wafers | STE2001DIE1 |
| Bumped Dice on Waffle Pack | STE2001DIE2 |

Figure 1. Block Diagram



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This is preliminary information on a new product now in development. Details are subject to change without notice.

STE2001**PIN DESCRIPTION**

| N° | Pad | Type | Function |
|---------------------------------|---|--------|---|
| R0 to R64 | 1 to 16 145 to 177 257 to 272 | O | LCD Row Driver Output |
| C0 to C127 | 17 to 144 | O | LCD Column Driver Output |
| VSS1,2 | 227 to 238 | GND | Ground pads. VSS1 is GND for VDD1, VSS2 for VDD2 and VDD3 |
| VDD1 | 186 to 191 | Supply | IC Positive Power Supply |
| VDD2,3 | 192 to 201 | Supply | Internal Generator Supply Voltages. |
| VLCDIN | 246 to 251 | Supply | LCD Supply Voltages for the Column and Row Output Drivers. |
| VLCDOUT | 239 to 244 | Supply | Voltage Multiplier Output |
| VLCDSENSE | 245 | Supply | Voltage Multiplier Regulation Input. V _{LCDOUT} Sensing for Output Voltage Fine Tuning |
| SEL1,2 | 183, 184 | I | Interface Mode Selection |
| SDA_IN | 223 | I | I ² C Bus Data In |
| SDA_OUT | 222 | O | I ² C Bus Data Out |
| SCL | 224 | I | I ² C bus Clock |
| SA0 | 225 | I | I ² C Slave Address LSB |
| OSC | 185 | I | External Oscillator Input |
| $\overline{\text{RES}}$ | 221 | I | Reset Input. Active Low. |
| DB0 to DB7 | 211 to 218 | I | Parallel Interface 8 Bit Data Bus |
| E | 220 | I | Parallel Interface Data Latch Signal. Data are Latched on the Falling EDGE. |
| $\text{PD}/\overline{\text{C}}$ | 219 | I | Parallel Interface Data/Command Selector |
| SDIN | 207 | I | Serial Interface Data Input |
| SCLK | 210 | I | Serial Interface Clock |
| $\overline{\text{SCE}}$ | 209 | I | Serial Interface ENABLE. When Low the Incoming Data are Clocked In. |
| $\text{SD}/\overline{\text{C}}$ | 208 | I | Serial Interface Data/Command selection |
| $\overline{\text{BSYFLG}}$ | 206 | O | Active Procedure Flag. Notice if There is an ongoing Internal Operation. Active Low. |
| T1 to T13 | 178 to 181 202 to 205 226 252 to 256 | I/O | Test Pads. |

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|--------------------|---|----------------------------------|------|
| V _{DD1} | Supply Voltage Range | - 0.5 to + 6.5 | V |
| V _{DD2,3} | Supply Voltage Range | - 0.5 to + 5 | V |
| V _{LCD} | LCD Supply Voltage Range | - 0.5 to + 10 | V |
| I _{SS} | Supply Current | - 50 to +50 | mA |
| V _i | Input Voltage (all input pads) | -0.5 to V _{DD2,3} + 0.5 | V |
| I _{in} | DC Input Current | - 10 to + 10 | mA |
| I _{out} | DC Output Current | - 10 to + 10 | mA |
| P _{tot} | Total Power Dissipation (T _j = 85°C) | 300 | mW |
| P _o | Power Dissipation per Output | 30 | mW |
| T _j | Operating Junction Temperature | -40 to + 85 | °C |
| T _{stg} | Storage Temperature | - 65 to 150 | °C |

ELECTRICAL CHARACTERISTICS

DC OPERATION

(V_{DD1} = 1.9 to V_{DD2,3} + 0.5V; V_{DD2,3} = 2.4 to 4.5 V; V_{SS1,2} = 0V; V_{LCD} = 4.5 to 9V; T_{amb} = -40 to 85°C; unless otherwise specified)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|------------------------|----------------------------------|---|------|------|--------------------------|------|
| Supply Voltages | | | | | | |
| V _{DD1} | Supply Voltage | | 1.9 | | V _{DD2,3} + 0.5 | V |
| | | T _{amb} = -20 to 85°C | 1.8 | | V _{DD2,3} + 0.5 | V |
| V _{DD2,3} | Supply Voltage | LCD Voltage Internally generated | 2.4 | | 4.5 | V |
| V _{LCDIN} | LCD Supply Voltage | LCD Voltage Supplied externally | 4.5 | | 9 | V |
| V _{LCDOUT} | LCD Supply Voltage | Internally generated; note 1 | 4.5 | | 9 | V |
| I(V _{DD1}) | Supply Current | V _{DD} = 2.8V; V _{LCD} = 7.6V; 4x charge pump; f _{sclk} = 0; T _{amb} = 25°C; note 3. | | 8 | 15 | μA |
| I(V _{DD2,3}) | Voltage Generator Supply Current | with VOP = 0 and PRS = 0 with external V _{LCD} = 7.6V | | 10 | 15 | μA |
| | | V _{LCD} = 7.6V; V _{DD} = 2.8V; f _{sclk} = 0; T _{amb} = 25°C; no display load; 4x charge pump; note 3,6 F _{osc} = 0 | | 70 | 115 | μA |

STE2001**ELECTRICAL CHARACTERISTICS** (continued)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|------------------------------|--|--|------------------------|-------|-----------------------------|--------|
| I(V _{DD1,2,3}) | Total Supply Current | V _{LCD} = 7.6V; V _{DD} = 2.8V; 4x charge pump; f _{sclk} = 0; T _{amb} = 25°C; no display load; note 3,6 F _{osc} = 0 | | 80 | 125 | μA |
| I(V _{LDCIN}) | External LCD Supply Voltage Current | V _{DD} = 2.8V; V _{LCD} = 7.6V; no display load; f _{sclk} = 0; T _{amb} = 25°C; note 3. F _{osc} = 0 | | 15 | 25 | μA |
| Logic Inputs | | | | | | |
| V _{IL} | Logic LOW voltage level | V _{IN} = V _{ih} (t _p < 10μs) | V _{SS} | | 0.3 V _{DD} | V |
| V _{IH} | Logic HIGH Voltage Level | V _{IN} = V _{il} (t _p < 10μs) | 0.7 V _{DD} | | V _{DD2,3} + 0.5 | V |
| I _{in} | Input Current | V _{in} = V _{SS1} or V _{DD1} | -1 | | 1 | μA |
| Column and Row Driver | | | | | | |
| R _{row} | ROW Output Resistance | | | 12 | 20 | kohm |
| R _{col} | Column Output resistance | | | 12 | 20 | kohm |
| V _{col} | Column Bias voltage accuracy | No load | -100 | | 100 | mV |
| V _{row} | Row Bias voltage accuracy | | -100 | | 100 | mV |
| LCD Supply Voltage | | | | | | |
| V _{LCD} | LCD Supply Voltage accuracy; Internally generated | V _{DD} = 2.8V; V _{LCD} = 7.6V; f _{sclk} =0; T _{amb} =25 C; no display load; note 2, 3, 6 & 7 | -300 | | 300 | mV |
| TC | Temperature coefficient | 00 | | -550 | | PPM/°C |
| | | 01 | | -1350 | | PPM/°C |
| | | 10 | | -1650 | | PPM/°C |
| | | 11 | | -2650 | | PPM/°C |

Notes: 1. The maximum possible V_{LCD} voltage that can be generated is dependent on voltage, temperature and (display) load.

2. Internal clock

3. When f_{sclk} = 0 there is no interface clock.

4. Power-down mode. During power-down all static currents are switched-off.

5. If external V_{LCD}, the display load current is not transmitted to I_{DD}

6. Tolerance depends on the temperature; (typically zero at T_{amb} = 27°C), maximum tolerance values are measured at the temperature range limit.

7. For TC0 to TC3

AC OPERATION

(V_{DD1} = 1.9 to V_{DD2,3} + 0.5V; V_{DD2,3} = 2.4 to 4.5 V; V_{SS1,2} = 0V; V_{LCD} = 4.5 to 9V; T_{amb} = -40 to 85°C; unless otherwise specified)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|----------------------------|-------------------------------|-------------------------|------|------|------|------|
| INTERNAL OSCILLATOR | | | | | | |
| F _{OSC} | Internal Oscillator frequency | V _{DD} = 2.8V; | 20 | 38 | 70 | kHz |
| F _{EXT} | External Oscillator frequency | | 20 | 38 | 100 | kHz |

ELECTRICAL CHARACTERISTICS (continued)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|---------------------|------------------------------|--|------|------|------|------|
| F _{FRAME} | Frame frequency | fosc or fext = 38 kHz; note 1 | | 73 | | Hz |
| T _{VHRL} | V _{DD1} to RES Low | note 2 and 10; C _{VLCD} = 1μF | 0 | | 5 | ms |
| T _{W(RES)} | RES LOW pulse width | note 3 | 600 | | | ns |
| | Reset Pulse Rejection | T _{amb} = 25°C; note 11 | | 370 | | μs |
| | Reset Pulse Rejection | note 11 | | | 200 | μs |
| T _{START} | Reset Pulse vs. Device Ready | | 1 | | | ms |
| T _{VDD} | | | 0 | | | |

I²C BUS INTERFACE (See note 4)

| | | | | | | |
|---------------------|-----------------------|---|-----|-----|-----|-----|
| F _{SCL} | SCL Clock Frequency | Fast Mode ; V _{DD1} =4.5V | DC | | 400 | kHz |
| | | V _{DD1} =18V; T _{amb} = -20 to 70°C | | | 400 | kHz |
| | | High Speed Mode; C _b =100pF (max); note 6; V _{DD1} =4.5V | DC | 3.4 | | MHz |
| | | High Speed Mode; C _b =400pF (max); note 6 ; V _{DD1} =4.5V | DC | | 1.7 | MHz |
| T _{SCLL} | C _b =100pF | | 160 | | | ns |
| T _{SCLH} | C _b =100pF | | 160 | | | ns |
| T _{SCLL} | C _b =400pF | | 320 | | | ns |
| T _{SCLH} | C _b =400pF | | 320 | | | ns |
| T _{SU;DAT} | C _b =100pF | | | 30 | | ns |
| T _{HD;DAT} | C _b =100pF | | | 30 | | ns |
| T _{SU;DAT} | C _b =400pF | | | 30 | | ns |
| T _{HD;DAT} | C _b =400pF | | | 30 | | ns |
| T _{SU;STA} | C _b =100pF | Note 8 | | 170 | | ns |
| T _{SU;STA} | C _b =400pF | Note 8 | | 330 | | ns |
| T _{HD;STA} | C _b =100pF | Note 8 | | 170 | | ns |
| T _{HD;STA} | C _b =400pF | Note 8 | | 330 | | ns |
| T _{SU;STO} | C _b =100pF | Note 8 | | 170 | | ns |
| T _{SU;STO} | C _b =400pF | Note 8 | | 330 | | ns |
| T _{rCL} | C _b =100pF | Note 5, 8 | | 25 | | ns |
| T _{rCL} | C _b =400pF | Note 5, 8 | | 50 | | ns |
| T _{rCL1} | C _b =100pF | Note 5, 8 | | 30 | | ns |
| T _{rCL1} | C _b =400pF | Note 5, 8 | | 120 | | ns |
| T _{rDA} | C _b =100pF | Note 5, 8 | | 30 | | ns |
| T _{rDA} | C _b =400pF | Note 5, 8 | | 120 | | ns |
| T _{fCL} | C _b =100pF | Note 5, 8 | | 25 | | ns |
| T _{fCL} | C _b =400pF | Note 5, 8 | | 50 | | ns |

STE2001**ELECTRICAL CHARACTERISTICS** (continued)

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|------------------|---|----------------|------|------|------|------|
| T _{fDA} | C _b =100pF | | | 25 | | ns |
| T _{fDA} | C _b =400pF | | | 120 | | ns |
| C _b | Capacitive load for SDAH and SCLH | | 100 | | 400 | pF |
| C _b | Capacitive load for SDAH + SDA line and SCLH + SCL line | | | | 400 | pF |
| T _{SW} | | note 5 | | 10 | | ns |

PARALLEL INTERFACE

| | | | | | | |
|---------------------|---------------------|-------------------------------|-----|--|--|----|
| T _{CY(EN)} | Enable Cycle Time | V _{DD} = 4.5V; Write | 125 | | | ns |
| T _{W(EN)} | Enable Pulse width | V _{DD} = 4.5V; Write | 60 | | | ns |
| T _{SU(A)} | Address Set-up Time | V _{DD} = 4.5V; Write | 30 | | | ns |
| T _{H(A)} | Address Hold Time | V _{DD} = 4.5V; Write | 50 | | | ns |
| T _{SU(D)} | Data Set-Up Time | V _{DD} = 4.5V; Write | 30 | | | ns |
| T _{H(D)} | Data Hold Time | V _{DD} = 4.5V; Write | 50 | | | ns |

SERIAL INTERFACE

| | | | | | | |
|-------------------|------------------------------------|-------------------------|-----|--|---|-----|
| F _{SCLK} | Clock Frequency | V _{DD} = 4.5V | | | 8 | MHz |
| | | V _{DD1} = 1.8V | | | 5 | MHz |
| T _{CYC} | Clock Cycle SCLK | V _{DD} = 4.5V | 125 | | | ns |
| T _{PWH1} | SCLK pulse width HIGH | V _{DD} = 4.5V | 70 | | | ns |
| T _{PWL1} | SCLK Pulse width LOW | V _{DD} = 4.5V | 70 | | | ns |
| T _{S2} | \overline{SCE} setup time | | 50 | | | ns |
| T _{H2} | \overline{SCE} hold time | | 50 | | | ns |
| T _{PWH2} | \overline{SCE} minimum high time | | 60 | | | ns |
| T _{H5} | \overline{SCE} start hold time | Note 8 | 60 | | | ns |
| T _{S3} | SD/ \overline{C} setup time | | 60 | | | ns |
| T _{H3} | SD/ \overline{C} hold time | | 40 | | | ns |
| T _{S4} | SDIN setup time | | 40 | | | ns |
| T _{H4} | SDIN hold time | | 40 | | | ns |

Notes: 1. $F_{\text{frame}} = \frac{f_{\text{osc}}}{520}$

- \overline{RES} may be LOW or HIGH before V_{DD1} goes HIGH.
- If T_{w(RES)} is longer than 500ns (typical) a reset may be generated.
- All timing values are valid within the operating supply voltage and ambient temperature ranges and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}
- The rise and fall times specified here refer to the driver device and are part of general HS-mode specification.
- The device inputs SDA and SCL are filtered and will reject any spike on the bus-lines of with T_{SW}
- C_b is the capacitive load for each bus line.
- T_{H5} is the time from the previous SCLK positive edge to the negative edge of \overline{SCE}
- For bus line loads C_b between 100 and 400pF the timing parameters must be linearly interpolated
- C_{VLCD} is the filtering capacitor on VLCDOUT
- If T_{w(RES)} is shorter than max. value a reset pulse is rejected.

CIRCUIT DESCRIPTION

Supplies Voltages and Grounds

V_{DD2} and V_{DD3} are supply voltages to the internal voltage generator (see below). They must be externally connected. If the internal voltage generator is not used, these should be connected to V_{DD1} pad. V_{DD1} supplies the rest of the IC. This supply voltage could be different from V_{DD2} and V_{DD3} . V_{DD1} must be lower than $V_{DD2,3} + 0.5V$.

Internal Supply Voltage Generator

The IC has a fully integrated (no external capacitors required) charge pump for the Liquid Crystal Display supply voltage generation. The multiplying factor can be programmed to be: X5; X4; X3; X2, using the 'set CP Multiplication' Command. The output voltage (V_{LCDOUT}) is tightly controlled through the $V_{LCDSense}$ pad. For this voltage, four different temperature coefficients (TC, rate of change with temperature) can be programmed using the bits TC1 and TC0. This will ensure no contrast degradation over the LCD operating range. Using the internal charge pump, the V_{CDIN} and V_{LCDOUT} pads must be connected together. An external supply could be connected to V_{CDIN} to supply the LCD without using the internal generator. In such event the V_{LCDOUT} and $V_{LCDSense}$ must be connected to GND and the internal voltage generator must be programmed to zero (PRS = 0, Vop = 0 - Reset condition).

Oscillator

A fully integrated oscillator (requires no external components) is present to provide the clock for the Display System. When used the OSC pad must be connected to VDD1 pad. An external oscillator could be used and fed into the OSC pin.

Display Data RAM

The STE2001, provides an 65X128 bits Static RAM to store Display data. This is organized into 8 (Bank0 to Bank7) banks with 128 Bytes and one Bank (Bank8) with 128 Bits to be used for icons. RAM access is accomplished in either one of the Bus Interfaces provided (see below). Allowed addresses are X0 to X127 (Horizontal) and Y0 to Y8 (Vertical). When writing to RAM, four addressing mode are provided:

- Normal Horizontal (MX = 0 and V = 0), having the column with address X = 0 located on the left of the memory map. The X pointer is increased after each byte written. After the last column address (X = 127), Y address pointer is modified to jump to next row. X restarts from X = 0 (Fig.2).
- Normal Vertical (MX = 0 and V = 1), having the column with address X = 0 located on the left of the memory map. The Y pointer is increased after each byte written. After the last row address (Y = 8), the X pointer is modified to jump to next column and Y restarting from Y = 0. (Fig. 3).
- Mirrored Horizontal (MX = 1 and V = 0), having the column with address X = 0 located on the right of the memory map. The X pointer is increased after each byte written. After the last column address (X = 127), Y address pointer is modified to jump to next row. X restarts from X = 0 (fig. 4).
- Mirrored Vertical (MX = 1 and V = 1), having the column with address X = 0 located on the right of the memory map. The Y pointer is increased after each byte written. After the last row address (Y = 8), the X pointer is modified to jump to next column and Y restarting from Y = 0. (Fig. 5).

After the last allowed address (X;Y) = (128;8), the address pointers always jump to the cell with address (X;Y) = (0;0). Data bytes in the memory could have the MSB either on top (D0 = 0, Fig. 6) or on the bottom (D0 = 1, Fig. 7).

Mux 65 Mode

The STE2001 provides also means to alter the normal output addressing. A mirroring of the Display along the X axis is enabled setting to a logic one the MY bit. This function is achieved reading the matrix from physical row 63 to 0, since the relation between the physical memory rows and the output row drivers is only dependent on the memory reading sequence (1st row read output on R0, 2nd on R1... last on R65). This function doesn't affect the content of the memory map. It is only related to the visualization process (Fig. 8 & Fig. 9).

It is also possible to modify the way with which row drivers are connected with DDRAM memory. A flip along y-axis of each sub-block can be applied on both the Row Pads located on the Interface Side (the edge of the chip where the Interface Pads are located), setting the TRS bit to a logic one, and on the Row Pads located on the other edge, setting the BRS bit to a logic one.

Figure 2 Automatic data RAM writing sequence with V=0 and Data RAM Normal Format (MX=0) Figure 3 Automatic data RAM writing sequence with V=1 and Data RAM Normal Format (MX=0)



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Figure 2. Automatic data RAM writing sequence with V=0 and Data RAM Normal Format (MX=0)

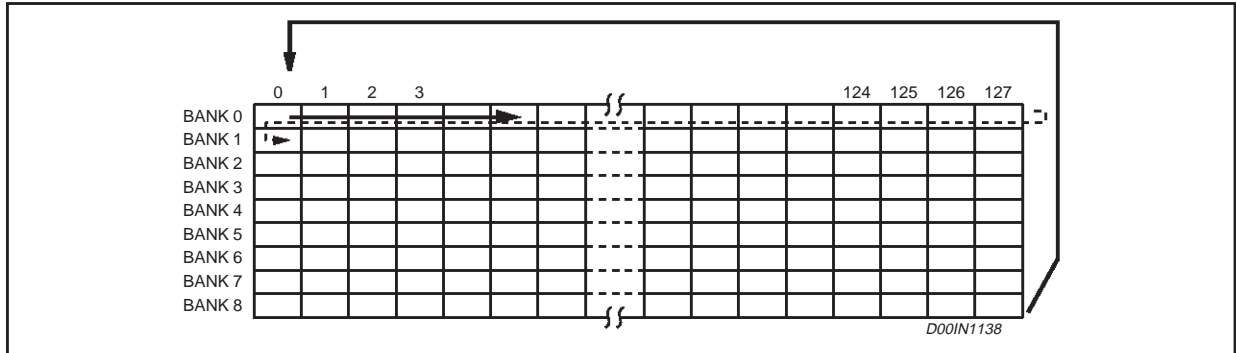


Figure 3. Automatic data RAM writing sequence with V=1 and Data RAM Normal Format (MX=0)

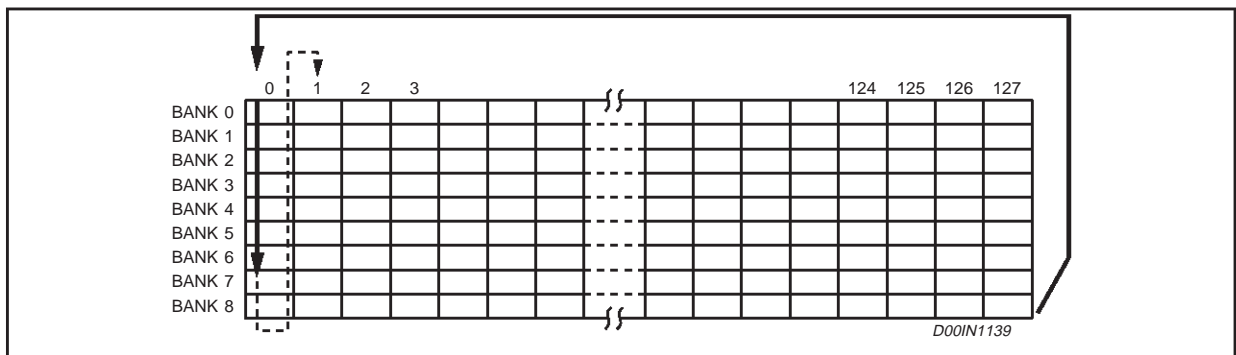


Figure 4. Automatic data RAM writing sequence with V=0 and Data RAM Mirrored Format (MX=1)

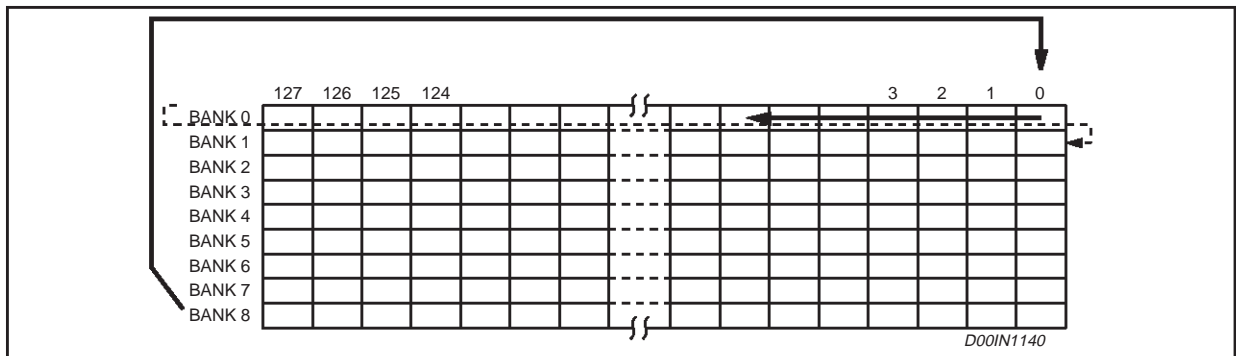


Figure 5. Automatic data RAM writing sequence with V=1 and Data RAM Mirrored Format (MX=1)

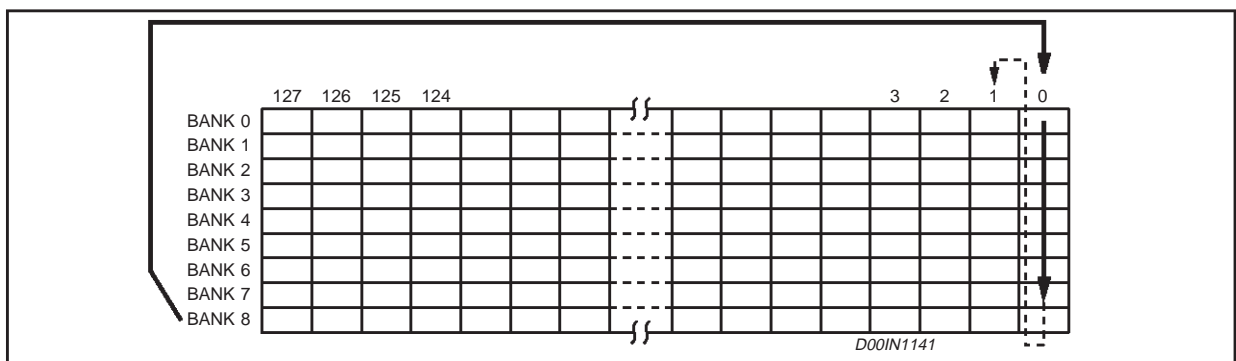


Figure 6. Data RAM Byte organization with D0 = 0

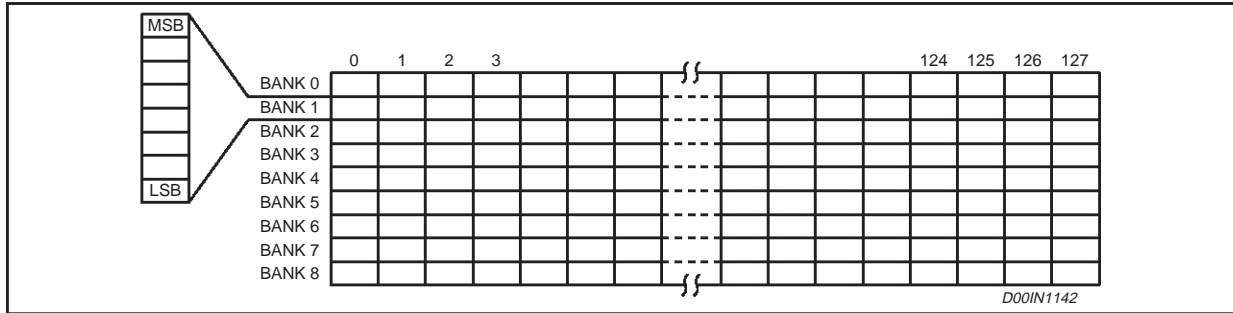


Figure 7. Data RAM Byte organization with D0 = 1

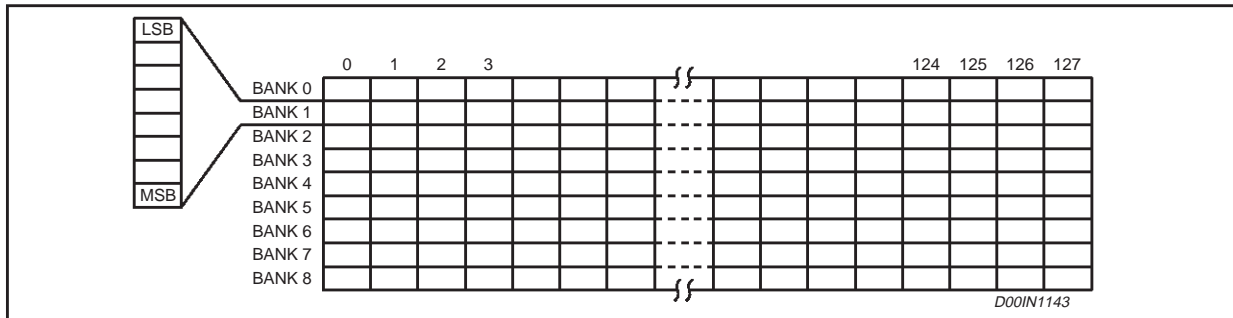


Figure 8. Output drivers rows and physical memory rows correspondence with MY = 0

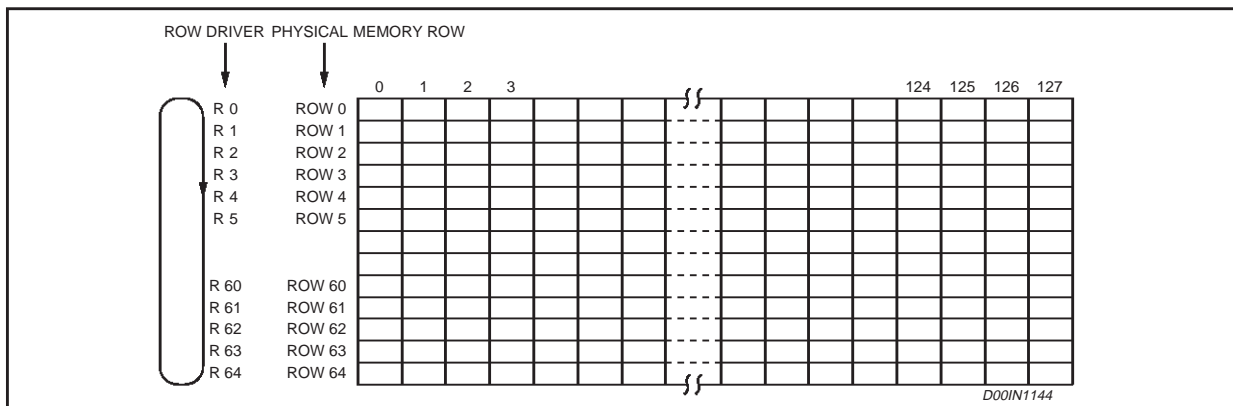
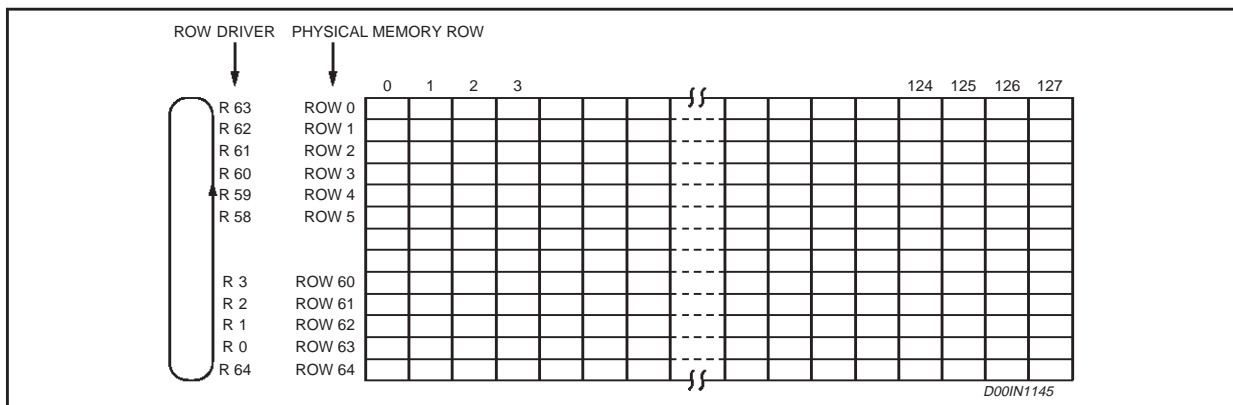


Figure 9. Output drivers rows and physical memory rows correspondence with MY = 1



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MUX 33 Mode

When using the 1:33 MUX ratio (MUX bit Set), the memory map is changed so that the only "active" row drivers are the ones related to Bank4 to Bank7.

When writing data RAM, as for Mux 65, four addressing mode are provided. The memory matrix is written as in mux 65 mode so the user must take care of updating X and Y pointers to fill the memory matrix in the correct way.

In MUX 33 mode only the MUX 33 memory logic matrix is read. The MY bit control the reading process. If MY is set to a logic zero the row reading sequence is 0-1-2.....33 (fig.11). If MY is set to a logic one the reading sequence is 32....1-33 (Fig 12).

The icon row (BANK8) is always the last being output either MY bit is a logic one or zero.

The functions related to bit TRS is the same as in MUX 65 mode.

In fig. 11 is shown the output drivers pad connection for MUX 33 mode. Note that the unused BANK 0-3 row drivers become columns drivers.

If a 33x128 LCD matrix is driven, the output row drivers R0-R15 and R32-R47 must be floating.

Figure 10. Physical 65x128 memory matrix and 33x128 correspondence

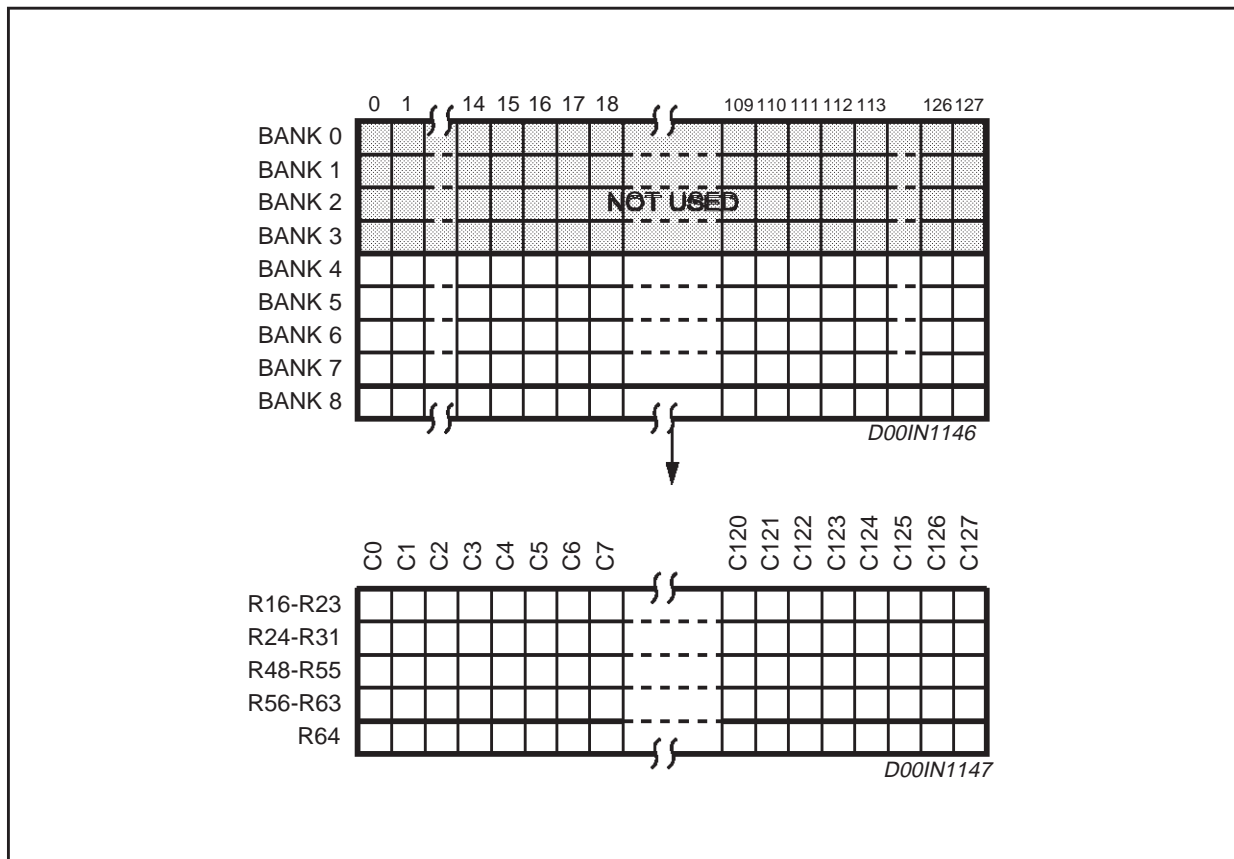


Figure 11. Output drivers rows and logical memory rows correspondence with MY = 0

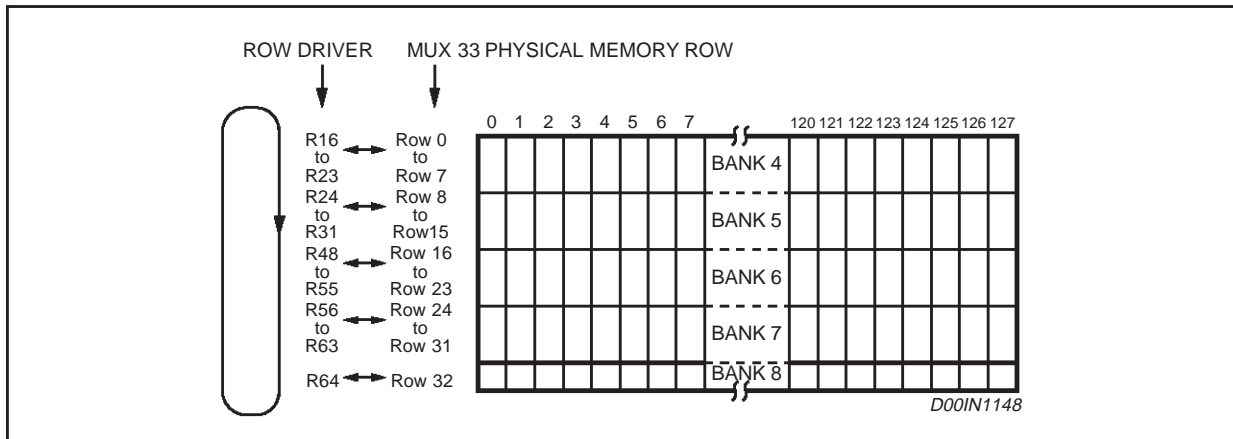
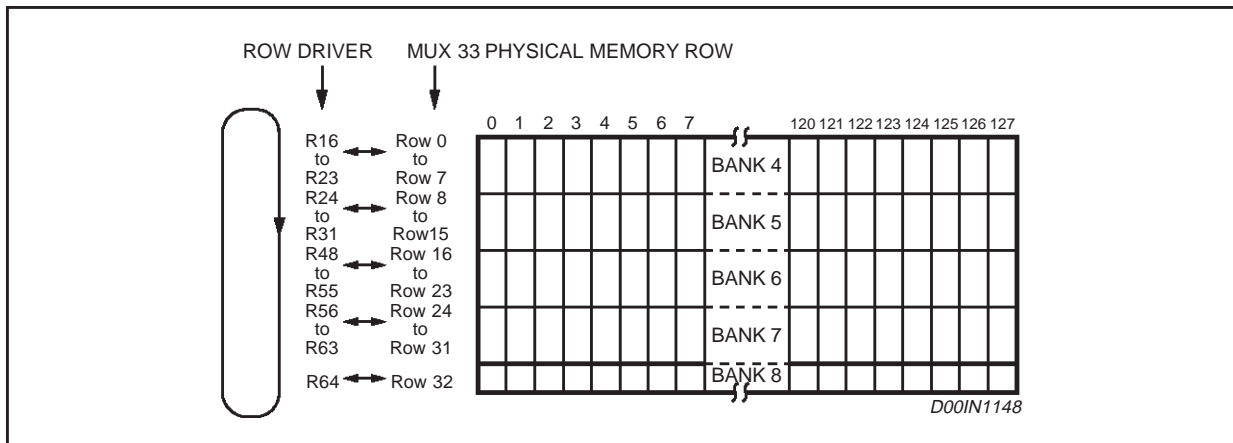


Figure 12. Output drivers rows and logical memory rows correspondence with MY = 1



Instruction Set

Two different instructions formats are provided:

- With D/\overline{C} set to LOW

commands are sent to the Control circuitry.

- With D/\overline{C} set to HIGH

the Data RAM is addressed Instructions have the syntax summarized in Table.1.

Reset (RES)

At power-on, all internal registers and RAM content are not defined. A Reset pulse must be applied on RES pad (active low) to initialize the internal registers content (see Tables 3,4,5,&6). Every on-going communication with the host controller is interrupted. The IC after the reset pulse is programmed in Power Down mode.

The Default configurations is:

- Horizontal addressing ($V = 0$)
- Normal instruction set ($H = 0$)
- Normal display ($MX = MY = TRS = BRS = 0$)
- MUX 65 mode ($MUX = 0$)

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- Display blank (E = D = 0)
- Address counter X[6: 0] = 0 and Y[3 : 0] = 0
- Temperature coefficient (TC[1 : 0] = 0)
- Bias system (BS[2 : 0] = 0)
- V_{OP} = 0
- Power Down (PD = 1)

To clear the RAM content a MEMORY BLANK instruction should be executed.

Power Down (PD = 1)

When at Power Down, all LCD outputs are kept at V_{SS} (display off). Bias generator and V_{LCD} generator are OFF (V_{LCDOUT} output is discharged to V_{SS}, and then is possible to disconnect V_{LCDOUT}). The internal Oscillator is in off state. An external clock can be provided. The RAM contents is not cleared.

Charge Pump Factor

The desired Charge Pump Multiplication Factor can be programmed though the S1 and S0 bits, as follows:

| S1 | S0 | Multiplication Factor |
|----|----|-----------------------|
| 0 | 0 | 2X |
| 0 | 1 | 3X |
| 1 | 0 | 4X |
| 1 | 1 | 5X |

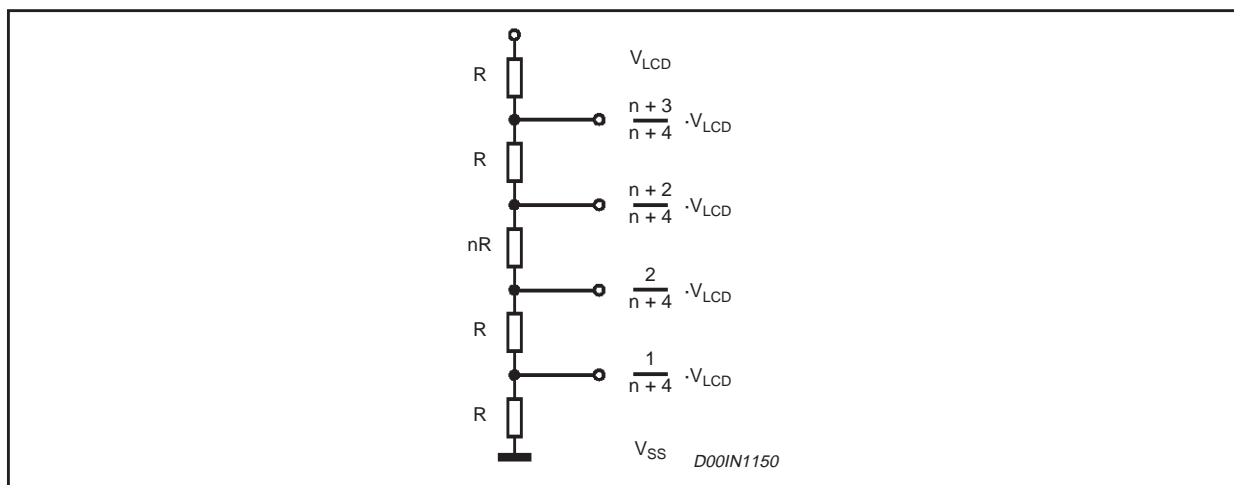
At Reset the X2 factor is selected.

Bias Levels

To properly drive the LCD, six (Including VLCD and VSS) different voltage (Bias) levels are generated. The ratios among these levels and VLCD, should be selected according to the MUX ratio (m). They are established to be (Fig. 14):

$$V_{LCD}, \frac{n+3}{n+4} V_{LCD}, \frac{n+2}{n+4} V_{LCD}, \frac{2}{n+4} V_{LCD}, \frac{1}{n+4} V_{LCD}, V_{SS}$$

Figure 13. Bias level Generator



thus providing an $1/(n+4)$ ratio, with n calculated from:

$$n = \sqrt{m} - 3$$

For m = 65, n = 5 and an 1/9 ratio is set.

For m = 33, n = 3 and an 1/7 ratio is set.

The STE2001 provides three bits (BS0, BS1, BS2) for programming the desired Bias Ratio as shown below:

| BS2 | BS1 | BS0 | n |
|-----|-----|-----|---|
| 0 | 0 | 0 | 7 |
| 0 | 0 | 1 | 6 |
| 0 | 1 | 0 | 5 |
| 0 | 1 | 1 | 4 |
| 1 | 0 | 0 | 3 |
| 1 | 0 | 1 | 2 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

The following table Bias Level for m = 65 and m = 33 are provided:

| Symbol | m = 65 (1/9) | m = 33 (1/7) |
|--------|---------------------|---------------------|
| V1 | V_{LCD} | V_{LCD} |
| V2 | $8/9 \cdot V_{LCD}$ | $6/7 \cdot V_{LCD}$ |
| V3 | $7/9 \cdot V_{LCD}$ | $5/7 \cdot V_{LCD}$ |
| V4 | $2/9 \cdot V_{LCD}$ | $2/7 \cdot V_{LCD}$ |
| V5 | $1/9 \cdot V_{LCD}$ | $1/7 \cdot V_{LCD}$ |
| V6 | V_{SS} | V_{SS} |

LCD Voltage Generation

The LCD Voltage at reference temperature ($T_0 = 35^\circ\text{C}$) can be set using the VOP register content according to the following formula:

$$V_{LCD}(T=T_0) = V_{LCD0} = (A_i + V_{OP} \cdot B) \quad (i=0,1)$$

with the following values:

| Symbol | Value | Unit | Note |
|----------------|-------|------|---------|
| A ₀ | 2.90 | V | PRS = 0 |
| A ₁ | 6.91 | V | PRS = 1 |
| B | 0.034 | V | |
| T ₀ | 35 | °C | |

Note that the two PRS value produces two adjacent ranges for VLCD. If the register and PRS bit are set to zero

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the internal voltage generator is switched off.

The proper value for the VLCD is a function of the Liquid Crystal Threshold Voltage (V_{th}) and of the Multiplexing Rate. A general expression for this is:

$$V_{LCD} = \frac{1 + \sqrt{m}}{\sqrt{2 \cdot \left(1 - \frac{1}{\sqrt{m}}\right)}} \cdot V_{th}$$

For MUX Rate $m = 65$ the ideal V_{LCD} is:

$$V_{LCD(to)} = 6.85 \cdot V_{th}$$

than:

$$V_{op} = \frac{(6.85 \cdot V_{th} - A_i)}{0.03}$$

Temperature Coefficient

As the viscosity, and therefore the contrast, of the LCD are subject to change with temperature, there's the need to vary the LCD Voltage with temperature. The STE2001 provides the possibility to change the VLCD in a linear fashion against temperature with four different Temperature Coefficient selectable through the TC0 and TC1 bits.

| TC1 | TC0 | Value | Unit |
|-----|-----|-------|--------|
| 0 | 0 | -550 | PPM/°C |
| 0 | 1 | -1350 | PPM/°C |
| 1 | 0 | -1650 | PPM/°C |
| 1 | 1 | -2650 | PPM/°C |

Figure 14. VLCD Slopes Cross Point with Different TC

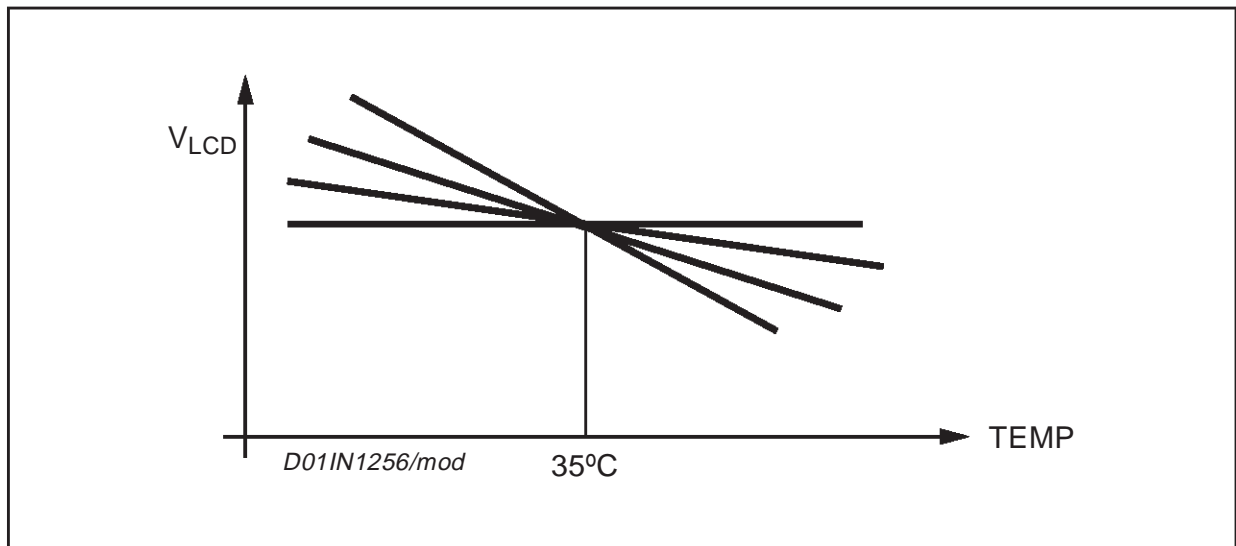
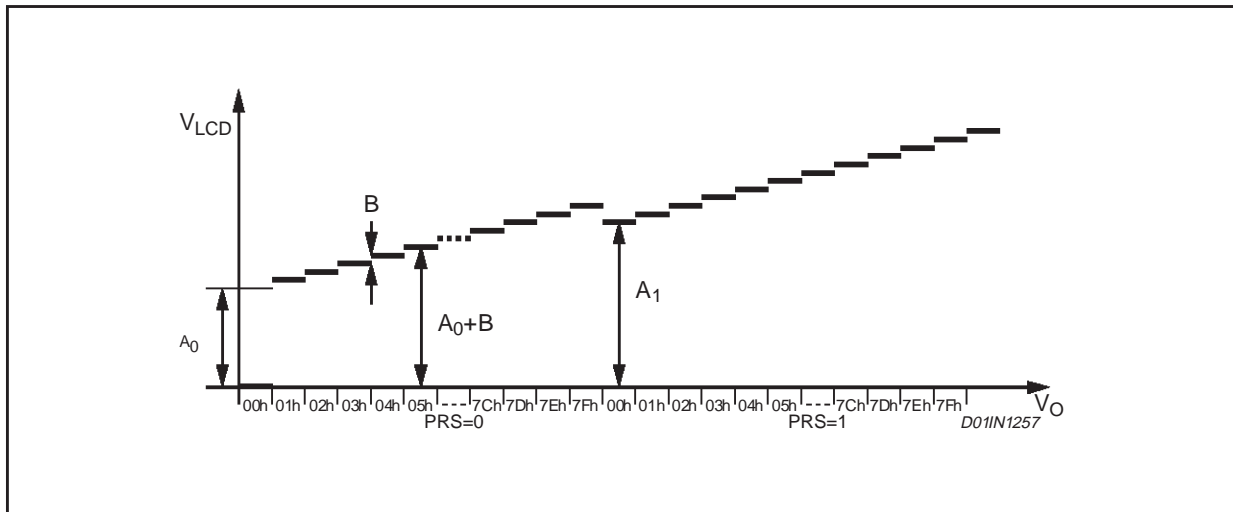


Figure 15.



Finally, the V_{LCD} voltage at a given (T) temperature can be calculated as:

$$V_{LCD}(T) = V_{LCD0} \cdot [1 + (T - T_0) \cdot TC]$$

Memory Blanking Procedure

This instruction allows to fill the memory with "blank" patterns, in order to delete patterns randomly generated in memory when starting up the device. This instruction substitutes (128X9) single "write" instructions. It is possible to program "Memory Blanking Procedure" only under the following conditions:

- X address = 0
- Y address = 0
- V bit = 0
- PD bit = 0
- MX bit = 0

The end of the procedure will be notified on the $\overline{BSY_FLG}$ pad going HIGH (while LOW the procedure is running). Any instruction programmed with $\overline{BSY_FLG}$ LOW will be ignored that is, no instruction can be programmed for a period equivalent to 128X9 internal write cycles (128X9X1/fclock). The start of Memory blanking procedure will be between one and two fclock cycles from the last active edge (E rising edge for the parallel interface, last SCLK rising edge for the Serial interface, last SCL rising edge for the I^2C interface).

Checker Board Procedure

This instruction allows to fill the memory with "checker-board" pattern. It is mainly intended to developers, who can now simply obtain complex module test configuration by means of a single instruction. It is possible to program "Checker Board Procedure" only under the following conditions:

- X address = 0
- Y address = 0
- V bit = 0
- PD bit = 0
- MX bit = 0

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The end of the procedure will be notified on the BSY_FLG pad going HIGH, while LOW the procedure is running. Any instruction programmed with BSY_FLG LOW will be ignored, that is, no instruction can be programmed for a period equivalent to 128X9 internal write cycles (128X9X1/fdock). The start of Memory blanking procedure will be between one and two fclock cycles from the last active edge (E rising edge for the parallel interface, last SCLK rising edge for the Serial interface, last SCL rising edge for the I²C interface).

Scroll

The STE2001 can scroll the graphics display in units of raster-rows. The scrolling function is achieved changing the correspondence between the rows of the logical memory map and the output row drivers. The scroll function doesn't affect the data ram content. It is only related to the visualization process. The information output on the drivers is related to the row reading sequence (the 1st row read is output on R0, the 2nd on R1 and so on). Scrolling means reading the matrix starting from a row that is sequentially increased or decreased. After every scrolling command the offset between the memory address and the memory scanning pointer is increased or decreased by one. The offset range is between 0 to 63 in mux 65 mode and 0-31 in mux 33 mode. After the 64th scrolling command in mux 65 mode and after the 32th in mux 33 mode, the offset between the memory address and the memory scanning pointer is again zero (Cyclic Scrolling). Bank8 is always accessed last in each frame, and so isn't scrolled.

If the DIR Bit is set to a logic zero the offset register is increased by one and the raster is scrolled from top down. If the DIR Bit is set to a logic one the offset register is decreased by one and the raster is scrolled from bottom-up.

Bus Interfaces

To provide the widest flexibility and ease of use the STE2001 features three different methods for interfacing the host Controller. To select the desired interface the SEL1 and SEL2 pads need to be connected to a logic LOW (connect to GND) or a logic HIGH (connect to VDD). All the I/O pins of the unused interfaces must be connected to GND. If I/O pins voltage is lower than VDD interfaces could sink more current than expected.

All interfaces are working while the STE2001 is in Power Down.

| SEL2 | SEL1 | Interface | Note |
|------|------|------------------|--|
| 0 | 0 | I ² C | Read and Write; Fast and High Speed Mode |
| 0 | 1 | Serial | Write only |
| 1 | 1 | Parallel | Write only |
| 1 | 0 | Not Used | |

I²C Interface

The I²C interface is a fully complying I²C bus specification, selectable to work in both Fast (400kHz Clock) and High Speed Mode (3.4MHz).

This bus is intended for communication between different Ics. It consists of two lines: one bi-directional for data signals (SDA) and one for clock signals (SCL). Both the SDA and SCL lines must be connected to a positive supply voltage via an active or passive pull-up.

The following protocol has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

BUS not busy: Both data and clock lines remain High.

Start Data Transfer: A change in the state of the data line, from High to Low, while the clock is High, define the START condition.

Stop Data Transfer: A Change in the state of the data line, from low to High, while the clock signal is High, defines the STOP condition.

Data Valid: The state of the data line represents valid data when after a start condition, the data line is stable for the duration of the High period of the clock signal. The data on the line may be changed during the Low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a start condition and terminated with a stop condition. The number of data bytes transferred between the start and the stop conditions is not limited. The information is transmitted byte-wide and each receiver acknowledges with the ninth bit.

By definition, a device that gives out a message is called "transmitter", the receiving device that gets the signals is called "receiver". The device that controls the message is called "master". The devices that are controlled by the master are called "slaves"

Acknowledge. Each byte of eight bits is followed by one acknowledge bit. This acknowledge bit is a low level put on the bus by the receiver, whereas the master generates an extra acknowledge related clock pulse.

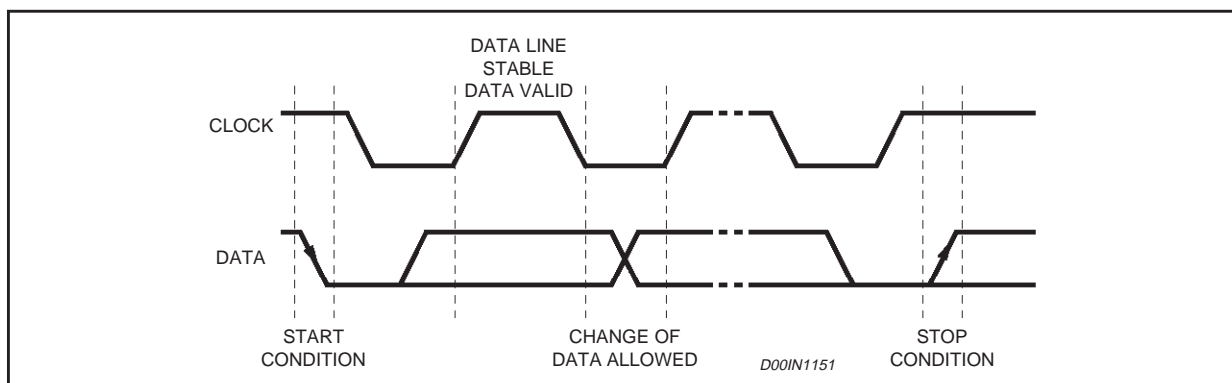
A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also, a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges has to pull down the SDA_IN line during the acknowledge clock pulse. Of course, setup and hold time must be taken into account. A master receiver must signal an end-of-data to the slave transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this case, the transmitter must leave the data line High to enable the master to generate the STOP condition.

Connecting SDA_IN and SDA_OUT together the SDA line become the standard data line. Having the acknowledge output (SDAOUT) separated from the serial data line is advantageous in Chip-On-Glass (COG) applications. In COG applications where the track resistance from the SDAOUT pad to the system SDA line can be significant, a potential divider is generated by the bus pull-up resistor and the Indium Tin Oxide (ITO) track resistance. It is possible that during the acknowledge cycle the STE2001 will not be able to create a valid logic 0 level. By splitting the SDA input from the output the device could be used in a mode that ignores the acknowledge bit. In COG applications where the acknowledge cycle is required, it is necessary to minimize the track resistance from the SDACK pad to the system SDA line to guarantee a valid LOW level.

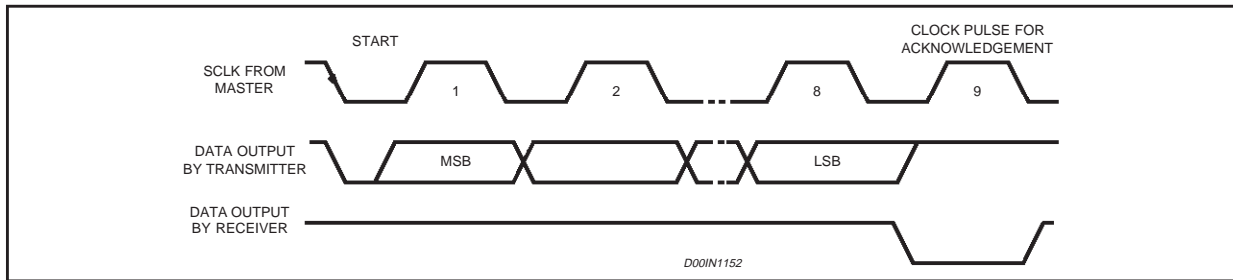
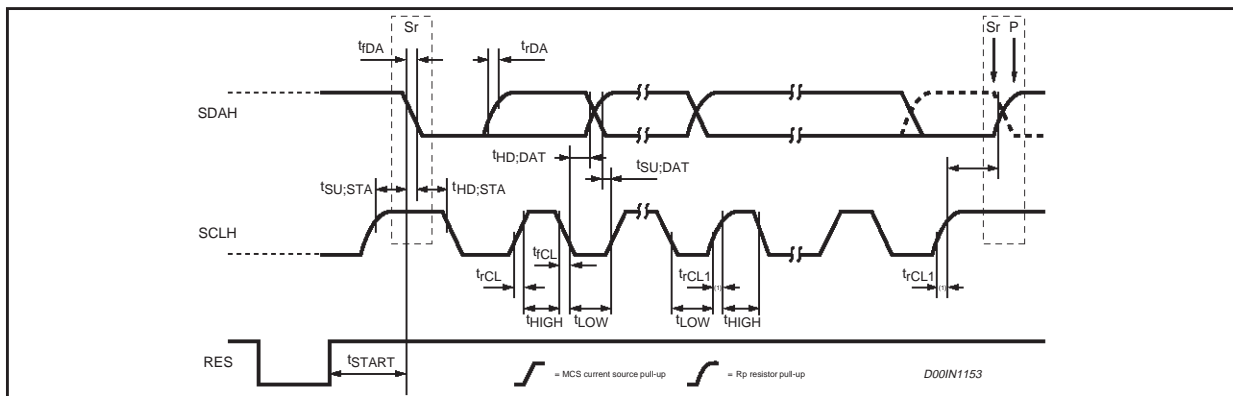
To be compliant with the I²C-bus Hs-mode specification the STE2001 is able to detect the special sequence "S00001xxx". After this sequence no acknowledge pulse is generated.

Since no internal modification are applied to work in Hs-mode, the device is able to work in Hs-mode without detecting the master code.

Figure 16. Bit transfer and START,STOP conditions definition



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Figure 17. Acknowledgment on the I²C-busFigure 18. I²C-bus timings

Communication Protocol

The STE2001 is an I²C slave. The access to the device is bi-directional since data write and status read are allowed. Two are the device addresses available for the device. Both have in common the first 6 bits (011110). The least significant bit of the slave address is set by connecting the SA0 input to a logic 0 or to a logic 1.

To start the communication between the bus master and the slave LCD driver, the master must initiate a START condition. Following this, the master sends an 8-bit byte, shown in Fig. 18, on the SDA bus line (Most significant bit first). This consists of the 7-bit Device select Code, and the 1-bit Read/Write Designator (R/W).

All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C-bus transfer.

Writing Mode.

If the R/W bit is set to logic 0 the STE2001 is set to be a receiver. After the slaves acknowledge one or more command word follows to define the status of the device.

A command word is composed by two bytes. The first is a control byte which defines the Co and D/C values, the second is a data byte (fig 18). The Co bit is the command MSB and defines if after this command will follow one data byte and another command word or if will follow a stream of data (Co = 1 Command word, Co = 0 Stream of data). The D/C bit defines whether the data byte is a command or RAM data (D/C = 1 RAM Data, D/C = 0 Command).

If Co = 1 and D/C = 0 the incoming data byte is decoded as a command, and if Co = 1 and D/C = 1, the following data byte will be stored in the data RAM at the location specified by the data pointer.

Every byte of a command word must be acknowledged by all addressed units.

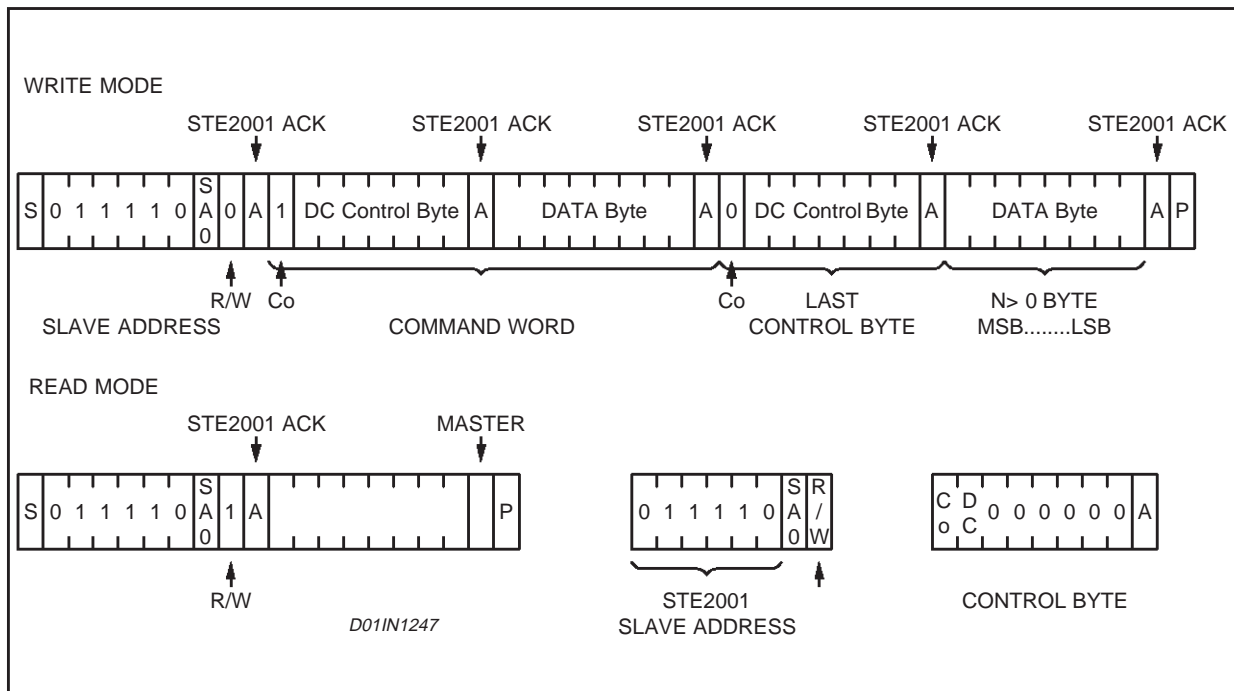
After the last control byte, if D/C is set to a logic 1 the incoming data bytes are stored inside the STE2001 Display RAM starting at the address specified by the data pointer. The data pointer is automatically updated after every byte written and in the end points to the last RAM location written.

Every byte must be acknowledged by all addressed units.

Reading Mode.

If the R/W bit is set to logic 1 the chip will output data immediately after the slave address. If the D/C bit sent during the last write access, is set to a logic 0, the byte read is the status byte.

Figure 19. communication protocol



SERIAL INTERFACE

The STE2001 serial Interface is a unidirectional link between the display driver and the application supervisor. It consists of four lines: one for data signals (SDIN), one for clock signals (SCLK), one for the peripheral enable (\overline{SCE}) and one for mode selection ($\overline{SD/C}$).

The serial interface is active only if the \overline{SCE} line is set to a logic 0. When \overline{SCE} line is high the serial peripheral power consumption is zero.

The STE2001 is always a slave on the bus and receive the communication clock on the SCLK pin from the master. The STE2001 is only able to receive data.

Information are exchanged byte-wide. During data transfer, the data line is sampled on the positive SCLK edge. While \overline{SCE} pin is high the serial interface is kept in reset.

$\overline{SD/C}$ line status indicates whether the byte is a command ($\overline{SD/C} = 0$) or RAM data ($\overline{SD/C} = 1$); it is read on the eighth SCLK clock pulse during every byte transfer.

If \overline{SCE} stays low after the last bit of a command/data byte, the serial interface expects the MSB of the next byte at the next SCLK positive edge.

A reset pulse on \overline{RES} pin interrupts the transmission. No data is written into the data RAM and all the internal registers are cleared.

If \overline{SCE} is low after the positive edge of \overline{RES} , the serial interface is ready to receive data.

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Figure 20. Serial bus protocol - one byte transmission

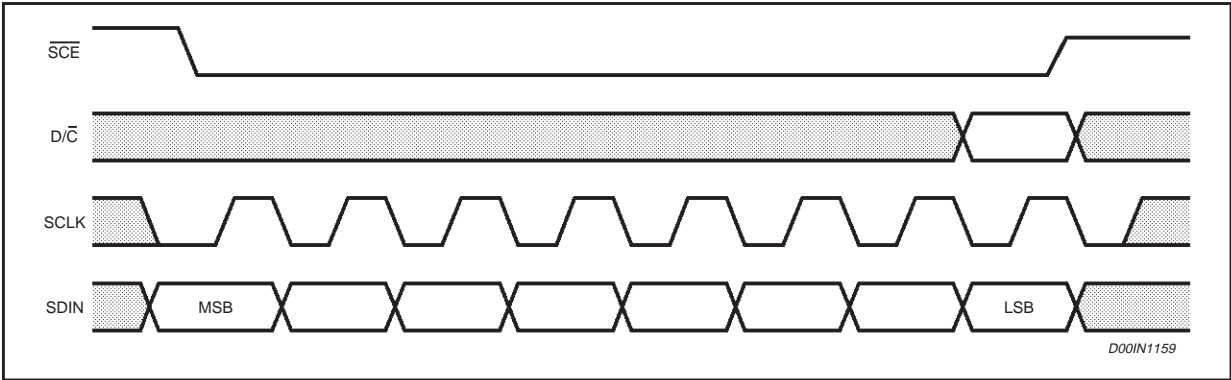


Figure 21. Serial bus protocol - several byte transmission

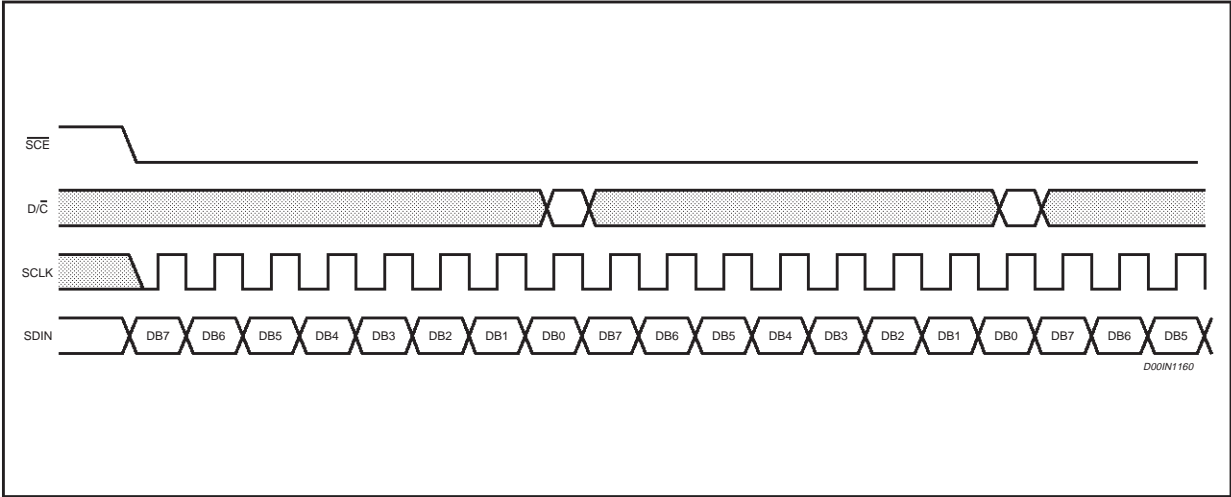
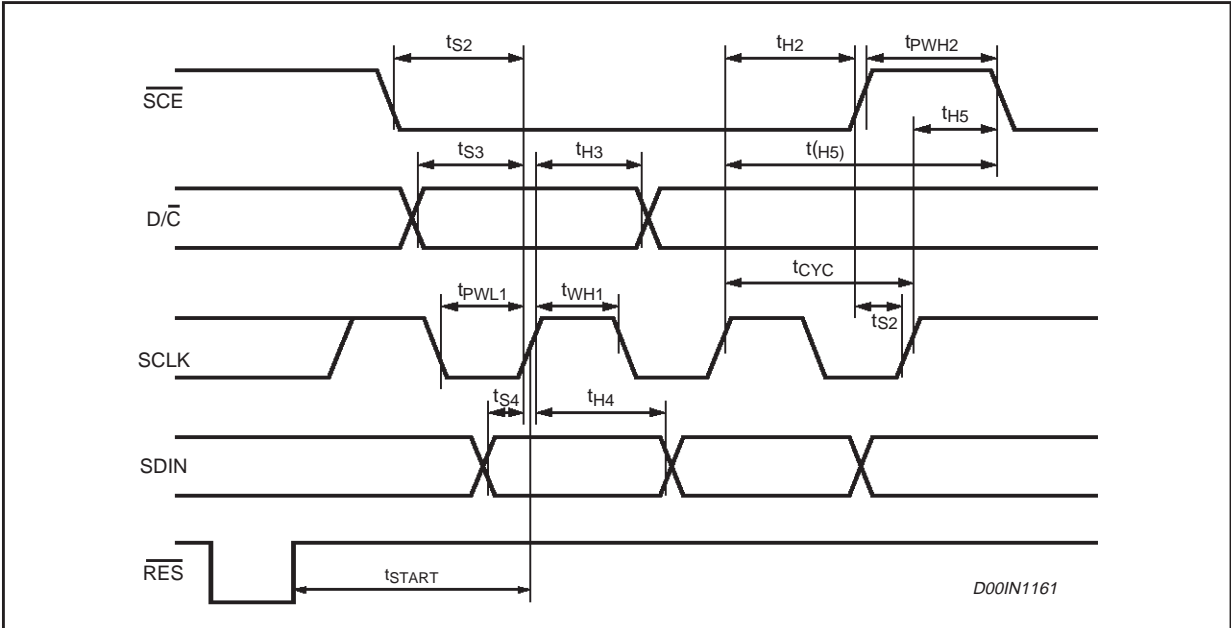


Figure 22. RESET effect on the serial interface



Parallel Interface

The STE2001 parallel Interface is a unidirectional link between the display driver and the application supervisor. It consists of ten lines: eight data lines (from DB7 to DB0) and two control lines. The control lines are: enable (E) for data latch and PD/C for mode selection.

The data lines and the control line values are internally latched on E rising edge (fig. 23).

Figure 23. Parallel interface timing

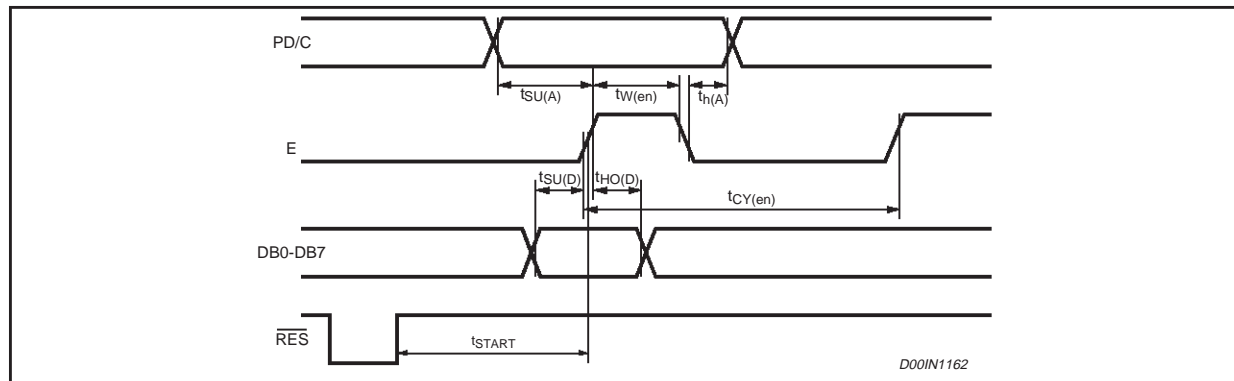


Table 1. Instruction Set

| Instruction | D/C | R/W | | | | | | | | | Description |
|--------------------------------|-----|-----|----|-----|-----|-----|-----|-----|-----|-----|---|
| | | | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | |
| H=0 or H=1 | | | | | | | | | | | |
| NOP | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | No Operation |
| Function Set | 0 | 0 | 0 | 0 | 1 | MX | MY | PD | V | H | Power Down Management; Entry Mode; Extended Instruction Set |
| Read Status Byte | 0 | 1 | PD | TRS | BRS | D | E | MX | MY | DO | (I ² C interface only) |
| Write Data | 1 | 0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Writes data to RAM |
| H=0 | | | | | | | | | | | |
| Memory Blank | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Starts Memory Blank Procedure |
| Scroll | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | DIR | Scrolls by one Row UP or DOWN |
| V _{LCD} Range Setting | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | PRS | V _{LDC} programming range selection |
| Display Control | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | 0 | E | Select Display Configuration |
| Set CP Factor | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | S1 | S0 | Charge Pump Multiplication Factor |
| Set RAM Y | 0 | 0 | 0 | 1 | 0 | 0 | Y3 | Y2 | Y1 | Y0 | Set Horizontal (Y) RAM Address |
| Set RAM X | 0 | 0 | 1 | X6 | X5 | X4 | X3 | X2 | X1 | X0 | Set Vertical (X) RAM Address |
| H=1 | | | | | | | | | | | |
| Checker Board | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Starts Checker Board Procedure |
| Multiplex Select | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | MUX | Selects MUX factor |
| TC Select | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | TC1 | TC0 | Set Temperature Coefficient for V _{LDC} |
| Output Address | 0 | 0 | 0 | 0 | 0 | 0 | 1 | DO | TRS | BRS | Set Row Order on Output Pads |
| Bias Ratios | 0 | 0 | 0 | 0 | 0 | 1 | 0 | BS2 | BS1 | BS0 | Set desired Bias Ratios |
| Reserved | 0 | 0 | 0 | 1 | X | X | X | X | X | X | Not to be used |
| Set V _{OP} | 0 | 0 | 1 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 | V _{OP} register Write instruction |

STE2001**Table 2. Explanations of Table 6 symbols**

| BIT | 0 | 1 | RESET STATE |
|-----|--|---|-------------|
| DIR | Scroll by one down | Scroll by one up | |
| H | Use basic instruction set | Use extended instruction set | 0 |
| PD | Device fully working | Device in power down | 1 |
| V | Horizontal addressing | Vertical addressing | 0 |
| MX | Normal X axis addressing | X axis address is mirrored. | 0 |
| MY | Image is displayed not vertically mirrored | Image is displayed vertically mirrored | 0 |
| TRS | No top rows mirroring | Top rows mirroring (row pads 16-31 & 48-64) | 0 |
| BRS | No bottom rows mirroring | Bottom rows mirroring (row pads 0-15 & 32-47) | 0 |
| DO | MSB on TOP | MSB on BOTTOM | 0 |
| PRS | V _{LCD} = 2.94V | V _{LCD} = 6.75V | 0 |
| MUX | 1:65 multiplexing ratio | 1:33 multiplexing ratio | 0 |

Table 3.

| D | E | DESCRIPTION | RESET STATE |
|---|---|-------------------------|-------------|
| 0 | 0 | display blank | D=0 E=0 |
| 1 | 0 | normal mode | |
| 0 | 1 | all display segments on | |
| 1 | 1 | inverse video mode | |

Table 4.

| S1 | S0 | DESCRIPTION | RESET STATE |
|----|----|--------------------------|-------------|
| 0 | 0 | Multiplication Factor 2X | 0 |
| 0 | 1 | Multiplication Factor 3X | |
| 1 | 0 | Multiplication Factor 4X | |
| 1 | 1 | Multiplication Factor 5X | |

Table 5.

| TC1 | TC0 | DESCRIPTION | RESET STATE |
|-----|-----|--------------------------------|-------------|
| 0 | 0 | VLCD temperature Coefficient 0 | 00 |
| 0 | 1 | VLCD temperature Coefficient 1 | |
| 1 | 0 | VLCD temperature Coefficient 2 | |
| 1 | 1 | VLCD temperature Coefficient 3 | |

Table 6.

| BS2 | BS1 | BS0 | DESCRIPTION | RESET STATE |
|-----|-----|-----|-----------------------|-------------|
| 0 | 0 | 0 | Bias Ratio equal to 7 | 000 |
| 0 | 0 | 1 | Bias Ratio equal to 6 | |
| 0 | 1 | 0 | Bias Ratio equal to 5 | |
| 0 | 1 | 1 | Bias Ratio equal to 4 | |
| 1 | 0 | 0 | Bias Ratio equal to 3 | |
| 1 | 0 | 1 | Bias Ratio equal to 2 | |
| 1 | 1 | 0 | Bias Ratio equal to 1 | |
| 1 | 1 | 1 | Bias Ratio equal to 0 | |

Figure 24. Application Schematic Using an External LCD Voltage Generator

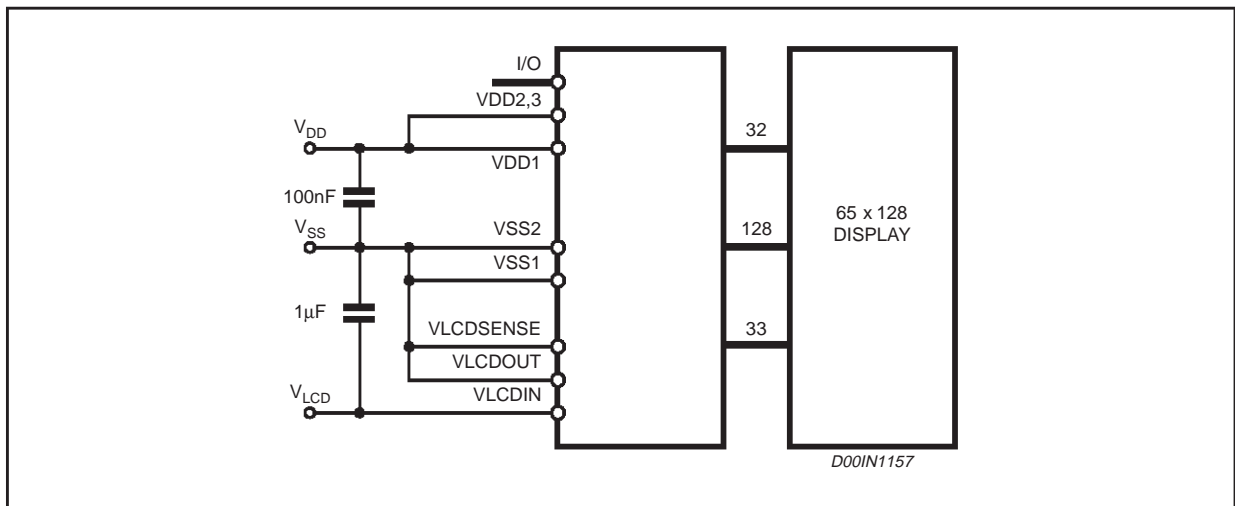
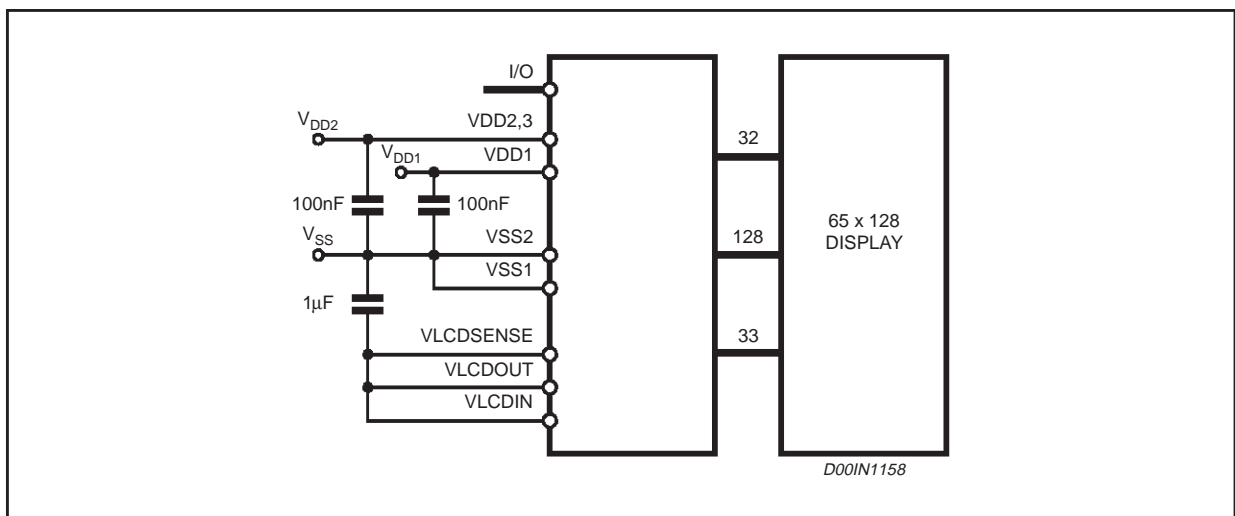


Figure 25. Application Schematic using the Internal LCD Voltage Generator and two separate supplies



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Figure 26. Application Schematic using the Internal LCD Voltage Generator and a single supply

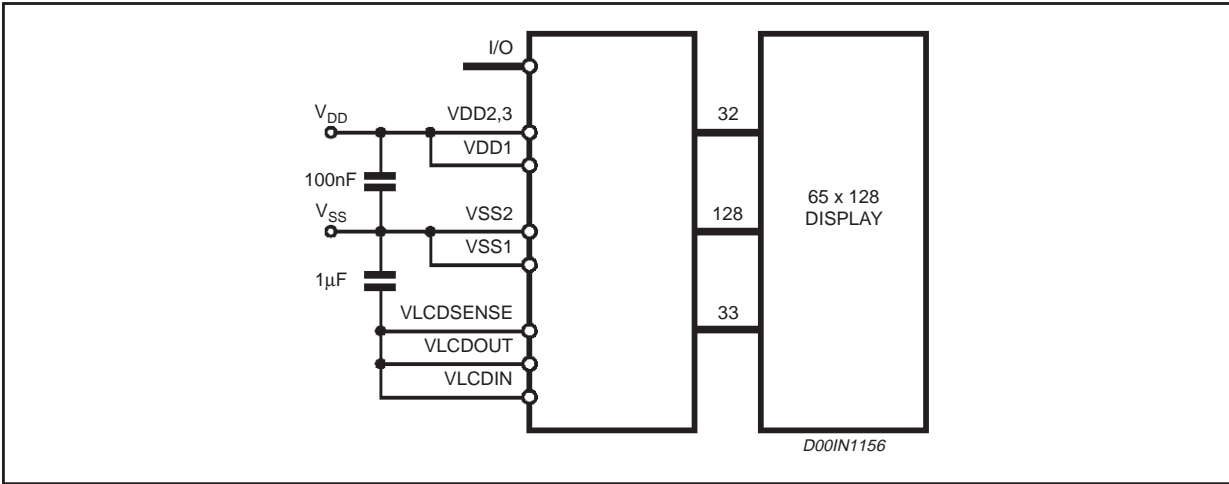


Figure 27. Pad Configuration with I2C interface

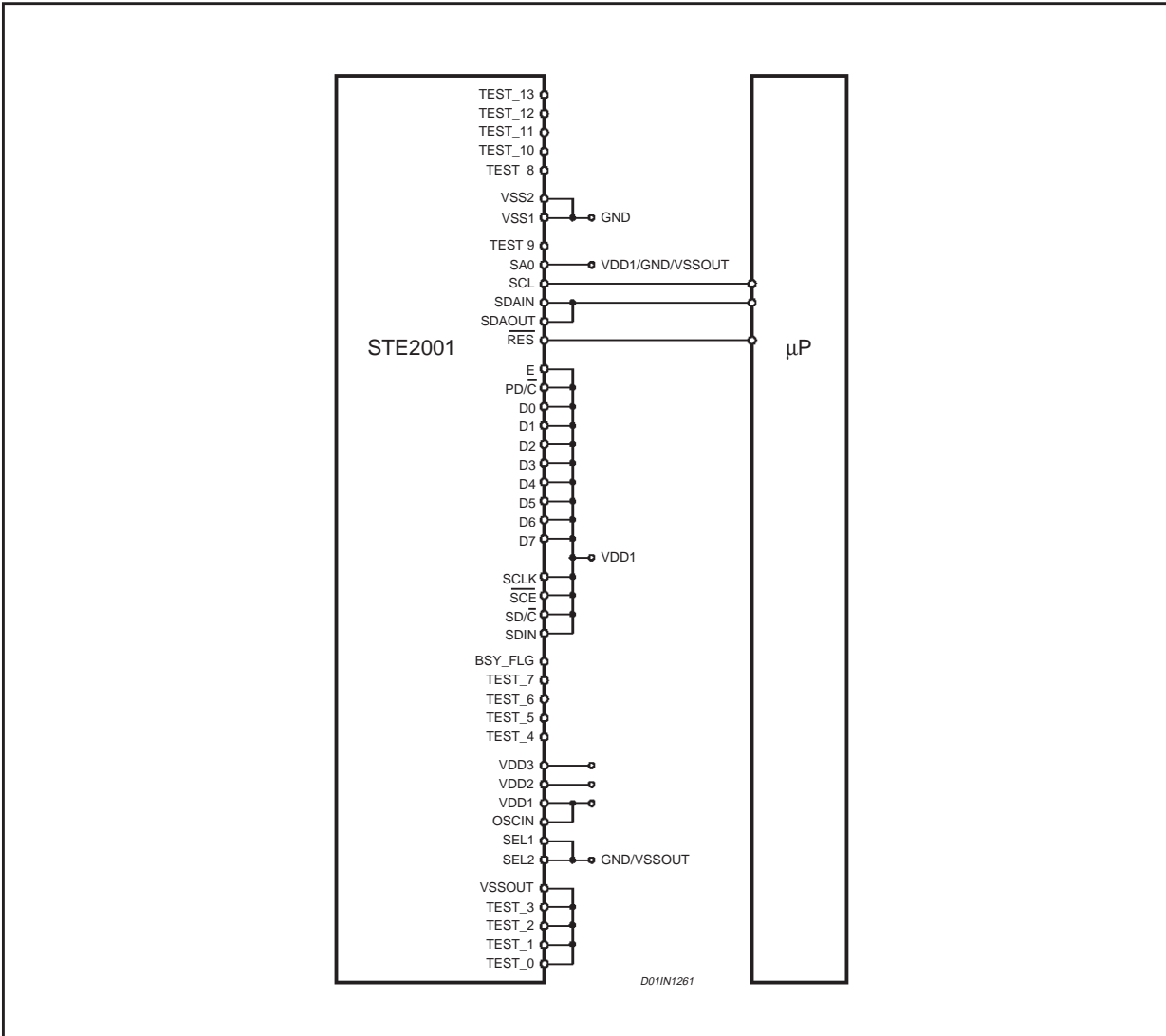


Figure 28. Pad Configuration with Parallel interface

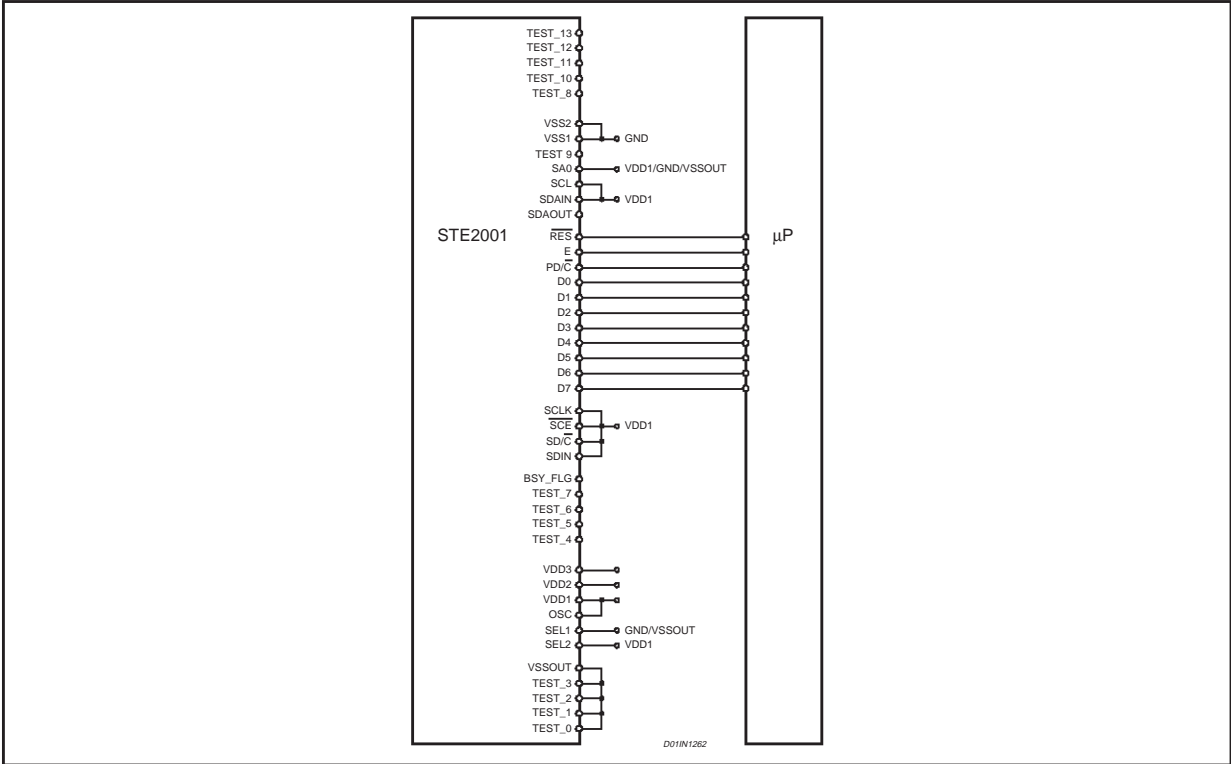
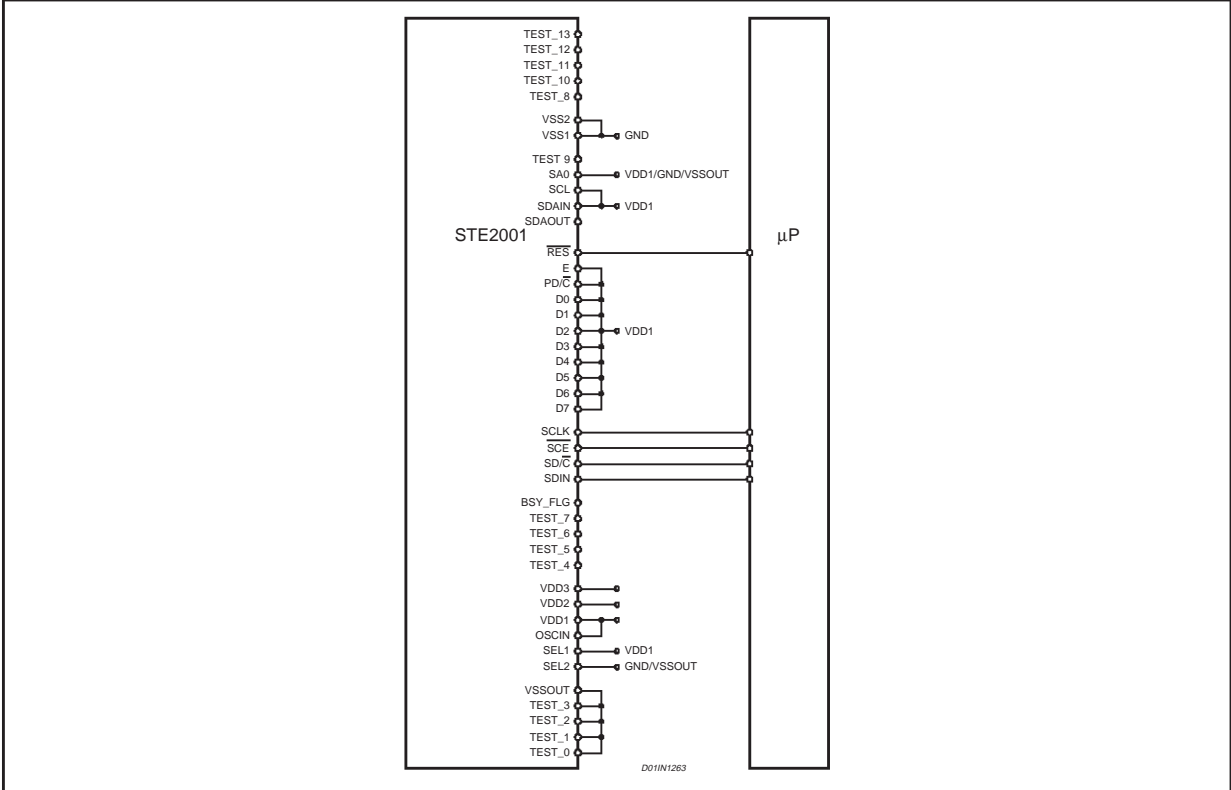


Figure 29. Pad Configuration with Serial interface



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Figure 30. Power OFF Timing Diagram

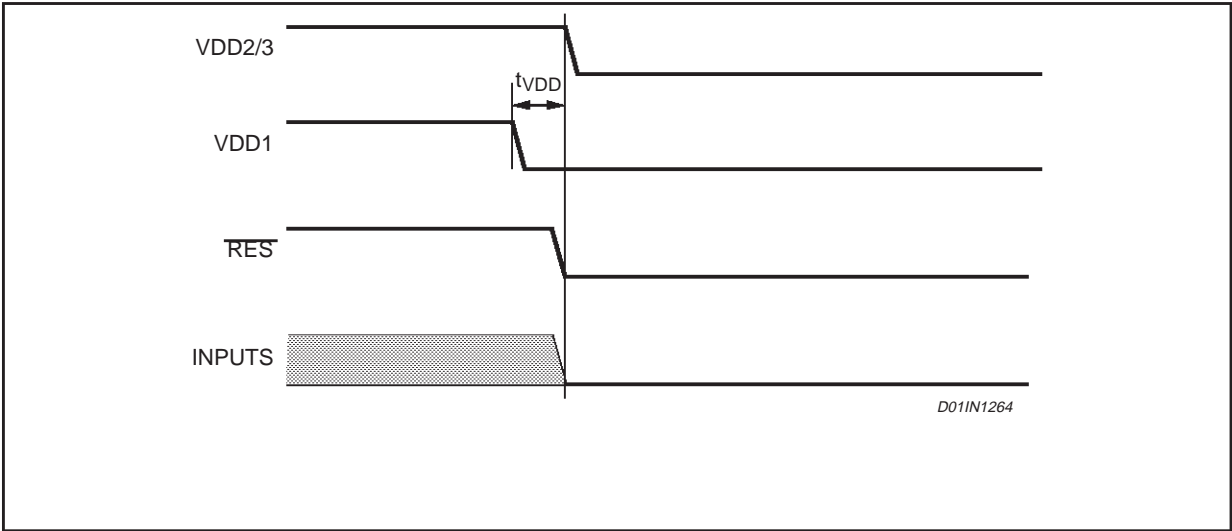


Figure 31. Power OFF Sequence

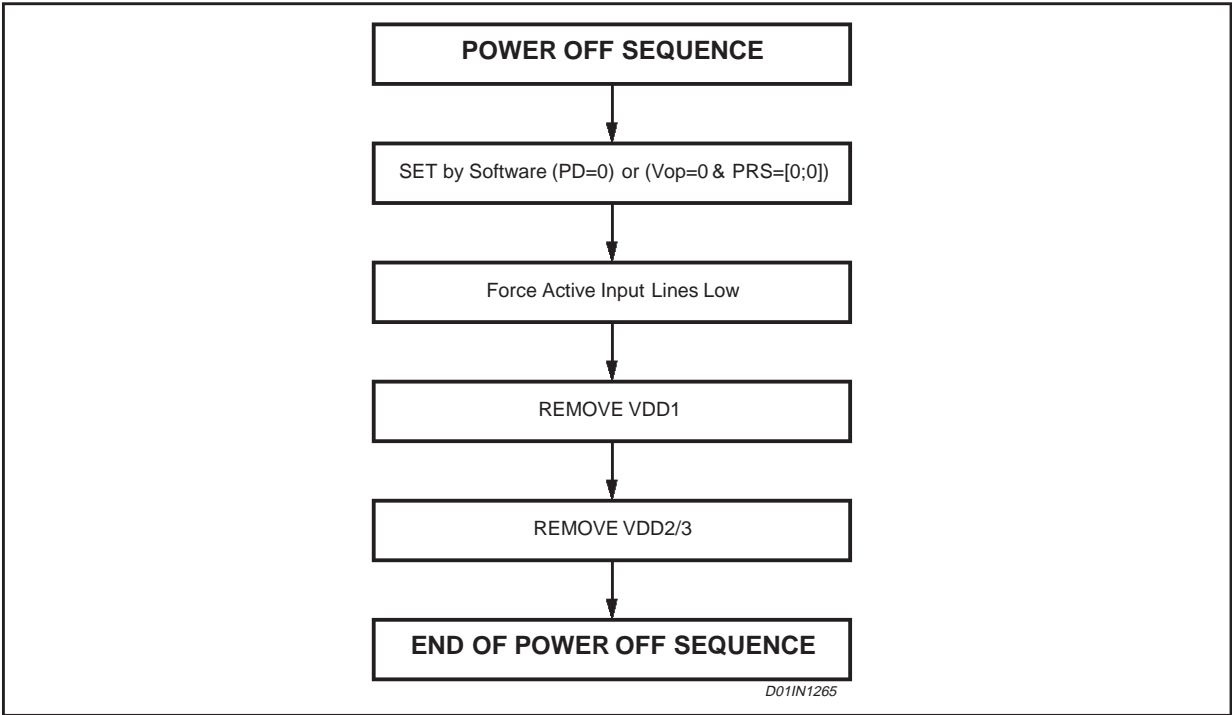


Figure 32. Power-Up & RESET timing diagram

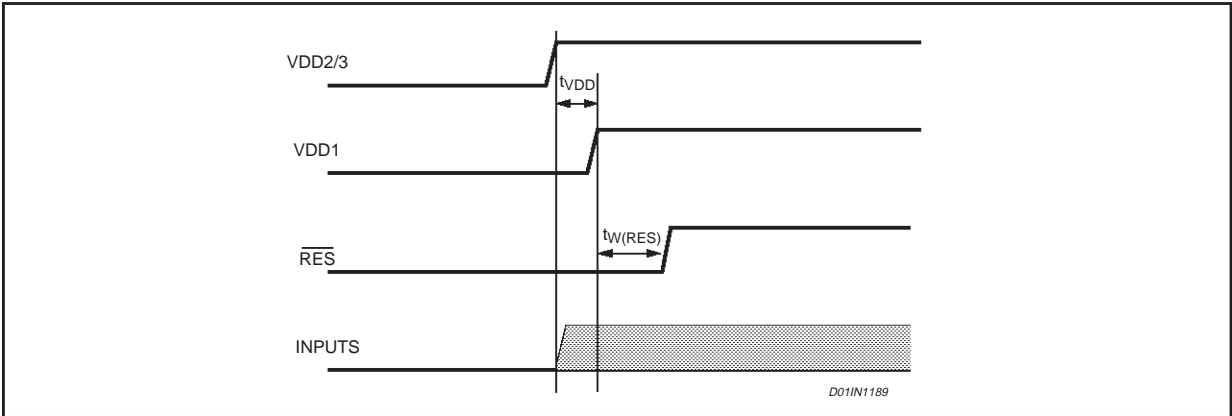


Figure 33. Power-Up & RESET timing diagram

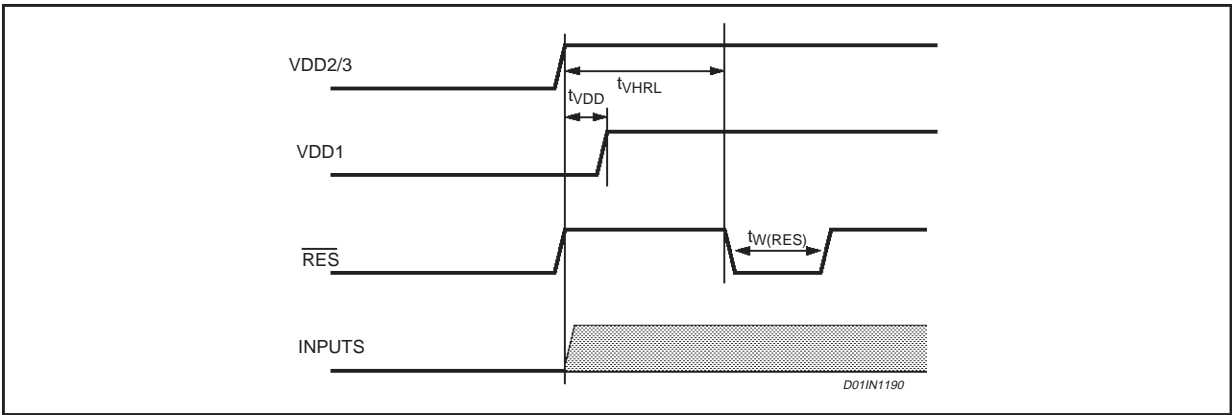
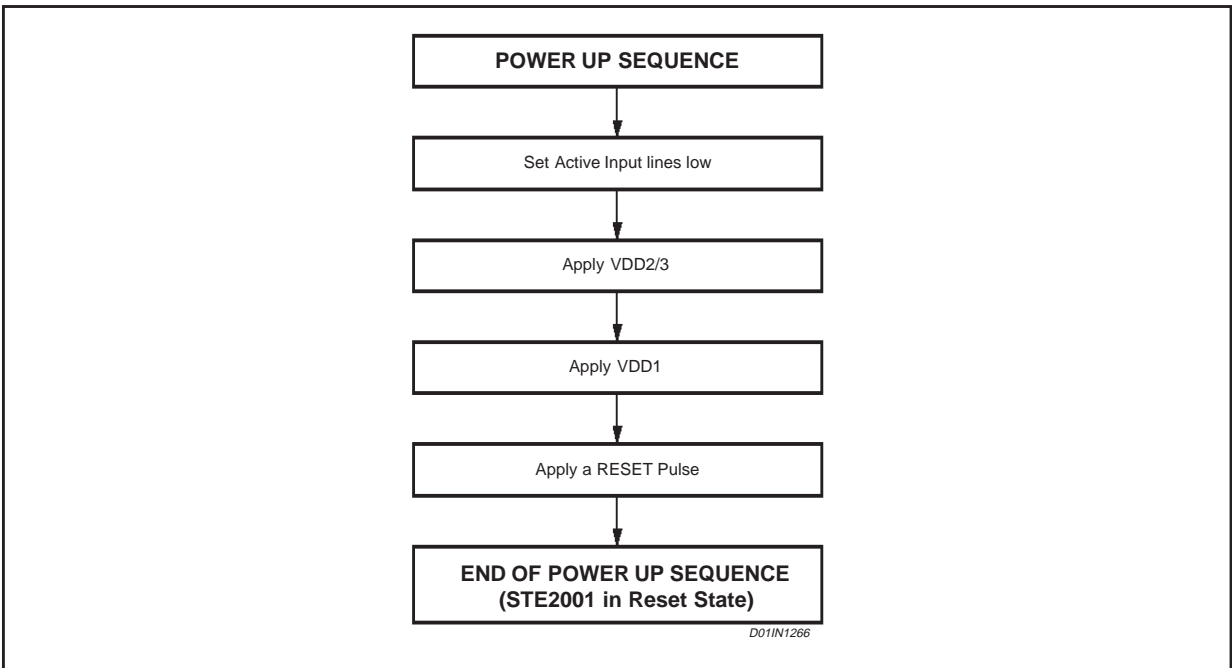


Figure 34. Power Up Sequence



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Figure 35. Chip Mechanical Drawing

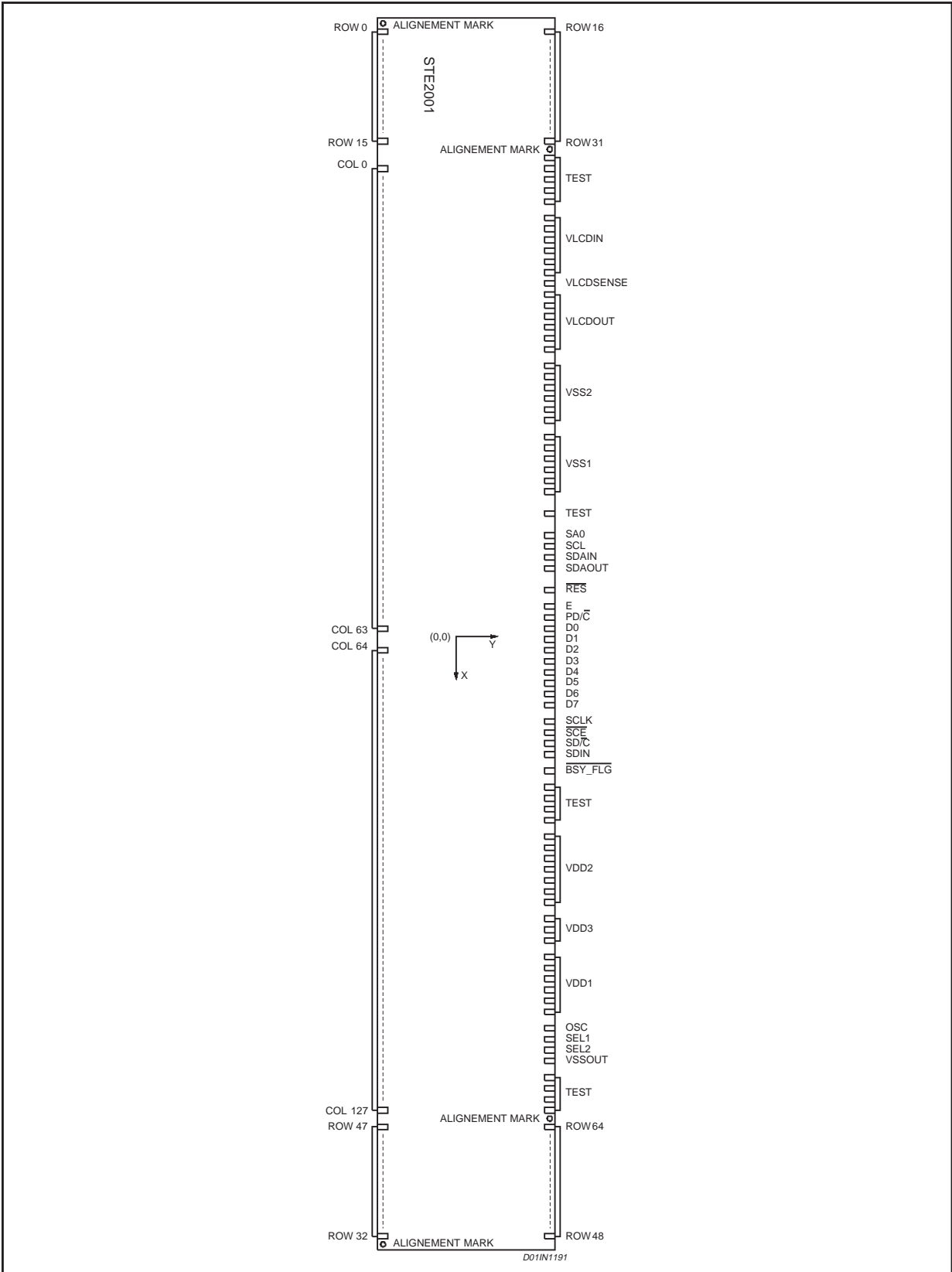
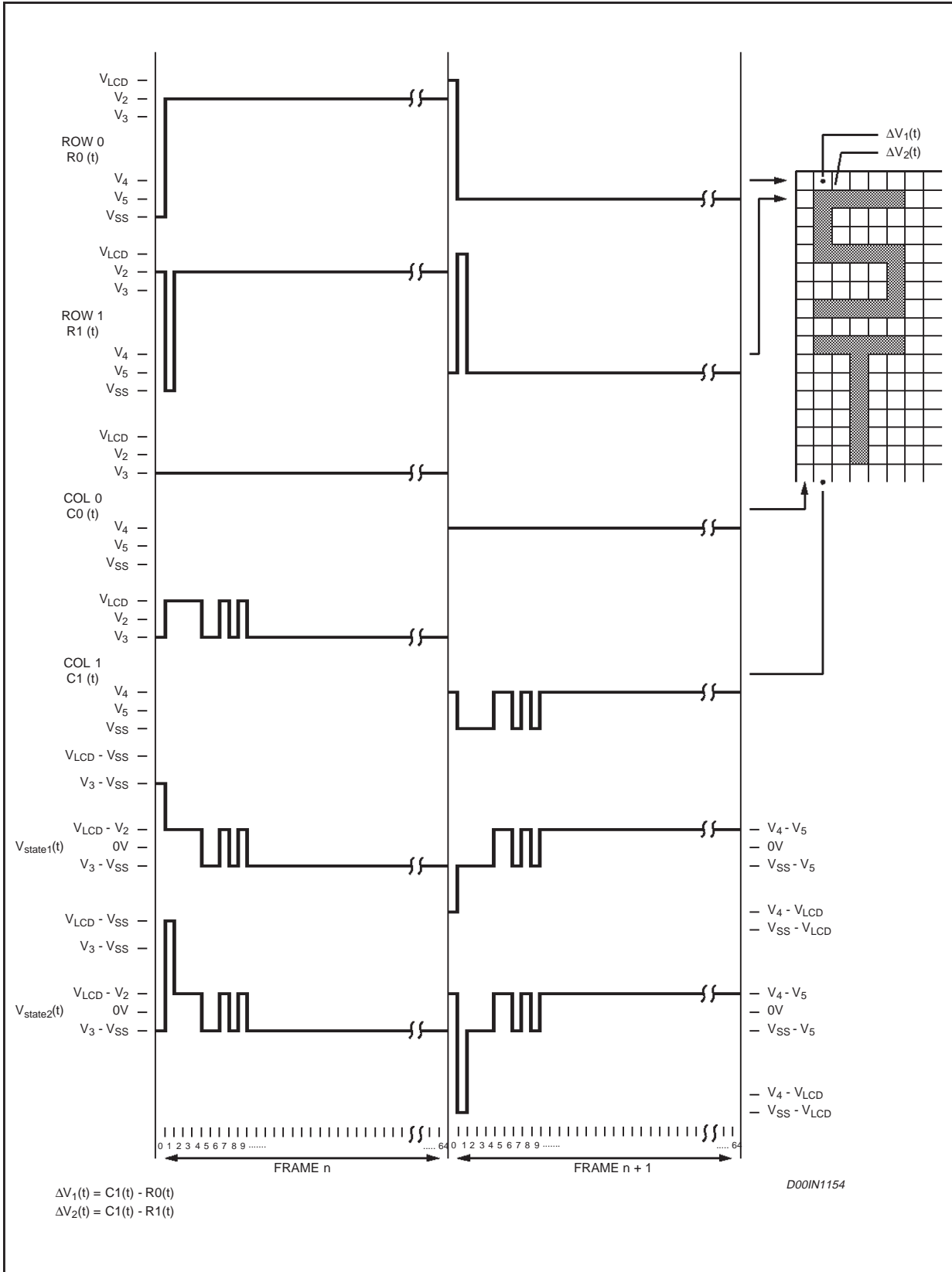


Figure 36. Improved ALTH & PLESKO Driving Method



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Figure 37. DATA RAM to display Mapping

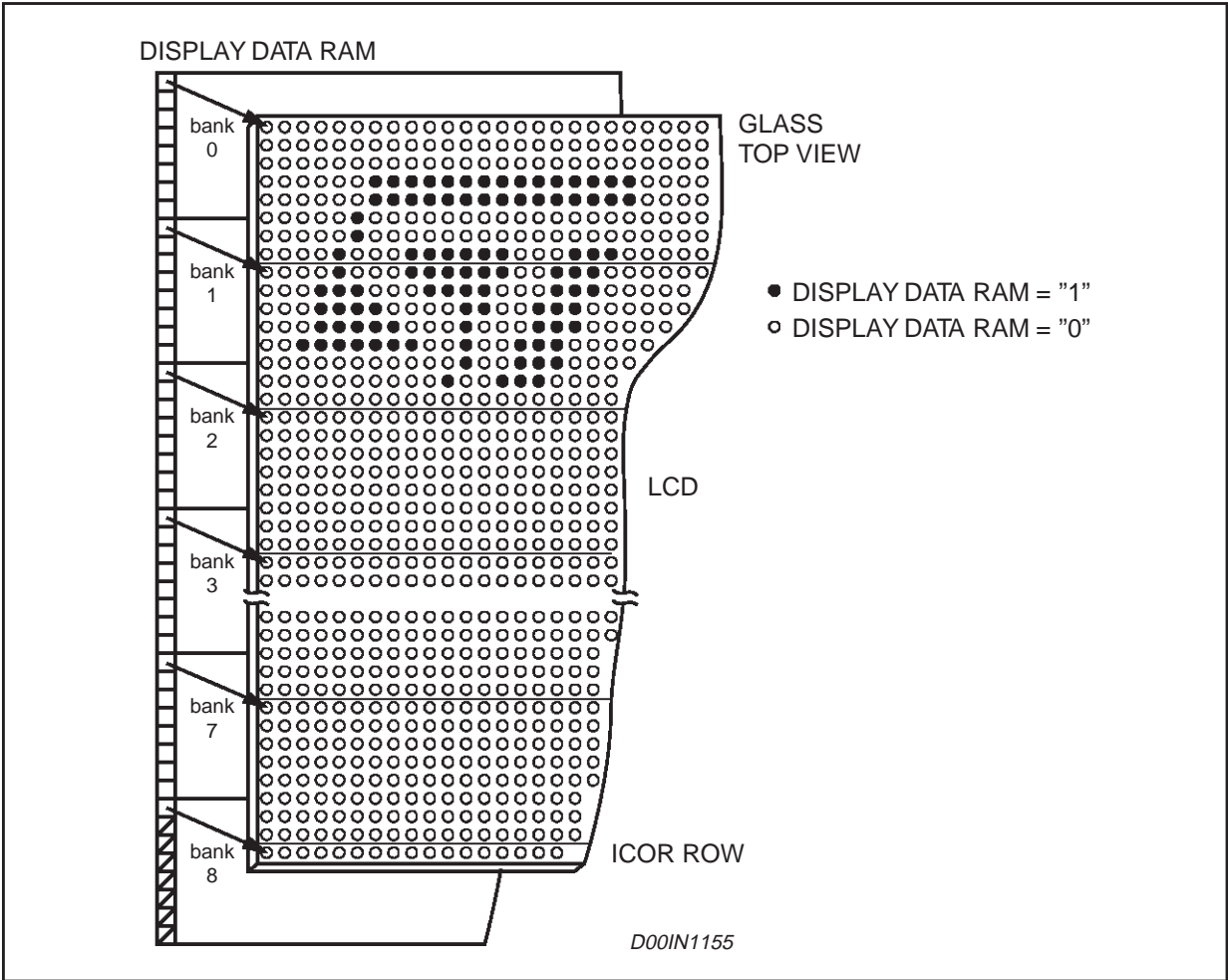


Table 7. Test Pin Configuration

| Test Numb. | Pin |
|------------|------|
| TEST_0 | GND |
| TEST_1 | GND |
| TEST_2 | GND |
| TEST_3 | GND |
| TEST_4 | OPEN |
| TEST_5 | OPEN |
| TEST_6 | OPEN |
| TEST_7 | OPEN |
| T8 | OPEN |
| T9 | OPEN |
| TEST_10 | OPEN |
| TEST_11 | OPEN |
| TEST_12 | OPEN |
| TEST_13 | OPEN |



Table 8. Mechanical Dimensions

| | |
|-----------------|--|
| Die Size | 2.12mmX12.5mm |
| Pad Pitch | 70 μm |
| Pad Size | 62 μm X 100 μm |
| Bump Dimensions | 50 μm X88 μm X17.5 |
| WFS Thickness | 500 μm |

Table 9. Pad Coordinates (continued)

Table 9. Pad Coordinates

| NAME | PAD | X (μm) | Y(μm) |
|------|-----|---------------------|--------------------|
| R0 | 1 | -5,994 | -898.2 |
| R1 | 2 | -5,924 | -898.2 |
| R2 | 3 | -5,854 | -898.2 |
| R3 | 4 | -5,784 | -898.2 |
| R4 | 5 | -5,714 | -898.2 |
| R5 | 6 | -5,644 | -898.2 |
| R6 | 7 | -5,574 | -898.2 |
| R7 | 8 | -5,504 | -898.2 |
| R8 | 9 | -5,434 | -898.2 |
| R9 | 10 | -5,364 | -898.2 |
| R10 | 11 | -5,294 | -898.2 |
| R11 | 12 | -5,224 | -898.2 |
| R12 | 13 | -5,154 | -898.2 |
| R13 | 14 | -5,084 | -898.2 |
| R14 | 15 | -5,014 | -898.2 |
| R15 | 16 | -4,944 | -898.2 |
| C0 | 17 | -4,591.8 | -898.2 |
| C1 | 18 | -4,521.8 | -898.2 |
| C2 | 19 | -4,451.8 | -898.2 |
| C3 | 20 | -4,381.8 | -898.2 |
| C4 | 21 | -4,311.8 | -898.2 |
| C5 | 22 | -4,241.8 | -898.2 |
| C6 | 23 | -4,171.8 | -898.2 |
| C7 | 24 | -4,101.8 | -898.2 |
| C8 | 25 | -4,031.8 | -898.2 |
| C9 | 26 | -3,961.8 | -898.2 |
| C10 | 27 | -3,891.8 | -898.2 |
| C11 | 28 | -3,821.8 | -898.2 |
| C12 | 29 | -3,751.8 | -898.2 |

| NAME | PAD | X (μm) | Y(μm) |
|------|-----|---------------------|--------------------|
| C13 | 30 | -3,681.8 | -898.2 |
| C14 | 31 | -3,611.8 | -898.2 |
| C15 | 32 | -3,541.8 | -898.2 |
| C16 | 33 | -3,471.8 | -898.2 |
| C17 | 34 | -3,401.8 | -898.2 |
| C18 | 35 | -3,331.8 | -898.2 |
| C19 | 36 | -3,261.8 | -898.2 |
| C20 | 37 | -3,191.8 | -898.2 |
| C21 | 38 | -3,121.8 | -898.2 |
| C22 | 39 | -3,051.8 | -898.2 |
| C23 | 40 | -2,981.8 | -898.2 |
| C24 | 41 | -2,911.8 | -898.2 |
| C25 | 42 | -2,841.8 | -898.2 |
| C26 | 43 | -2,771.8 | -898.2 |
| C27 | 44 | -2,701.8 | -898.2 |
| C28 | 45 | -2,631.8 | -898.2 |
| C29 | 46 | -2,561.8 | -898.2 |
| C30 | 47 | -2,491.8 | -898.2 |
| C31 | 48 | -2,421.8 | -898.2 |
| C32 | 49 | -2,351.8 | -898.2 |
| C33 | 50 | -2,281.8 | -898.2 |
| C34 | 51 | -2,211.8 | -898.2 |
| C35 | 52 | -2,141.8 | -898.2 |
| C36 | 53 | -2,071.8 | -898.2 |
| C37 | 54 | -2,001.8 | -898.2 |
| C38 | 55 | -1,931.8 | -898.2 |
| C39 | 56 | -1,861.8 | -898.2 |
| C40 | 57 | -1,791.8 | -898.2 |
| C41 | 58 | -1,721.8 | -898.2 |
| C42 | 59 | -1,651.8 | -898.2 |
| C43 | 60 | -1,581.8 | -898.2 |
| C44 | 61 | -1,511.8 | -898.2 |
| C45 | 62 | -1,441.8 | -898.2 |
| C46 | 63 | -1,371.8 | -898.2 |
| C47 | 64 | -1,301.8 | -898.2 |
| C48 | 65 | -1,231.8 | -898.2 |
| C49 | 66 | -1,161.8 | -898.2 |

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Table 9. Pad Coordinates (continued)

| NAME | PAD | X (μm) | Y(μm) |
|------|-----|----------|--------|
| C50 | 67 | -1,091.8 | -898.2 |
| C51 | 68 | -1,021.8 | -898.2 |
| C52 | 69 | -951.8 | -898.2 |
| C53 | 70 | -881.8 | -898.2 |
| C54 | 71 | -811.8 | -898.2 |
| C55 | 72 | -741.8 | -898.2 |
| C56 | 73 | -671.8 | -898.2 |
| C57 | 74 | -601.8 | -898.2 |
| C58 | 75 | -531.8 | -898.2 |
| C59 | 76 | -461.8 | -898.2 |
| C60 | 77 | -391.8 | -898.2 |
| C61 | 78 | -321.8 | -898.2 |
| C62 | 79 | -251.8 | -898.2 |
| C63 | 80 | -181.8 | -898.2 |
| C64 | 81 | 175.44 | -898.2 |
| C65 | 82 | 245.44 | -898.2 |
| C66 | 83 | 315.44 | -898.2 |
| C67 | 84 | 385.44 | -898.2 |
| C68 | 85 | 455.44 | -898.2 |
| C69 | 86 | 525.44 | -898.2 |
| C70 | 87 | 595.44 | -898.2 |
| C71 | 88 | 665.44 | -898.2 |
| C72 | 89 | 735.44 | -898.2 |
| C73 | 90 | 805.44 | -898.2 |
| C74 | 91 | 875.44 | -898.2 |
| C75 | 92 | 945.44 | -898.2 |
| C76 | 93 | 1,015.44 | -898.2 |
| C77 | 94 | 1,085.44 | -898.2 |
| C78 | 95 | 1,155.44 | -898.2 |
| C79 | 96 | 1,225.44 | -898.2 |
| C80 | 97 | 1,295.44 | -898.2 |
| C81 | 98 | 1,365.44 | -898.2 |
| C82 | 99 | 1,435.44 | -898.2 |
| C83 | 100 | 1,505.44 | -898.2 |
| C84 | 101 | 1,575.44 | -898.2 |
| C85 | 102 | 1,645.44 | -898.2 |
| C86 | 103 | 1,715.44 | -898.2 |

Table 9. Pad Coordinates (continued)

| NAME | PAD | X (μm) | Y(μm) |
|------|-----|----------|--------|
| C87 | 104 | 1,785.44 | -898.2 |
| C88 | 105 | 1,855.44 | -898.2 |
| C89 | 106 | 1,925.44 | -898.2 |
| C90 | 107 | 1,995.44 | -898.2 |
| C91 | 108 | 2,065.44 | -898.2 |
| C92 | 109 | 2,135.44 | -898.2 |
| C93 | 110 | 2,205.44 | -898.2 |
| C94 | 111 | 2,275.44 | -898.2 |
| C95 | 112 | 2,345.44 | -898.2 |
| C96 | 113 | 2,415.44 | -898.2 |
| C97 | 114 | 2,485.44 | -898.2 |
| C98 | 115 | 2,555.44 | -898.2 |
| C99 | 116 | 2,625.44 | -898.2 |
| C100 | 117 | 2,695.44 | -898.2 |
| C101 | 118 | 2,765.44 | -898.2 |
| C102 | 119 | 2,835.44 | -898.2 |
| C103 | 120 | 2,905.44 | -898.2 |
| C104 | 121 | 2,975.44 | -898.2 |
| C105 | 122 | 3,045.44 | -898.2 |
| C106 | 123 | 3,115.44 | -898.2 |
| C107 | 124 | 3,185.44 | -898.2 |
| C108 | 125 | 3,255.44 | -898.2 |
| C109 | 126 | 3,325.44 | -898.2 |
| C110 | 127 | 3,395.44 | -898.2 |
| C111 | 128 | 3,465.44 | -898.2 |
| C112 | 129 | 3,535.44 | -898.2 |
| C113 | 130 | 3,605.44 | -898.2 |
| C114 | 131 | 3,675.44 | -898.2 |
| C115 | 132 | 3,745.44 | -898.2 |
| C116 | 133 | 3,815.44 | -898.2 |
| C117 | 134 | 3,885.44 | -898.2 |
| C118 | 135 | 3,955.44 | -898.2 |
| C119 | 136 | 4,025.44 | -898.2 |
| C120 | 137 | 4,095.44 | -898.2 |
| C121 | 138 | 4,165.44 | -898.2 |
| C122 | 139 | 4,235.44 | -898.2 |
| C123 | 140 | 4,305.44 | -898.2 |

Table 9. Pad Coordinates (continued)

| NAME | PAD | X (μm) | Y(μm) |
|------|-----|----------|--------|
| C124 | 141 | 4,375.44 | -898.2 |
| C125 | 142 | 4,445.44 | -898.2 |
| C126 | 143 | 4,515.44 | -898.2 |
| C127 | 144 | 4,585.44 | -898.2 |
| R47 | 145 | 4,943.84 | -898.2 |
| R46 | 146 | 5,013.84 | -898.2 |
| R45 | 147 | 5,083.84 | -898.2 |
| R44 | 148 | 5,153.84 | -898.2 |
| R43 | 149 | 5,223.84 | -898.2 |
| R42 | 150 | 5,293.84 | -898.2 |
| R41 | 151 | 5,363.84 | -898.2 |
| R40 | 152 | 5,433.84 | -898.2 |
| R39 | 153 | 5,503.84 | -898.2 |
| R38 | 154 | 5,573.84 | -898.2 |
| R37 | 155 | 5,643.84 | -898.2 |
| R36 | 156 | 5,713.84 | -898.2 |
| R35 | 157 | 5,783.84 | -898.2 |
| R34 | 158 | 5,853.84 | -898.2 |
| R33 | 159 | 5,923.84 | -898.2 |
| R32 | 160 | 5,993.84 | -898.2 |
| R48 | 161 | 6,021.92 | 898.2 |
| R49 | 162 | 5,951.92 | 898.2 |
| R50 | 163 | 5,881.92 | 898.2 |
| R51 | 164 | 5,811.92 | 898.2 |
| R52 | 165 | 5,741.92 | 898.2 |
| R53 | 166 | 5,671.92 | 898.2 |
| R54 | 167 | 5,601.92 | 898.2 |
| R55 | 168 | 5,531.92 | 898.2 |
| R56 | 169 | 5,461.92 | 898.2 |
| R57 | 170 | 5,391.92 | 898.2 |
| R58 | 171 | 5,321.92 | 898.2 |
| R59 | 172 | 5,251.92 | 898.2 |
| R60 | 173 | 5,181.92 | 898.2 |
| R61 | 174 | 5,111.92 | 898.2 |
| R62 | 175 | 5,041.92 | 898.2 |
| R63 | 176 | 4,971.92 | 898.2 |
| R64 | 177 | 4,901.92 | 898.2 |

Table 9. Pad Coordinates (continued)

| NAME | PAD | X (μm) | Y(μm) |
|----------|-----|----------|-------|
| TEST_3 | 178 | 4,640.52 | 898.2 |
| TEST_2 | 179 | 4,500.68 | 898.2 |
| TEST_1 | 180 | 4,360.84 | 898.2 |
| TEST_0 | 181 | 4,221 | 898.2 |
| VSSOUT | 182 | 4,151 | 898.2 |
| SEL2 | 183 | 4,011.16 | 898.2 |
| SEL1 | 184 | 3,871.32 | 898.2 |
| OSC | 185 | 3,731.48 | 898.2 |
| VDD1_1 | 186 | 3,661.48 | 898.2 |
| VDD1_2 | 187 | 3,591.48 | 898.2 |
| VDD1_3 | 188 | 3,521.48 | 898.2 |
| VDD1_4 | 189 | 3,451.48 | 898.2 |
| VDD1_5 | 190 | 3,381.48 | 898.2 |
| VDD1_6 | 191 | 3,311.48 | 898.2 |
| VDD3_1 | 192 | 3,223.08 | 898.2 |
| VDD3_2 | 193 | 3,153.08 | 898.2 |
| VDD3_3 | 194 | 3,083.08 | 898.2 |
| VDD2_1 | 195 | 2,994.68 | 898.2 |
| VDD2_2 | 196 | 2,924.68 | 898.2 |
| VDD2_3 | 197 | 2,854.68 | 898.2 |
| VDD2_4 | 198 | 2,784.68 | 898.2 |
| VDD2_5 | 199 | 2,714.68 | 898.2 |
| VDD2_6 | 200 | 2,644.68 | 898.2 |
| VDD2_7 | 201 | 2,574.68 | 898.2 |
| TEST_7 | 202 | 2,033.84 | 898.2 |
| TEST_6 | 203 | 1,894 | 898.2 |
| TEST_5 | 204 | 1,754.16 | 898.2 |
| TEST_4 | 205 | 1,614.32 | 898.2 |
| BSY_FLAG | 206 | 1,474.48 | 898.2 |
| SDIN | 207 | 1,333.2 | 898.2 |
| SD/C | 208 | 1,193.36 | 898.2 |
| SCE | 209 | 1,053.52 | 898.2 |
| SCLK | 210 | 913.68 | 898.2 |
| D7 | 211 | 773.84 | 898.2 |
| D6 | 212 | 634 | 898.2 |
| D5 | 213 | 494.16 | 898.2 |
| D4 | 214 | 354.32 | 898.2 |

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Table 9. Pad Coordinates (continued)

| NAME | PAD | X (μm) | Y(μm) |
|----------|-----|-----------|-------|
| D3 | 215 | 214.48 | 898.2 |
| D2 | 216 | 74.64 | 898.2 |
| D1 | 217 | -65.2 | 898.2 |
| D0 | 218 | -205.04 | 898.2 |
| PD/C | 219 | -344.88 | 898.2 |
| E | 220 | -484.72 | 898.2 |
| RES | 221 | -624.56 | 898.2 |
| SDA_OUT | 222 | -764.4 | 898.2 |
| SDA_IN | 223 | -904.24 | 898.2 |
| SCL | 224 | -1,044.08 | 898.2 |
| SA0 | 225 | -1,183.92 | 898.2 |
| TEST9 | 226 | -1,722.04 | 898.2 |
| VSS1_1 | 227 | -1,795.48 | 898.2 |
| VSS1_2 | 228 | -1,865.48 | 898.2 |
| VSS1_3 | 229 | -1,935.48 | 898.2 |
| VSS1_4 | 230 | -2,075.88 | 898.2 |
| VSS1_5 | 231 | -2,145.88 | 898.2 |
| VSS1_6 | 232 | -2,215.88 | 898.2 |
| VSS2_1 | 233 | -2,356.28 | 898.2 |
| VSS2_2 | 234 | -2,426.28 | 898.2 |
| VSS2_3 | 235 | -2,496.28 | 898.2 |
| VSS2_4 | 236 | -2,636.68 | 898.2 |
| VSS2_5 | 237 | -2,706.68 | 898.2 |
| VSS2_6 | 238 | -2,776.68 | 898.2 |
| VLCDOUT1 | 239 | -3,545.64 | 898.2 |
| VLCDOUT2 | 240 | -3,615.64 | 898.2 |
| VLCDOUT3 | 241 | -3,685.64 | 898.2 |
| VLCDOUT4 | 242 | -3,755.64 | 898.2 |
| VLCDOUT5 | 243 | -3,825.64 | 898.2 |
| VLCDOUT6 | 244 | -3,895.64 | 898.2 |
| VLCSENSE | 245 | -3,968.08 | 898.2 |
| VLCDIN_1 | 246 | -4,040.48 | 898.2 |
| VLCDIN_2 | 247 | -4,110.48 | 898.2 |
| VLCDIN_3 | 248 | -4,180.48 | 898.2 |
| VLCDIN_4 | 249 | -4,250.48 | 898.2 |
| VLCDIN_5 | 250 | -4,320.48 | 898.2 |
| VLCDIN_6 | 251 | -4,390.48 | 898.2 |

Table 9. Pad Coordinates (continued)

| NAME | PAD | X (μm) | Y(μm) |
|---------|-----|-----------|-------|
| TEST_12 | 252 | -4,460.48 | 898.2 |
| TEST_13 | 253 | -4,540.48 | 898.2 |
| TEST_10 | 254 | -4,620.48 | 898.2 |
| TEST_11 | 255 | -4,700.48 | 898.2 |
| TEST_8 | 256 | -4,780.48 | 898.2 |
| R31 | 257 | -4,971.92 | 898.2 |
| R30 | 258 | -5,041.92 | 898.2 |
| R29 | 259 | -5,111.92 | 898.2 |
| R28 | 260 | -5,181.92 | 898.2 |
| R27 | 261 | -5,251.92 | 898.2 |
| R26 | 262 | -5,321.92 | 898.2 |
| R25 | 263 | -5,391.92 | 898.2 |
| R24 | 264 | -5,461.92 | 898.2 |
| R23 | 265 | -5,531.92 | 898.2 |
| R22 | 266 | -5,601.92 | 898.2 |
| R21 | 267 | -5,671.92 | 898.2 |
| R20 | 268 | -5,741.92 | 898.2 |
| R19 | 269 | -5,811.92 | 898.2 |
| R18 | 270 | -5,881.92 | 898.2 |
| R17 | 271 | -5,951.92 | 898.2 |
| R16 | 272 | -6,021.92 | 898.2 |

Table 10. Alignment marks coordinates

| X | Y | MARKS |
|---------|--------|-------|
| 4806.2 | 901.8 | mark1 |
| -4876.2 | 901.8 | mark2 |
| -6092.6 | -901.8 | mark3 |
| 6092.6 | -901.8 | mark4 |

Figure 38. Alignment marks dimensions

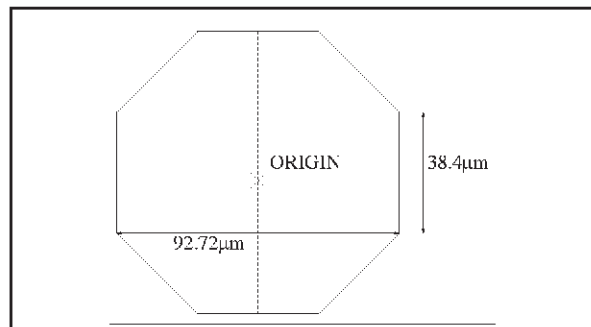


Figure 39.

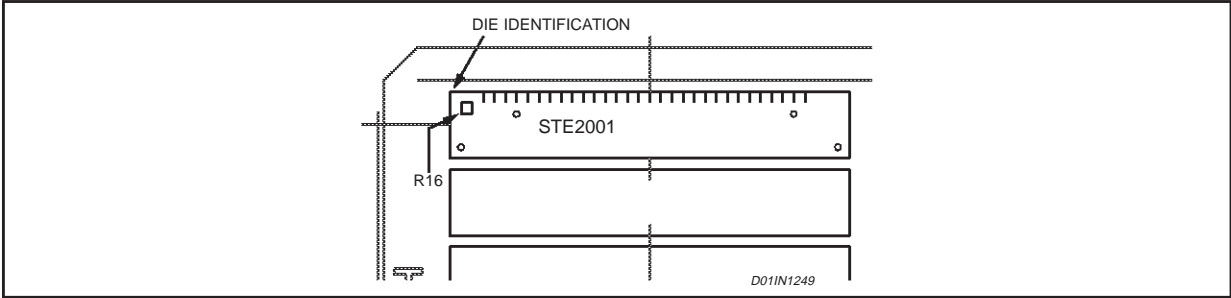
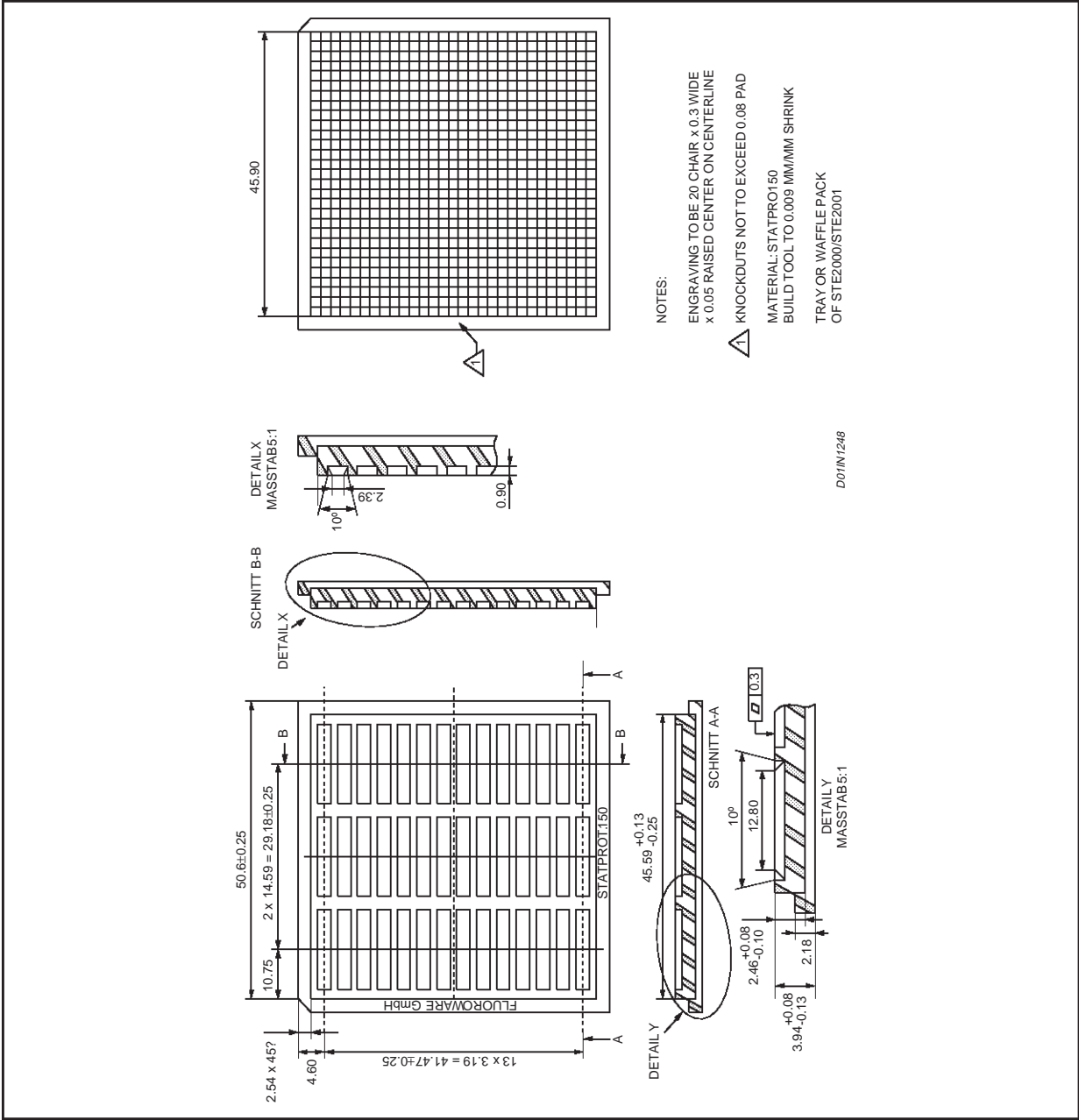


Figure 40. Tray Information



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