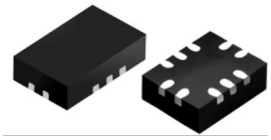
STEF512PUR

Datasheet

Dual electronic fuse (eFuse) for 5 V and 12 V rails



QFN10 (2 x 3 mm)

Maturity status link
STEF512PUR

Features

- 5 V and 12 V channels into one chip
- Output over voltage clamp
- Fixed current limit : 3 A on 5 V, 4 A on 12 V
- Latched-off thermal protection
- Input undervoltage lockout
- Adjustable output voltage slew rate for each channel
- Integrated 40 mΩ Power FETs
- SAS disable pin
- Current monitor output
- QFN10-2x3 package

Applications

- HD and SSD drives
- Set-top boxes
- DVD and Blu-ray disc drivers

Description

The STEF512PUR is an integrated dual electronic eFuse, designed to protect circuitry on the output from overcurrent and overvoltage events, in those applications requiring hot swap operation and in-rush current control.

The device embeds two independent electronic fuses, one for the 5 V rails and one for the 12 V rails. Thanks to the very low ON-resistance of the integrated power FETs, the voltage drop from the main supply to the load is very low during normal operation.

The startup time can be adjusted by the user for each eFuse, via two small soft-start capacitors, connected to the relevant pins.

In this way the inrush current at startup can be kept under control.

The maximum load current is precisely limited, by utilizing a sense FET topology, to factory-defined values (3 A for 5 V output and 4 A for 12 V output).

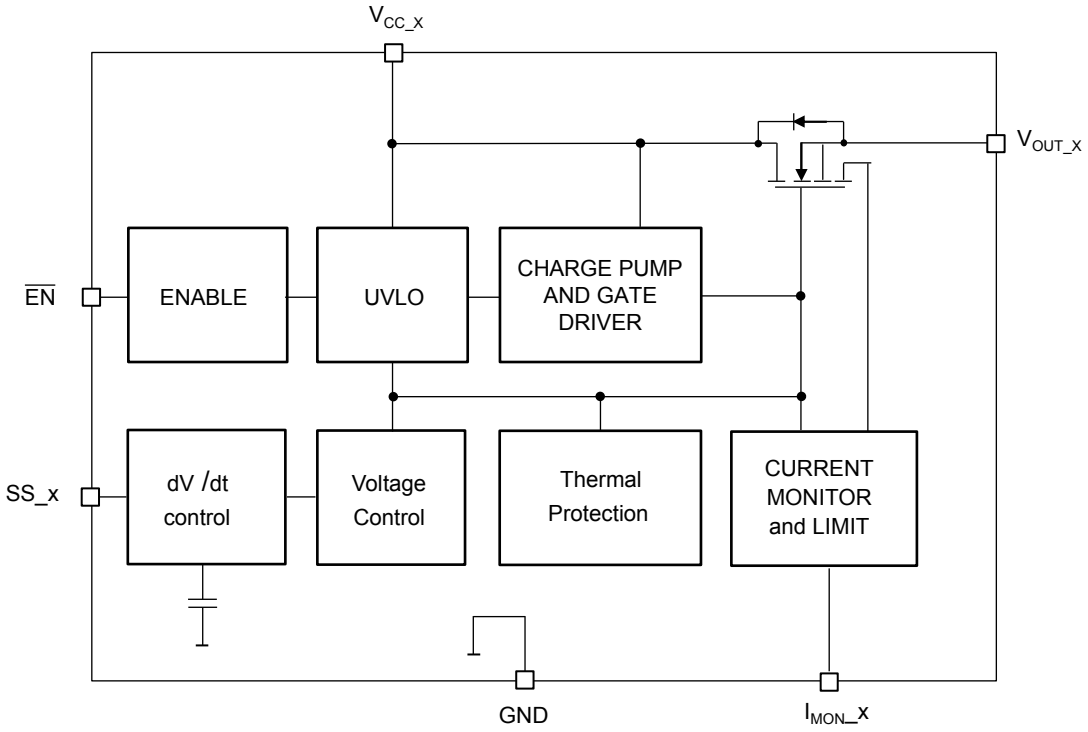
The device also provides precise overvoltage clamp for each channel, preventing the load being damaged from power supply failures, and undervoltage lockout (UVLO), assuring that the input voltage is above the minimum operating threshold, before the power device is turned on.

When an overload condition occurs, the STEF512PUR limits the output current to the predefined safe value. If the anomalous overload condition persists, the device goes into thermal shutdown, the internal switch is opened and the load disconnected from the power supply.

In the QFN10 package two current monitor pins are available, providing continuous information on the load current for each channel.

1 Diagram

Figure 1. Block diagram (one channel)



2 Pin configuration

Figure 2. **Pin connection (top view)**

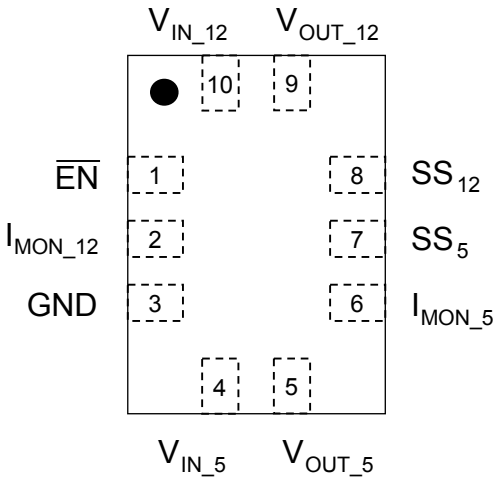
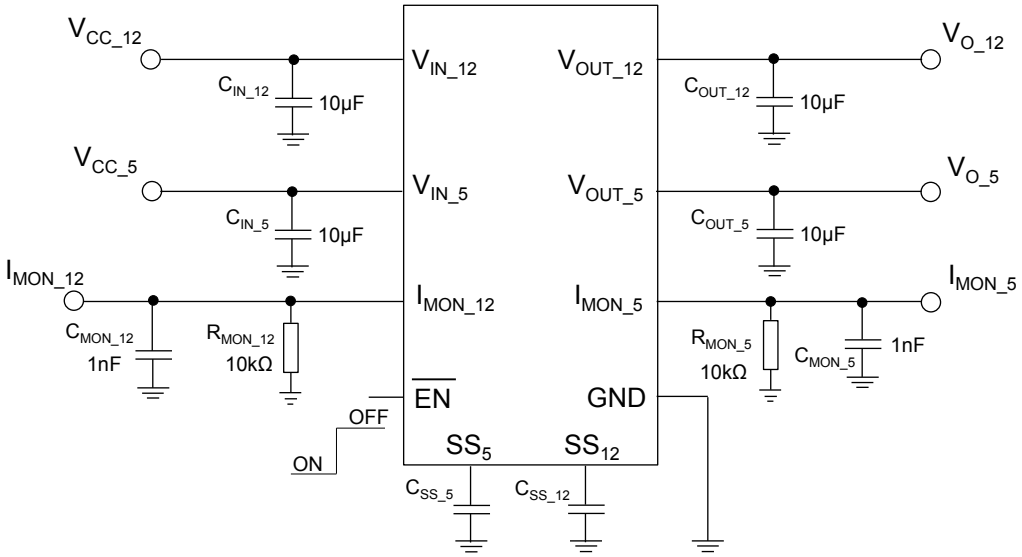


Table 1. **Pin description**

Symbol	Pin n°	Description
V_{IN_12}	10	12 V rail supply voltage
V_{IN_5}	4	5 V rail supply voltage
V_{OUT_12}	9	12 V rail output voltage
V_{OUT_5}	5	5 V rail output voltage
GND	3	Ground
$\overline{EN}$	1	SAS disable input: set this pin logic-low to turn on the device, high to turn off the device. This pin is internally pulled down via 1 MΩ resistor.
SS_5	7	Soft Start adjustment pin for the 5 V rail. A capacitor must be connected between this pin and GND to program the output voltage slew-rate. Do not leave floating.
SS_{12}	8	Soft-start adjustment pin for the 12 V rail. A capacitor must be connected between this pin and GND to program the output voltage slew-rate. Do not leave floating.
I_{MON_5}	6	5 V rail current monitor. Connect a resistor between this pin and GND.
I_{MON_12}	2	12 V rail current monitor. Connect a resistor between this pin and GND.

3 Typical application

Figure 3. **Typical application diagram**



4 Maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN_5}, V_{IN_12}	Input supply voltage (max 100 ms)	- 0.3 to 25	V
V_{IN_5}, V_{IN_12}	Input supply voltage	- 0.3 to 20	V
V_{OUT_5}	Output voltage (1)	10	V
V_{OUT_12}	Output voltage (1)	18	V
$V_{\overline{EN}}$	Enable pin voltage	- 0.3 to 7	V
SS_x	Soft-start pin voltage	- 0.3 to 7	V
I_{MON_x}	Monitor pin voltage	- 0.3 to 7	V
ESD	Charge device model	± 500	V
	Human body model	± 2000	
$T_{J\text{-}OP}$	Operating junction temperature	- 40 to 125	°C
$T_{J\text{-}MAX}$	Maximum junction temperature	150	°C
T_{STG}	Storage temperature	- 55 to 150	°C

1. *Refer to Section 6.5.*

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	105	°C/W
R_{thJC}	Thermal resistance junction to case	16	°C/W

5 Electrical characteristics

T_J = 25 °C, V_{IN_5} = 5 V, V_{IN_12} = 12 V, $\overline{EN}$ = 0 V; C_{IN} = 10 µF; C_{OUT} = 10 µF; unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
5 V eFuse						
V_{Clamp_5}	Output clamping voltage	V_{IN_5} = 8 V, I_{OUT} = 5 mA	5.5	5.7	5.9	V
V_{UVLO_5}	Undervoltage lockout	Turn-on, voltage rising	4.25	4.35	4.45	V
V_{Hyst_5}	UVLO hysteresis	Turn-off, voltage falling		1.78		V
R_{DSon_5}	On-resistance	T_J = 25 °C		36		mΩ
		T_J = 125 °C			50	
I_{L_5}	Off state leakage current	$V_{\overline{EN}}$ = 5 V, V_{OUT_5} = GND		1	5	µA
I_{D5}	Maximum continuous current	T_A = 25 °C		2.5		A
I_{Short_5}	Short-circuit current limit		0.6	1	1.4	A
I_{Lim_5}	Overload current limit		2.5	3	3.3	A
$dV/dt_{\_5}$	Output voltage ramp time	From 10 % to 90 % of V_{OUT} $C_{dv/dt}$ = 100 nF	11	13	15	ms
A_{I_5}	Current monitor output current gain, I_{MON_5} / I_{OUT_5}	I_{OUT_5} > = 200 mA	27	30	33	µA/A
12 V eFuse						
V_{Clamp_12}	Output clamping voltage	V_{IN_12} = 17 V, I_{OUT} = 5 mA	14.5	15	15.5	V
V_{UVLO_12}	Undervoltage lockout	Turn-on, voltage rising	9.4	9.7	10	V
V_{Hyst_12}	UVLO hysteresis (12 V rail)	Turn-off, voltage falling		2		V
R_{DSon_12}	On-resistance (12 V rail)	T_J = 25 °C		40		mΩ
		T_J = 125 °C			70	
I_{L_12}	Off state leakage current	$V_{\overline{EN}}$ = 5 V, V_{OUT_12} = GND		1	5	µA
I_{D12}	Continuous current (1)(2)	T_A = 25 °C		3.5		A
I_{Short_12}	Short-circuit current limit			1.8		A
I_{Lim_12}	Overload current limit		3.6	4	4.5	A
$dV/dt_{\_12}$	Output voltage ramp time	From 10 % to 90 % of V_{OUT}, $C_{dv/dt}$ = 100 nF	10	12	14	ms
A_{I_12}	Current monitor output current gain, I_{MON_12} / I_{OUT_12}	I_{OUT_12} ≥ 200 mA	27	30	33	µA/A
Common features						
V_{IL}	Low level input voltage	Output enabled			0.7	V
V_{IH}	High level input voltage	Output disabled	2.1			V
R_P	Pull-down resistor			1000		kΩ
I_q	Quiescent current (excluding $\overline{EN}$ current)	Device operating		250	1000	µA
		Off-state, = 5 V		40	80	µA
$I_{\overline{EN}}$	Enable pin current	$V_{\overline{EN}}$ = 5 V		5	10	µA

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Thermalprotection						
TSD	Shutdown temperature (1)			165		°C
	Hysteresis			20		

1. *Guaranteedby design, but not tested in production.*
2. *The maximum continuous current is the current level above which the control loop starts increasing the ON resistance of the pass element.*

Table 5. Recommended operating condition

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN}	Input capacitance	Stability	1	47		µF
C_{OUT}	Output capacitance		10	47		

6 Device functional description

The STEF512PUR embeds a 5 V and a 12 V electronic fuses (eFuses). Each eFuse is an intelligent load switch, able limit the voltage or the current during fault events, such as input overvoltage or output overload respectively. For this purpose it contains 2 analogue control loops, one limiting the output voltage and one limiting the input current.

The current limiting loop is also used during the start-up phase of the eFuse to limit the inrush current into the output capacitor.

During normal operation the eFuse behaves as a low-resistance Power FET, therefore the output voltage follows the input one. In case of overvoltage or overcurrent event, the eFuse limits the V_{GS} of the internal FET, in order to clamp the output voltage or current respectively. During such events the die temperature increases due to the power dissipation and so, if the fault persists and the overtemperature threshold is overcome, the device goes into thermal shutdown, the internal FET is turned-off and the load disconnected from the power supply.

Once the eFuse is in thermal shutdown, it does not restart automatically. The eFuse can be restarted manually by toggling the $\overline{EN}$ pin or performing a power-up cycle, (this will be effective as soon as the die temperature drops by at least the overtemperature hysteresis).

Each eFuse provides factory-trimmed undervoltage lockout feature and user-adjustable output voltage rise time.

6.1 Undervoltage lockout

Undervoltage lockout circuit prevents each eFuse to turn-on if the supply voltage is below the UVLO rising threshold. During operation, if the input voltage falls below (V_{UVLO_x} - V_{Hyst_x}), the output of the relevant channel is turned off.

If the supply voltage comes back into the operative range, the relevant channel restarts with soft-start cycle.

6.2 Startup sequence and voltage clamp

The typical start-up sequence of each eFuse is as follows:

- The power supply is connected to the V_{IN_x} pin and higher than the undervoltage lockout threshold
- The disable pin $\overline{EN}$ is asserted by the user to low logic level (or left floating), enabling the device
- Typically, 1.2 ms after the eFuse starts ramping up the output voltage
- Each channel will ramp up with a rate set by the relevant C_{SSx}
- If the input voltage continues rising, above the overvoltage threshold (V_{Clamp_x}), as a consequence of a failure in the power supply, the eFuse limits the output voltage to V_{Clamp_x}. The eFuse keeps operating in this state until it hits its overtemperature threshold and shuts down

6.3 Current limit function

Each eFuse provides 2 kinds of current limit protection mechanisms:

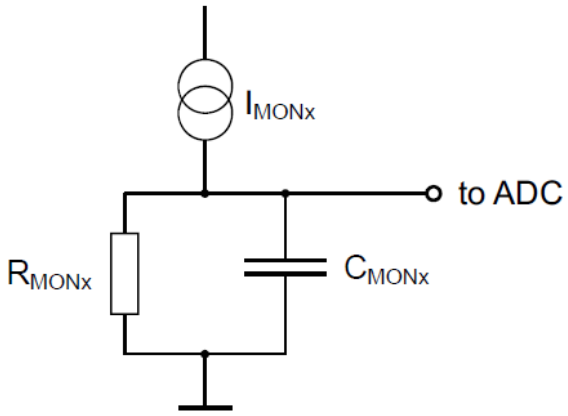
- In case of overload, the device starts increasing the power MOS resistance. The overload current limit (I_{Lim_x}) is 3 A typ. for the 5 V fuse and 4 A (typ.) for the 12 V
- In the case of strong overload or short circuit, the short-circuit current limit is activated and the current is clamped to I_{Short_x}: 1 A typ. on 5 V channel and 1.8 A typ. on 12 V channel

6.4 eFuse current monitor

The eFuse is equipped with current monitoring capability that allows the host processor to read the current flowing through each channel. An I_{MON_x} (x = 5, 12) current proportional to the load current flowing through the eFuse is imposed on an external R_{MON_x}, converting the sensing current into voltage for further processing by the ADC. An external RC filter is used to provide a stable signal (see figure below).

The current monitoring amplifier gain (A_{I_x} = I_{MON_x} / I_{OUT_x}) is typically 30 µA/A, as defined in the electrical characteristic Table 4. Electrical characteristics.

Figure 4. **Current monitor simplified circuit**



6.5 Application guidelines

Output capacitors are mandatory to guarantee device control loop stability. Input capacitors are recommended to reduce the transient effects of stray inductances which may be present on the input power paths. In fact, when the STEF512PUR interrupts the current flow, input inductance generates a positive voltage spike on the input, and output inductance generates a negative voltage spike on the output.

Input and output bypass capacitors must be placed as close as possible to the device.

When the device is powered by a power line made up of very long wires, the input inductance is higher than few µH, so the input capacitor should be increased in order to guarantee the proper operation of the device.

It is suggested to provide for additional protections and methods for addressing these transients, such as:

- Minimizing inductance of the input and output tracks
- TVS diodes on the input to absorb inductive spikes
- Schottky diode on the output to absorb negative spikes
- Combination of ceramic and electrolytic capacitors on the input and output

The device is not designed for continuous (DC) operation in reverse biasing conditions ($V_{OUT} > V_{IN} + 0.3$ V for more than 100 µs).

In fact the parasitic body diodes of the pass elements cannot withstand high current levels in DC biasing conditions that might lead to destruction or malfunction.

If this condition exists in the final application, we recommend placing a reverse current protection diode in series to the current path or selecting a device embedding reverse current protection MOSFET.

7 Typical characteristics

The following plots are referred to the typical application circuit and, unless otherwise noted, at T_A = 25 °C.

Figure 5. Start-up no load from V_{CC}

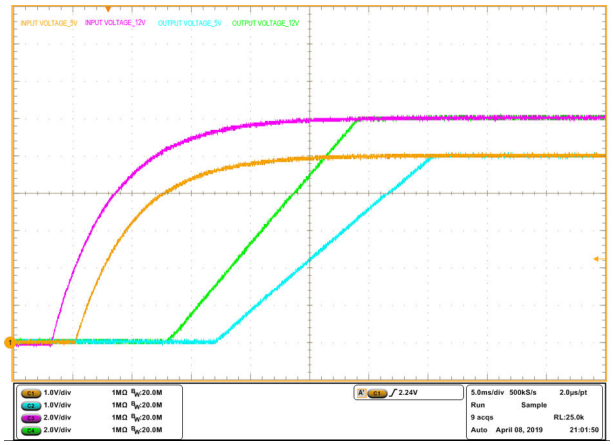


Figure 6. Out5 start-up with 2 A load

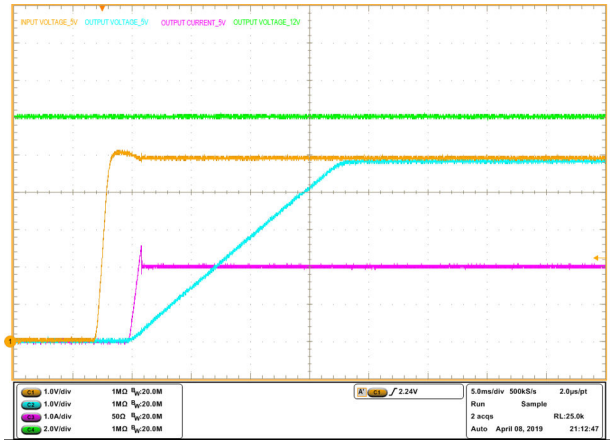


Figure 7. Out12 start-up with 2 A

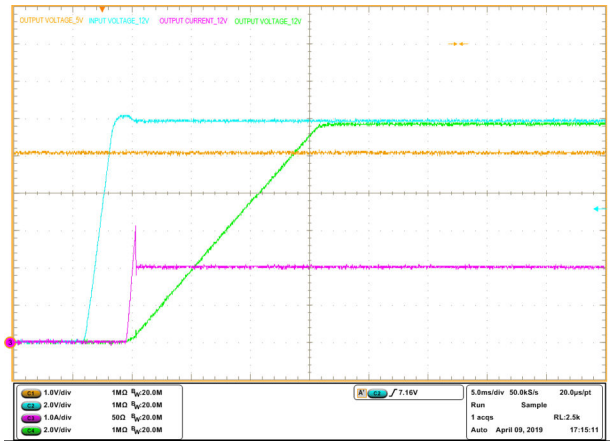


Figure 8. Start-up by EN, no load

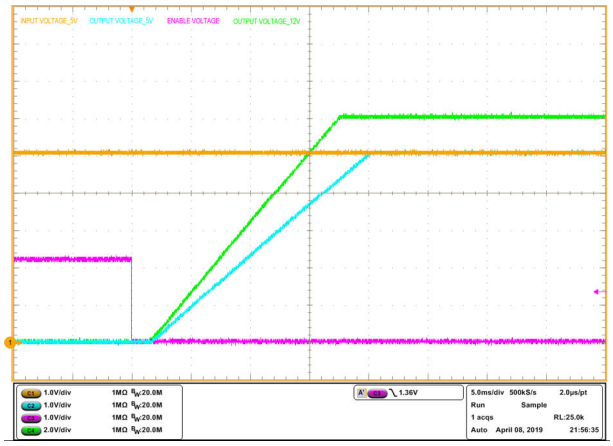


Figure 9. Start_up by En @ 2 A load

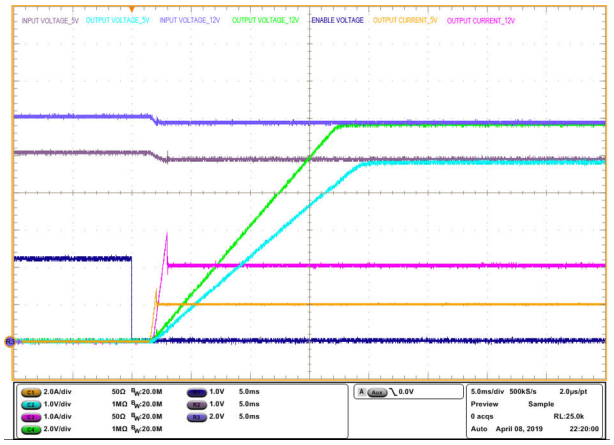


Figure 10. Out5 current limit and short

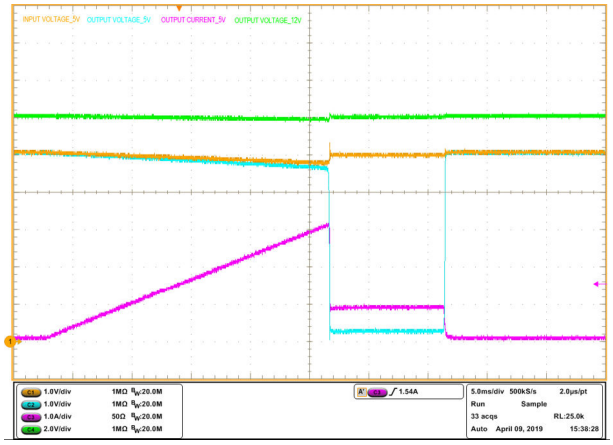


Figure 11. Out12 current limit and short

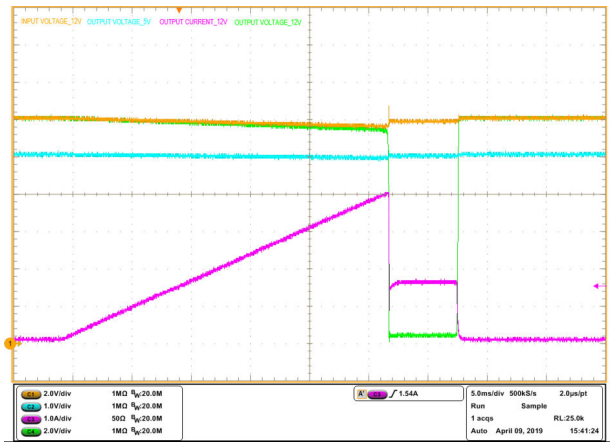


Figure 12. Out5 UVLO rising

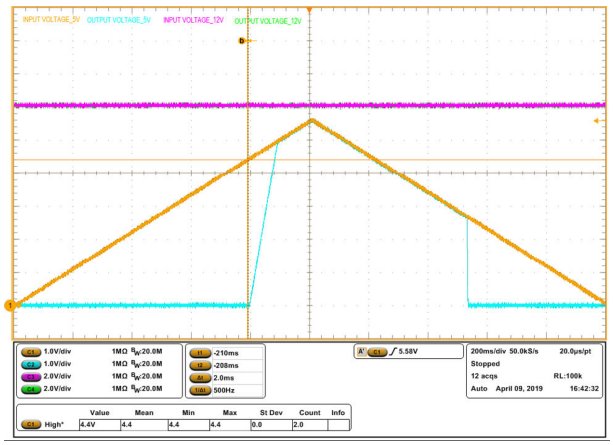


Figure 13. Out12 UVLO rising

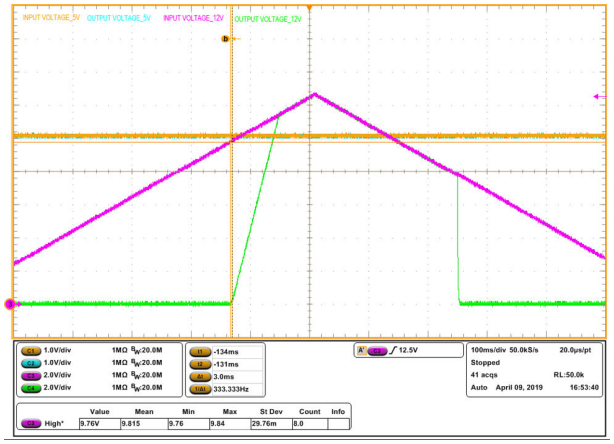


Figure 14. Out5 start-up vs. C_{SS}

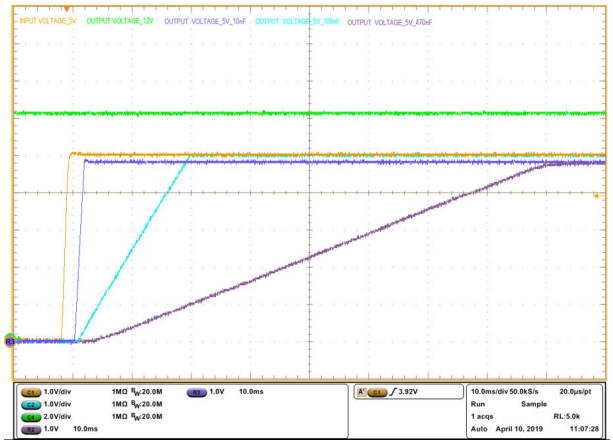


Figure 15. Out12 start-up vs. C_{SS}

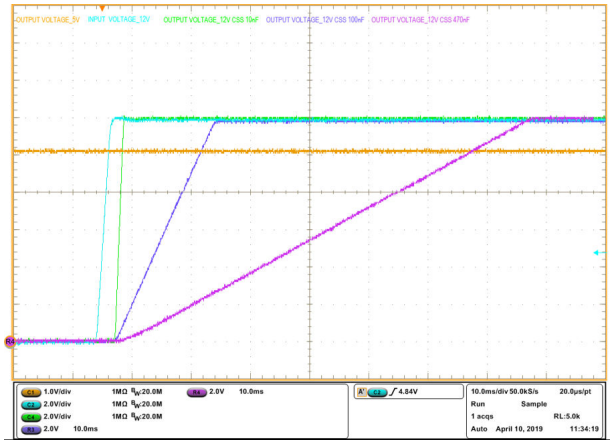


Figure 16. Out5 voltage clamp

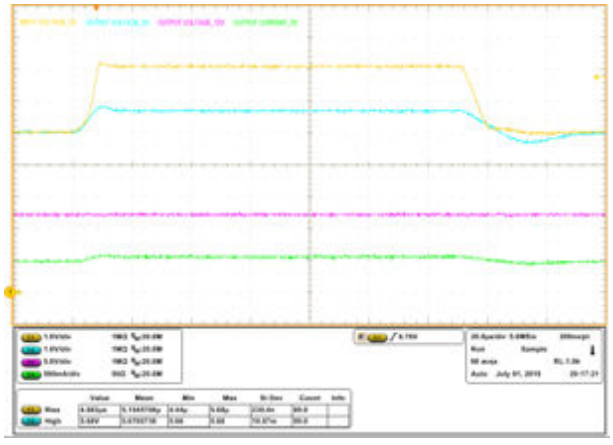


Figure 17. Out12 voltage clamp

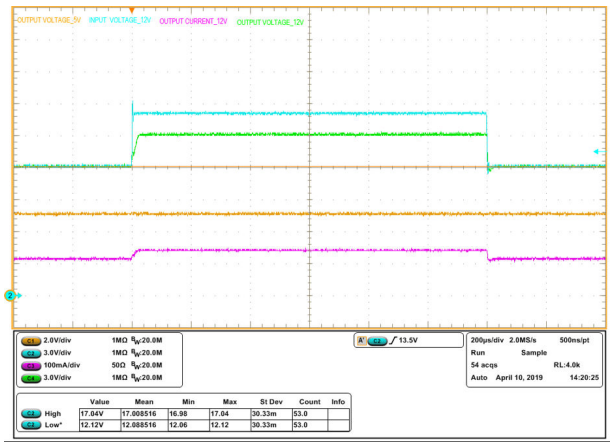


Figure 18. Imon5 gain

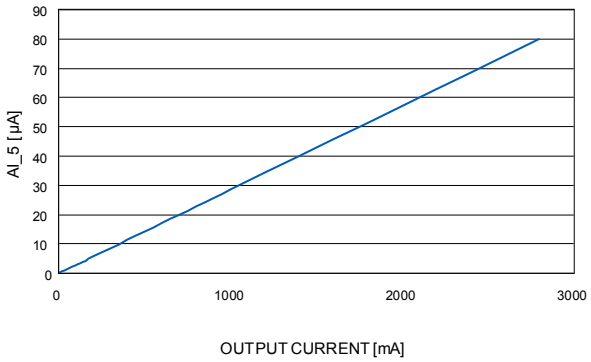


Figure 19. Imon12 Gain

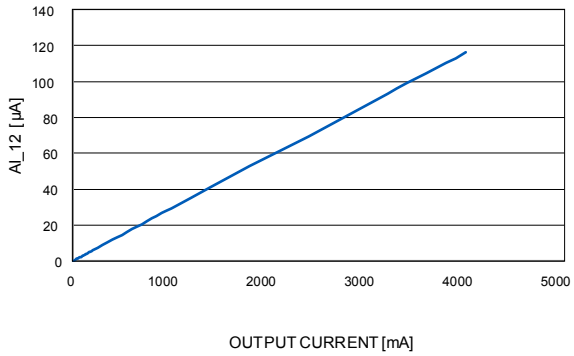


Figure 20. 5 V channel I_{lim} vs. temperature

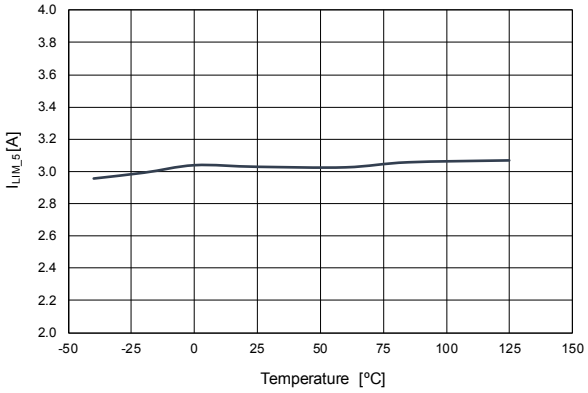


Figure 21. 12 V channel I_{lim} vs. temperature

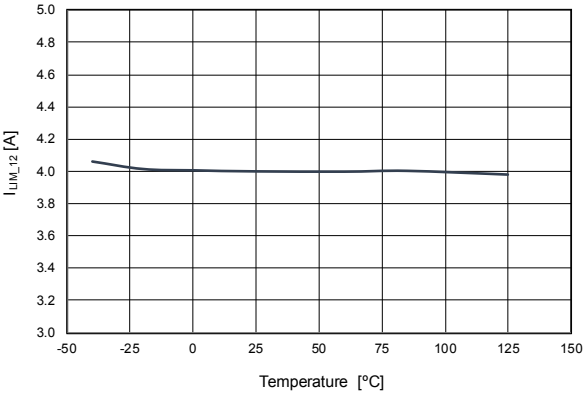


Figure 22. 5 V channel R_{DS_ON} vs. temperature

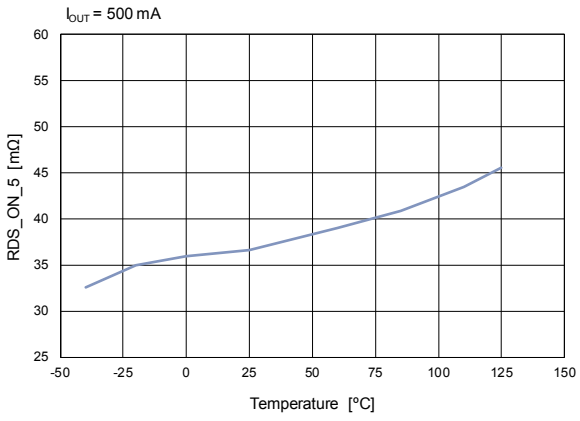
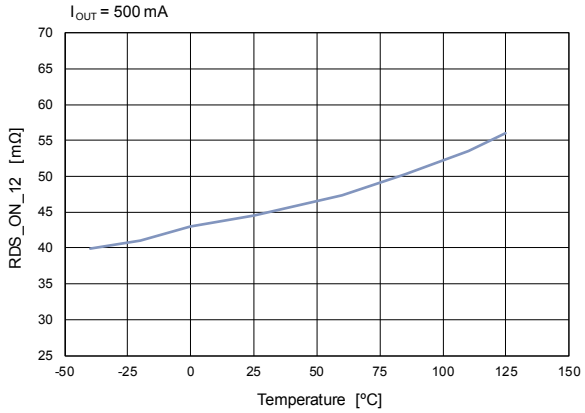


Figure 23. 12 V channel R_{DS_ON} vs. temperature



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 QFN10 (2 x 3 mm) package information

Figure 24. QFN10 (2 x 3 mm) package outline

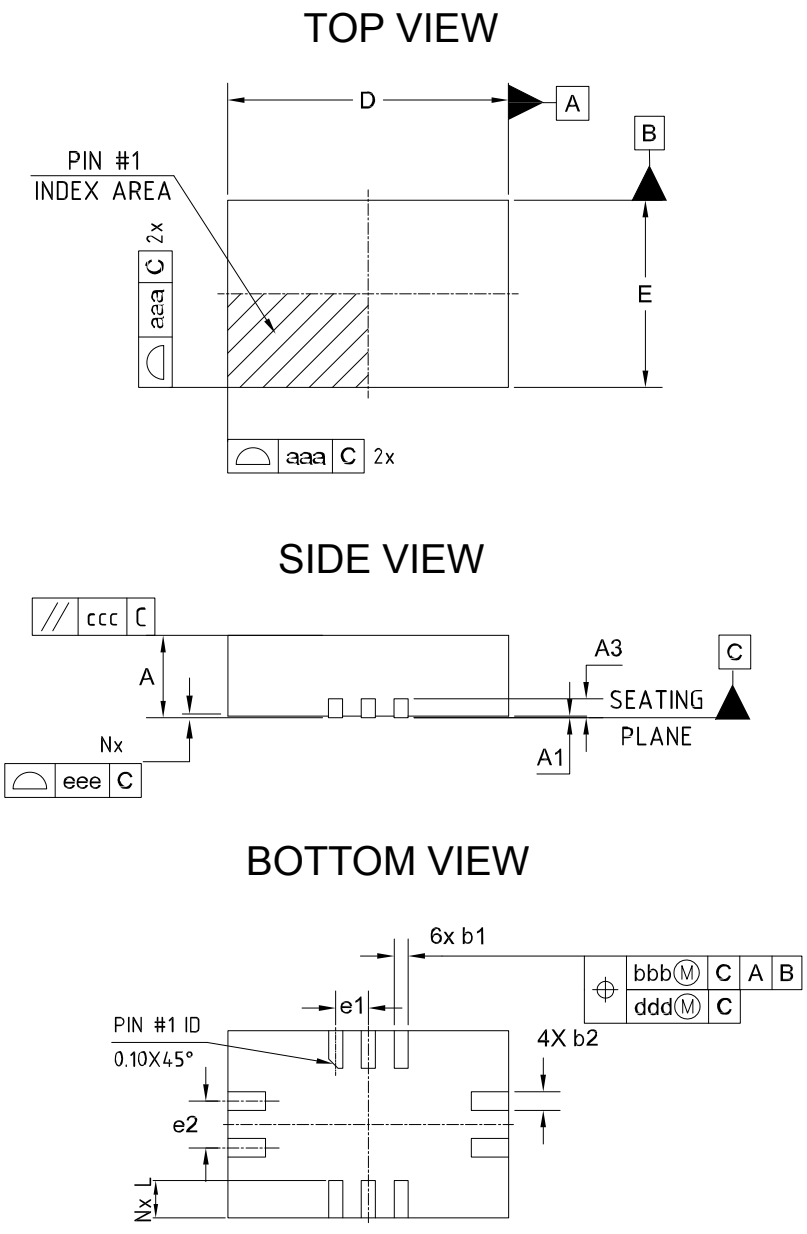
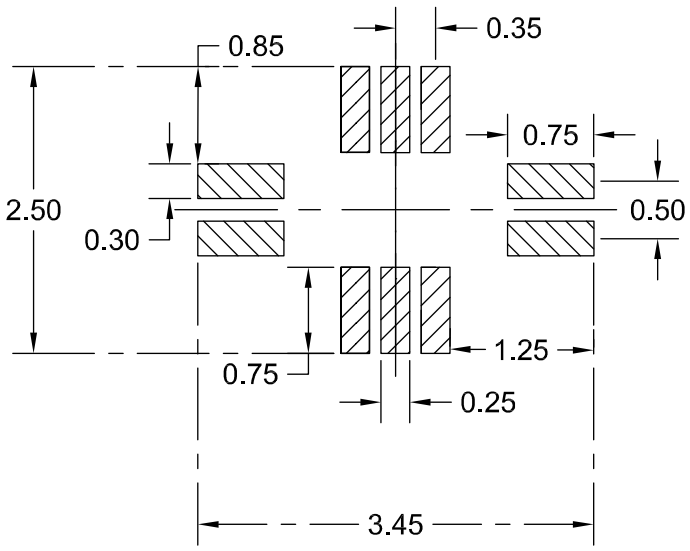


Table 6. **QFN10 (2 x 3 mm) mechanical data**

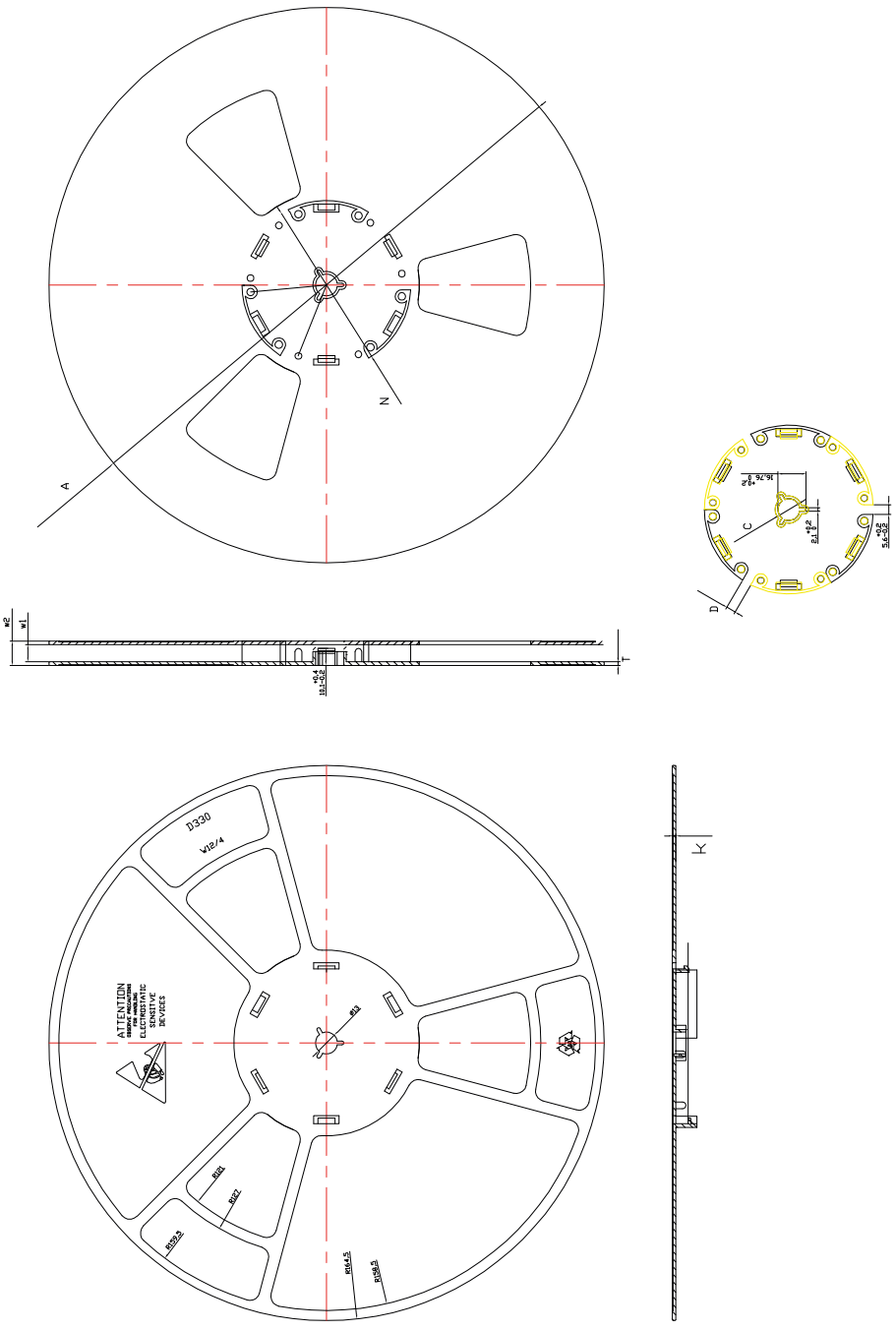
Dim.	mm		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.203 ref.	
b1	0.10	0.15	0.20
b2	0.15	0.20	0.25
D		3.00 BSC	
E		2.00 BSC	
e1		0.35 BSC	
e2		0.50 BSC	
L	0.30	0.40	0.50
aaa		0.05	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

Figure 25. **QFN10 (2 x 3 mm) recommended footprint**



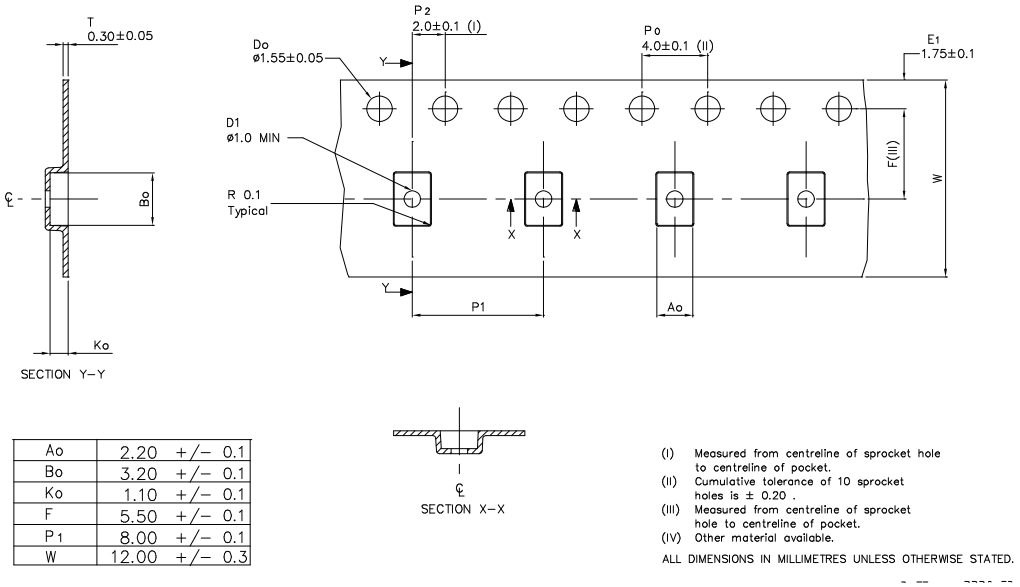
8.2 QFN10 (2 x 3 mm) packing information

Figure 26. **QFN10 (2 x 3 mm) reel drawing**



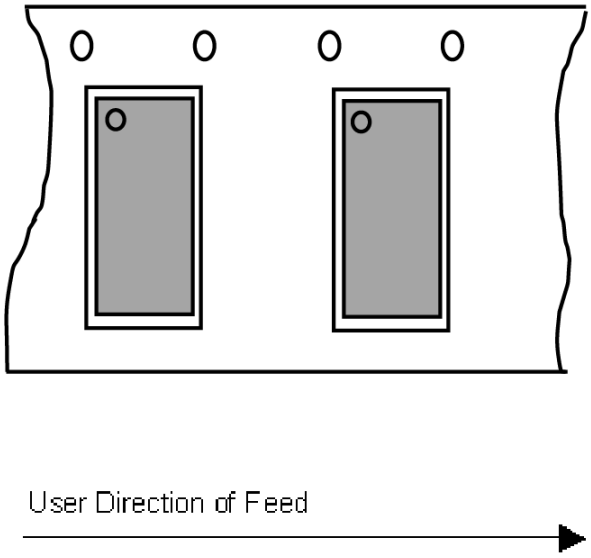
TYPE	A	N	C	D	w1	w2	T	k
12MM	ø330 +2 −2	ø100 +2 −2	ø13,1 +0,2 −0,2	5,6 +0,5 −0,5	12,4 +2 −0	16,6 +2 −0	2,1±0,15	1.4 +0,15 −0,1

Figure 27. **QFN10 (2 x 3 mm) reel drawing**



Ao	2.20	+/–	0.1
Bo	3.20	+/–	0.1
Ko	1.10	+/–	0.1
F	5.50	+/–	0.1
P1	8.00	+/–	0.1
W	12.00	+/–	0.3

Figure 28. **QFN10 (2 x 3 mm) tape oriented**



9 Ordering information

Table 7. **Order codes**

Order code	Package	Current limit configuration	Marking
STEF512PUR	QFN10	3 A on 5 V , 4 A on 12 V	W51

Revision history

Table 8. **Document revision history**

Date	Revision	Changes
07-Jan-2020	1	Initial release.
13-Jan-2020	2	Added A_{I_5} and A_{I_12} Min. and Max. values in Table 4. Electrical characteristics.
21-Sep-2020	3	Updated ILIM_5 Min. value in Table 4. Electrical characteristics. Minor text changes.
04-Apr-2023	4	Added Section 8.2 QFN10 (2 x 3 mm) packing information.
04-Apr-2024	5	Updated footnote in Table 2. Added Section 6.5: Application guidelines.

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