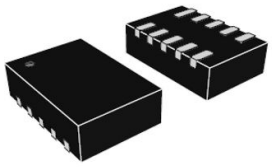
STEF512SRI

Datasheet

Dual electronic fuse for 5 V and 12 V rails with reverse current blocking



DFN10 (2 x 3 mm)

Maturity status link
STEF512SRI

Features

- 5 V and 12 V channels in one chip
- 23.5 V absolute maximum input voltage
- Precise output overvoltage clamp
- Fixed overcurrent protection for both channels
- Reverse current protection on 5 V channel
- Current monitor output in a single pin for both rails
- Current monitor pin selection
- Thermal protection
- Auto-retry after fault
- Input undervoltage lockout
- Integrated 45 mΩ power MOSFETs
- SAS-disable pin
- SATA ignore function
- DFN10 (2x3 mm) package

Applications

- HD and SSD
- Hard disk arrays and NAS
- Hot-swap, hot-plug protection

Description

The STEF512SRI is an integrated dual electronic fuse, designed to protect circuitry on the output from overcurrent and overvoltage events, in those applications requiring hot-swap operation and in-rush current control.

The device embeds two electronic fuses, one for the 5 V rail and one for the 12 V rail. Thanks to the very low ON-resistance of the integrated power MOSFETs, the voltage drop from the main supply to the load is very low during normal operation.

The 5 V channel provides a reverse blocking feature, preventing current flow to the input in case of brown-out or shutdown.

Startup time is internally controlled by a dedicated slew-rate circuit. In this way, the in-rush current at startup can be kept under control.

The maximum load current is precisely limited, by utilizing a sense FET topology, to factory-defined values.

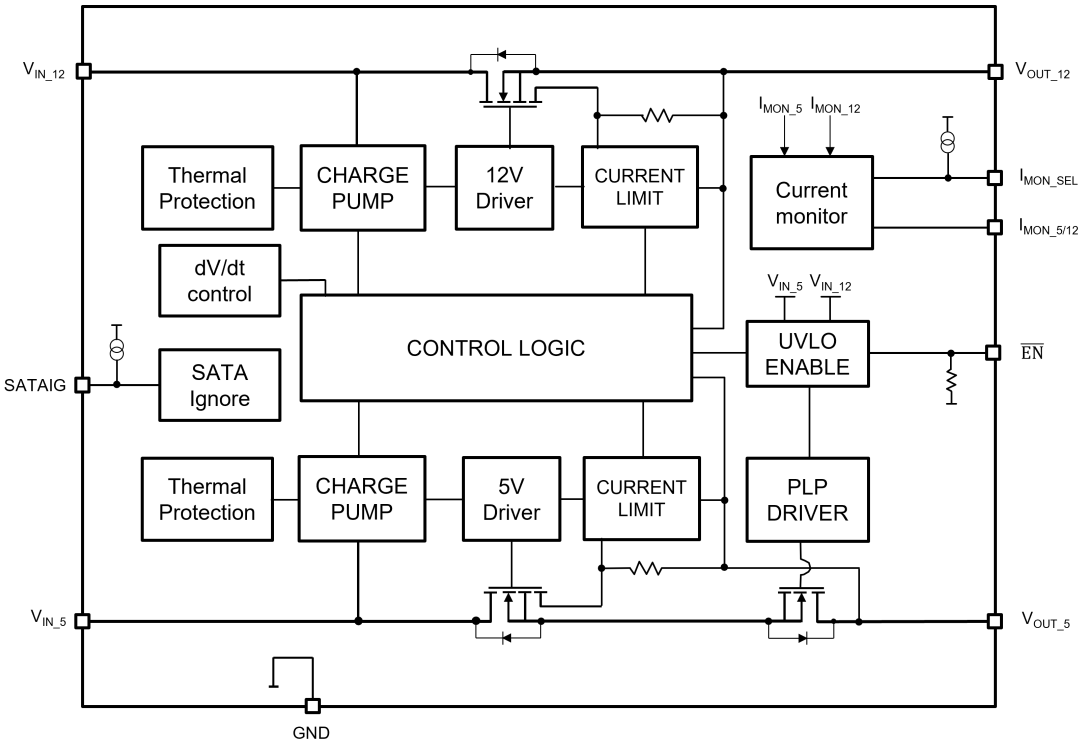
The device also provides precise overvoltage clamp for each channel, preventing the load from being damaged by power supply failures, and Undervoltage Lockout (UVLO), assuring that the input voltage is above the minimum operating threshold before the power device is turned on.

When an overload condition occurs, the STEF512SRI limits the output current to the predefined safe value. If the anomalous overload condition persists, the device goes into thermal shutdown, the internal switch opens, and the load is disconnected from the power supply. The load current on each channel can be precisely monitored by reading the signal on the IMON_5/12 pin.

The device features a SATA ignore pin (SATAIG) that can be used to simplify compatibility among SAS/SATA interfaces.

1 Diagram

Figure 1. **Block diagram**



2 Pin configuration

Figure 2. **Pin connection (marking view)**

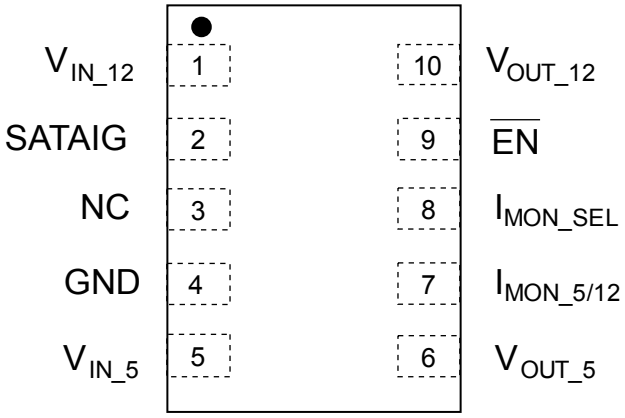


Table 1. **Pin description**

Pin #	Symbol	Function
1	V_{IN_12}	12 V rail supply voltage.
2	SATAIG	SATA ignore pin. This pin must be driven by an open-drain circuit. If left floating, the SAS-disable signal ($\overline{EN}$ pin signal) is used. If set low, it is ignored. This pin is internally pulled-up to 1.8 V via an internal current generator. Please refer to Section 6.3.
3	NC	Reserved. Leave this pin floating or connect it to GND.
4	GND	Ground
5	V_{IN_5}	5 V rail supply voltage.
6	V_{OUT_5}	5 V rail output voltage.
7	$I_{MON\_5/12}$	Current monitoring output for 5 V or 12 V rail.
8	I_{MON_SEL}	Current monitoring selection pin. This pin must be driven by an open-drain circuit. This pin is pulled up to 1.8 V via an internal current generator, so by default the I_{MON_12} signal is shown on pin 7. If connected to GND, pin 7 shows the I_{MON_5} value. Refer to Section 6.5.
9	$\overline{EN}$	SAS-disable input: set this pin logic-low to turn on the device, high to turn off the device. This pin is internally pulled down to GND via a 3.3 MΩ resistor.
10	V_{OUT_12}	12 V rail output voltage.

3 Typical application circuit

Figure 3. **Typical application circuit**

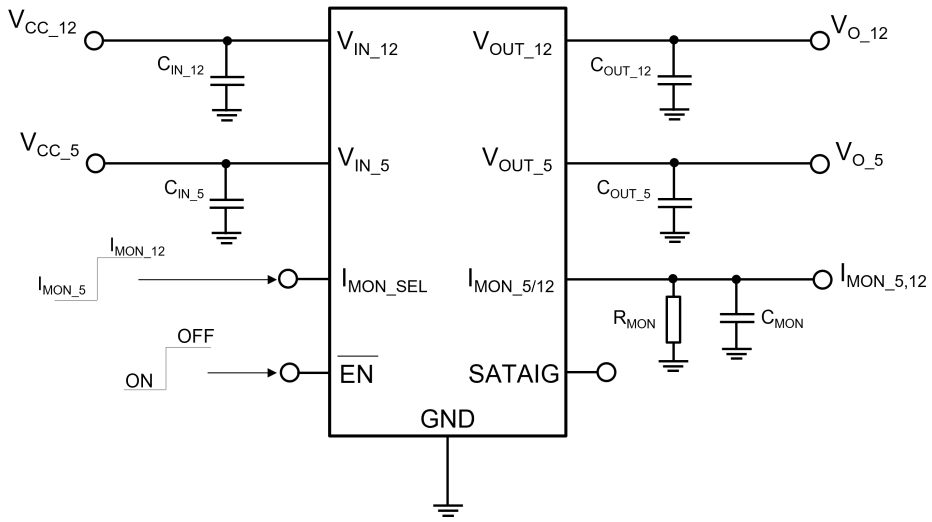


Table 2. **Recommended application components**

Symbol	Description	Min.	Typ.	Max.	Unit
C_{IN_12}	Input capacitor 12 V rail	1	10		µF
C_{IN_5}	Input capacitor 5 V rail	1	10		µF
C_{OUT_12}	Output capacitor 12 V rail	10	47		µF
C_{OUT_5}	Output capacitor 5 V rail	10	47		µF
C_{MON_x}	Current monitor pin filter capacitor	1	10		nF
R_{MON_x}	Current monitor pin resistor		10		kΩ

4 Maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{IN_5}	5 V supply voltage	-0.3 to 23.5	V
	Negative transient tolerance (<1 ms)	-3	V
V_{IN_12}	12 V supply voltage	-0.3 to 23.5	V
	Negative transient tolerance (<1 ms)	-3	V
V_{OUT_5}	5 V output voltage	-0.3 to 7	V
V_{OUT_12}	12 V output voltage	-0.3 to V_{IN} + 0.3 (18 V max.)	V
V_{SATAIG}	SATA ignore pin voltage	-0.3 to 4	V
$I_{MON\_5,12}$	Current monitor pin voltage	-0.3 to 7	A
I_{OUT_5}, I_{OUT_12}	Continuous output current, 5 and 12 V channels	Internally limited	A
$V_{\overline{EN}}$	Enable pin voltage	-0.3 to 7	V
I_{MON_SEL}	Current monitor selection pin voltage	-0.3 to 4	V
$T_{J\text{-}OP}$	Operating junction temperature range (1)	-40 to 125	°C
T_{STG}	Storage temperature range	-55 to 150	°C

1. *The thermal limit is set above the maximum thermal rating. It is not recommended to operate the device at temperatures greater than the maximum ratings for extended periods of time.*

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Exposure to absolute maximum rating conditions may affect device reliability. All values are referred to GND.

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient (1)	82	°C/W
R_{thJC}	Thermal resistance junction-case	12	°C/W

1. *Based on JESD51-7, 4-layer PCB.*

Table 5. ESD performance

Symbol	Parameter	Test conditions	Value	Unit
ESD	ESD performance	HBM	2	kV
		CDM	500	V

5 Electrical characteristics

T_J = 25 °C, V_{IN_5} = 5 V, V_{IN_12} = 12 V, $V_{\overline{EN}}$ = 0 V, V_{SATAIG} = floating, C_{IN_5} = C_{IN_12} = 1 µF, C_{OUT_5} = C_{OUT_12} = 10 µF, unless otherwise specified.

Table 6. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
5 V eFuse						
V_{IN_5}	Operating input voltage		4.5		V_{Clamp_5}	V
V_{Clamp_5}	Average output clamping voltage	V_{IN_5} = 8 V	5.5	5.7	5.9	V
V_{UVLO_5}	Undervoltage lockout	Turn-on, voltage rising	3.9	4.0	4.1	V
		Hysteresis		300		mV
R_{DSon_5}	ON-resistance	T_J = 25 °C, I_{OUT_5} = 500 mA		45		mΩ
		T_J = 125 °C (1)			70	
I_{L_5}	Off-state leakage current	$V_{\overline{EN}}$ = 5 V, V_{OUT_5} = GND			1	µA
I_{PLP_5}	Power loss protection reverse leakage current	$V_{\overline{EN}}$ = 0 V, V_{OUT_5} = 5 V, V_{IN_5} < V_{UVLO_5}		1		µA
T_{PLP}	Power loss protection intervention time (2)	$V_{\overline{EN}}$ = 0 V, V_{OUT_5} = 5 V, V_{IN_5} < V_{UVLO_5}, I_{PLP_5} < 1 µA (refer to Section 6.7)		600		ns
I_{TRIP_5}	Overcurrent trip point (2)			3.7		A
I_{HOLD_5}	Overload current limit	V_{OUT_5} > 2.5 V	2.9	3.1	3.3	A
I_{SHORT_5}	Short-circuit current (2)	V_{OUT_5} < 2.5 V		1.85		A
A_{I_5}	Current monitor output current gain I_{MON_5} / I_{OUT_5}	I_{OUT_5} ≥ 100 mA	27.5	30	32.5	µA/A
$dV/dt_{\_5}$	Output voltage ramp time	From 10 % to 90 % of V_{OUT_5}	10	13	16	ms
12 V eFuse						
V_{IN_12}	Operating input voltage		10.5		V_{Clamp_12}	V
V_{Clamp_12}	Average output clamping voltage	V_{IN_12} = 18 V	14.5	15	15.5	V
V_{UVLO_12}	Undervoltage lockout	Turn-on, V_{IN_12} rising	7.7	8.5	9.3	V
		Hysteresis		800		mV
R_{DSon_12}	ON-resistance	T_J = 25 °C, I_{OUT_12} = 500 mA		40		mΩ
		T_J = 125 °C (1)			70	
I_{L_12}	Off-state leakage current	$V_{\overline{EN}}$ = 5 V, V_{OUT_12} = GND			3	µA
I_{TRIP_12}	Overcurrent trip point (2)			3.9		A
I_{HOLD_12}	Overload current limit	V_{OUT_12} > 7.5 V	2.9	3.1	3.3	A
I_{SHORT_12}	Short-circuit current (2)	V_{OUT_12} < 7.5 V		1.85		A
A_{I_12}	Current monitor gain I_{MON_5} / I_{OUT_5}	I_{OUT_12} ≥ 100 mA	27.5	30	32.5	µA/A
$dV/dt_{\_12}$	Output voltage ramp time	From 10 % to 90 % of V_{OUT_12}	10	13	16	ms

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Common features						
V_{IL}	Low level input voltage, $\overline{EN}$ pin	eFuse outputs enabled			0.7	V
V_{IH}	High level input voltage, $\overline{EN}$ pin	eFuse outputs disabled	1.7			V
$R_{\overline{EN}}$	Pull-down resistor on $\overline{EN}$ pin	Connected to GND		3.3		MΩ
$I_{\overline{EN}}$	$\overline{EN}$ pin consumption	$V_{\overline{EN}}$ = 5 V		1.5		µA
V_{IL_IMSL}	I_{MON_SEL} low level input voltage	$I_{MON\_5/12}$ pin outputs I_{MON_5}			0.4	V
V_{IH_IMSL}	I_{MON_SEL} high level input voltage	$I_{MON\_5/12}$ pin outputs I_{MON_12}	1.2			V
V_{IMSL}	I_{MON_SEL} pin pull-up voltage			1.8		V
I_{IMSL}	I_{MON_SEL} pin pull-up current generator	I_{MON_SEL} pin to GND		5		µA
V_{IL_SATAIG}	SATA ignore low level input voltage	SAS pin signal ignored			0.4	V
V_{IH_SATAIG}	SATA ignore high level input voltage	SAS pin signal active	1.2			V
V_{SATAIG}	SATA ignore pin pull-up voltage			1.8		V
I_{SATAIG}	SAS ignore pin pull-up current generator	SATAIG pin to GND		5		µA
T_{DELAY}	Delay time (2)	From $\overline{EN}$ set to low state to soft-start ramp beginning		500		µs
I_q	Quiescent current (GND)	Device operating, no load		400	600	µA
		Off-state, $V_{\overline{EN}}$ = 5 V		150		µA
Thermal protection						
TSD (2)	Shutdown temperature			165		°C
	Hysteresis			30		

1. *Values across temperature range are guaranteed by design/correlation and tested in production only at ambient temperature.*
2. *Guaranteed by design, but not tested in production.*

6 Device functional description

The STEF512SRI embeds a 5 V and a 12 V electronic fuses (eFuses). Each eFuse can limit the voltage or the current during fault events, such as input overvoltage or output overload, respectively. For this purpose, it contains 2 hysteretic control loops, one for limiting the output voltage and the other for limiting the input current.

The current limiting loop is also used during the startup phase of the eFuse to limit the in-rush current into the output capacitor.

During normal operation the eFuse behaves as a low-resistance Power FET, therefore the output voltage follows the input one. In case of an overvoltage or overcurrent event, the eFuse limits the VGS of the internal FET, to clamp the output voltage or current respectively. During such events the die temperature increases due to the power dissipation and so, if the fault persists and the overtemperature threshold is overcome, the device goes into thermal shutdown, the internal FET is turned off and the load disconnected from the power supply.

Each eFuse provides factory-trimmed undervoltage lockout and output voltage rise time.

The power stage of the 5 V channel consists of 2 MOSFETS connected in a back-to-back configuration. This configuration is used to perform the reverse current blocking feature in case of input power loss.

The current flowing into each eFuse is continuously sensed through a dedicated copy-MOS and feed to the current monitor circuit. The current monitor signal generated by this circuit is provided on a single I_{MON} pin, which outputs either the 5 V or the 12 V channel depending on the logic status of the I_{MON} selection pin (I_{MON_SEL}).

6.1 Undervoltage lockout

The undervoltage lockout circuit prevents each eFuse from turning on if the supply voltage is below the UVLO rising threshold. During operation, if the input voltage of one channel falls below (V_{UVLO_x} - V_{Hyst_x}), the outputs of both channels are turned off simultaneously.

6.2 Startup sequence and voltage clamp

The typical startup sequence of the eFuse, when the SAS-ignore function is not used (SATAIG pin left floating), is described below and shown in Figure 4 and Figure 5:

- The power supply is connected to the VIN_x pins and both 5 V and 12 V input voltages are higher than the relevant undervoltage lockout threshold.
- The SATAIG pin is internally pulled up and latched once the internal regulator is active.
- The SAS-disable pin ($\overline{EN}$) is connected to GND or left floating by the user to enable the device.
- After an initial delay of 500 µs the eFuse starts ramping up the 5 and 12 V output voltages with a fixed slew-rate, to ensure a 13 ms (typ.) soft-start time and minimize the in-rush current.
- During the startup phase, the foldback current limit is disabled and the current limit is set to the I_{HOLD_x} value.
- If the input voltage continues rising, above the overvoltage threshold (V_{Clamp_x}), because of a failure in the power supply, the eFuse limits the output voltage to V_{Clamp_x}. The eFuse keeps operating in this state until the overtemperature threshold is reached and then it shuts down. The power MOSFET remains in an off-state until the die temperature drops by the overtemperature hysteresis, then the device automatically attempts to restart.

Figure 4. Typical startup sequence ($\overline{EN}$ toggled after V_{IN} rise)

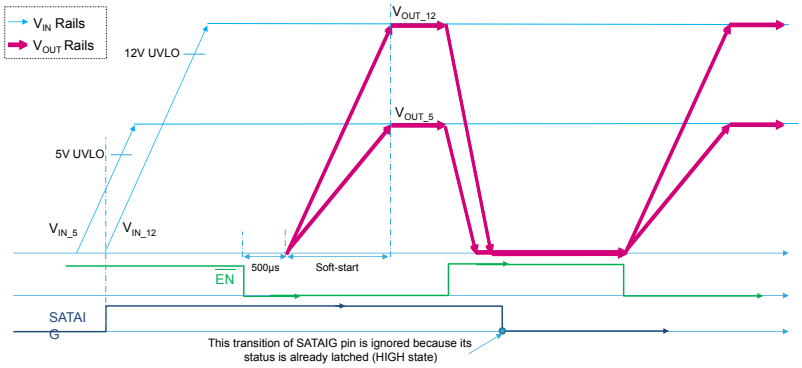
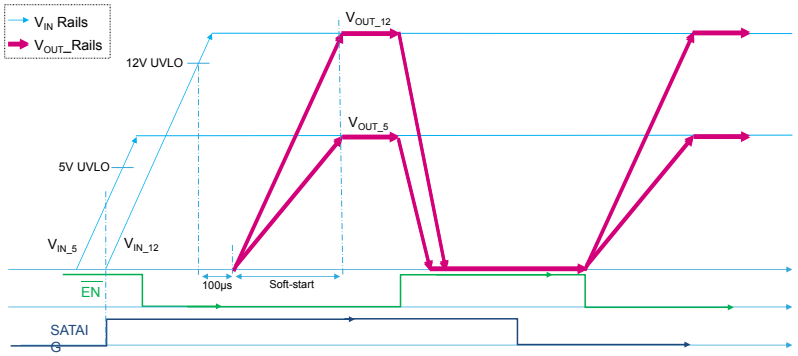


Figure 5. **Typical startup sequence ($\overline{EN}$ toggled during input voltage rise)**



6.3 Enable pin and SATA ignore function

The device provides an SAS-compliant chip disable pin ($\overline{EN}$). This pin is internally pulled down to GND via a 3.3 MΩ resistor. If the pin is left floating, the device outputs are turned on. Apply an external signal above V_{IH} to turn the device off.

Additionally, a SATA ignore logic can be activated via the SATAIG pin.

This function allows to configure the device for working on either SAS or SATA interfaces by propagating or ignoring the connector's SAS_DISABLE signal, usually connected to the $\overline{EN}$ pin.

We recommend driving the SATAIG pin via an open drain.

Internal pullup of the SATAIG pin is activated when at least one of the two input voltages has reached an internal threshold of around 3 V.

With reference to Figure 6 and Table 7, when SATAIG is left floating at startup, the SAS_DISABLE signal present on the $\overline{EN}$ pin is propagated to the eFuse and the internal SATA_ig latched signal is latched.

This means that the $\overline{EN}$ pin controls device startup and shutdown and any successive SATAIG toggling is ignored.

If SATAIG is connected to GND before power-up, the SAS_DISABLE signal is ignored, so as soon as the input voltage of both channels is higher than the UVLO thresholds, the device is turned on, regardless of the $\overline{EN}$ pin status.

Figure 6. **SATA ignore function simplified diagram**

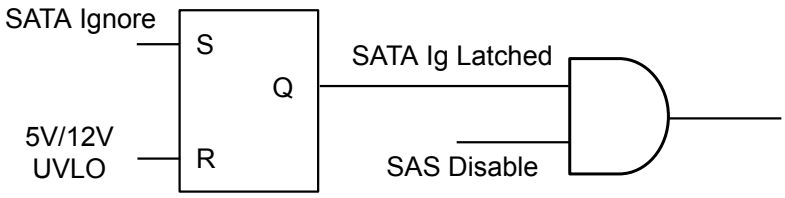


Table 7. **Enable/SATAIG pins truth table**

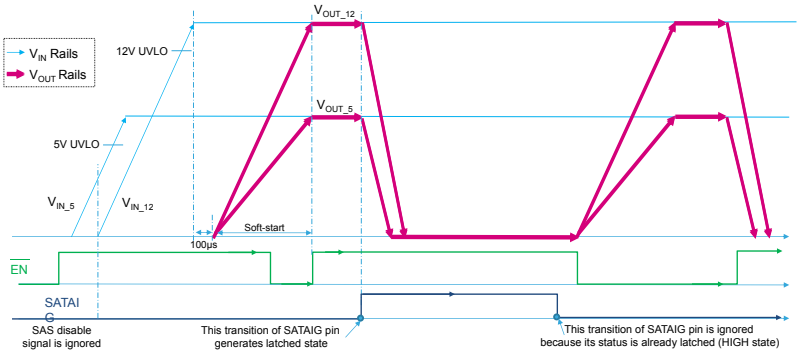
$\overline{EN}$	SATAIG	Device status
H	floating	Off
L or floating	floating	On
H	L	On
L or floating	L	On

The SATA_IG internal signal latch can be cleared only in case of a 5 V or 12 V UVLO event and it does not change by toggling the SAS-disable signal ($\overline{EN}$).

According to the above table and the internal pull-up configuration, if both $\overline{EN}$ and SATAIG pins are left floating, the device is in ON status.

A typical startup sequence in this configuration is shown Figure 7.

Figure 7. Startup sequence (SATAIG connected to GND at power-up)

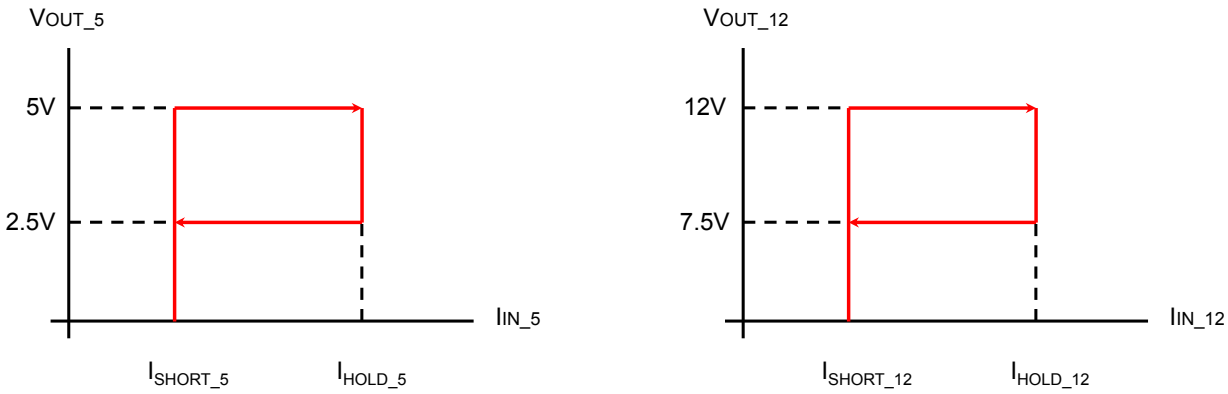


6.4 Current limit function after startup

Each eFuse provides 2 kinds of current limit protection mechanisms (see Figure 8):

- Operative current limit (I_{HOLD_x}) for both channels, active once the output voltage reaches the input voltage.
- Short-circuit current limit (I_{SHORT_x}) is applied when the output voltage falls below the short-circuit detection thresholds (2.5 V for the 5 V eFuse and 7.5 V for the 12 V eFuse).

Figure 8. Current limit function graphs



6.5 eFuse current monitor

Each channel is equipped with a current monitoring feature that allows the host processor to read the current flowing through the fuse. To use only one ADC, the $I_{MON\_5/12}$ pin is able to manage both outputs current information, thanks to a current monitoring selection pin (I_{MON_SEL}).

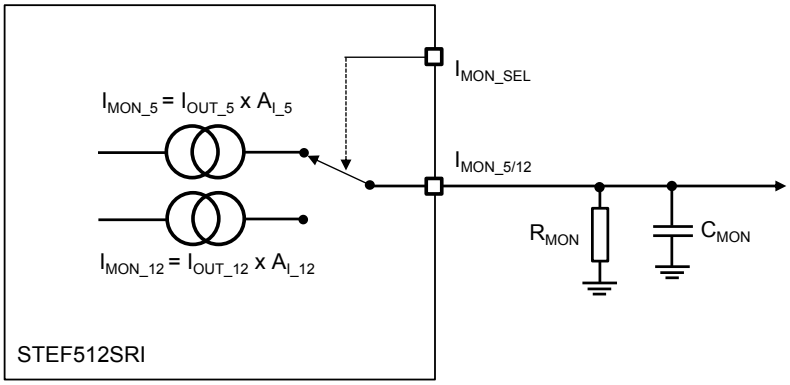
If I_{MON_SEL} is connected to GND, pin 7 outputs the I_{MON_5} signal. If it is left floating, pin 7 outputs the I_{MON_12} signal.

It is recommended to drive the I_{MON_SEL} pin via an open-drain circuit.

The I_{MON_x} signal is a current proportional to the relevant channel load current, by factor $A_{I\_x} = I_{MON\_x} / I_{OUT\_x}$.

This current is imposed on an external R_{MON_x}, converting the sensing current into voltage for further processing by the host system (see Figure 9).

Figure 9. **Current monitor simplified circuit**



The current monitoring circuit is also equipped with an internal clamp that limits the voltage on the pin at a static value of 1.8 V. Bypassing the pin to GND with a minimum C_{MON} of 1 nF is recommended as it avoids voltage spikes during fast output current transition.

6.6 Thermal shutdown

If the device temperature exceeds the thermal threshold, typically 165 °C, the thermal shutdown circuitry turns the power MOSFET off, thus disconnecting the load. The power MOSFET remains in an off-state until the die temperature drops below the hysteresis value. Once this happens, the internal auto-retry circuit attempts to reset the device.

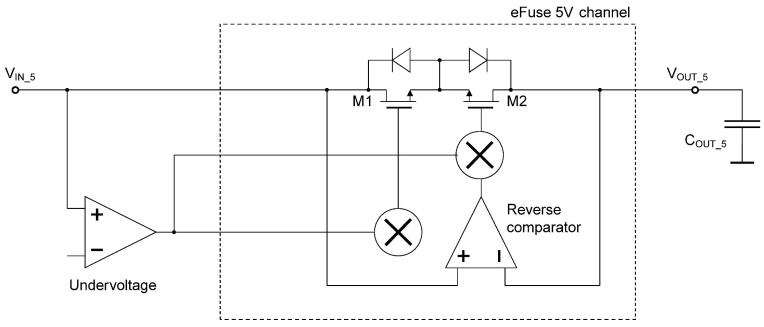
The device is also equipped with a differential thermal protection that avoids damage in case of fast thermal gradients inside the chip. When the differential thermal protection is activated, both channels are switched off. This protection works in auto-retry mode without soft-start phase.

6.7 Reverse current blocking feature on the 5 V channel

The 5 V eFuse contains a second power transistor (ISOFET) connected in a back-to-back configuration with the main one, to prevent significant current flowing back from the 5 V output into the 5 V input, in case of input short to ground, brown-out, or a deep input voltage glitch. The simplified structure is shown in Figure 10. The ISOFET is controlled by the UVLO circuit and by a reverse comparator, which continuously monitors the voltage difference between the V_{IN_5} and V_{OUT_5}.

As soon as the reverse comparator detects a significant negative voltage across the 5 V eFuse (typically 50 mV), the M2 transistor is immediately turned off. M2 can be turned back on only if the voltage drop across the eFuse has become zero (no negative current). However, in case of slow V_{IN_5} decay, the V_{OUT_5} voltage follows the V_{IN_5} because of the output capacitor being discharged through the eFuse into the V_{IN_5}, hence no significant negative voltage is generated across the eFuse. In that case the UVLO circuit serves as a “stop loss” feature, that is, the information from the reverse comparator is overridden by the V_{IN_5} undervoltage lockout and the M2 is forced to turn off. As soon as the UVLO threshold has been reached again, the eFuse restarts with normal soft-start cycle.

Figure 10. **5 V reverse current protection block diagram**



6.8 External capacitors and application suggestions

Input and output capacitors are mandatory to reduce the transient effects of stray inductances which may be present on the input and output power paths. In fact, when the STEF512SRI interrupts the current flow, input inductance generates a positive voltage spike on the input, and output inductance generates a negative voltage spike on the output. To reduce the effects of such transients, a C_{IN} capacitor of at least 1 µF (including derating effects) must be connected between the input pin and GND and located as close as possible to the device.

For the same reason, a C_{OUT} capacitor of at least 10 µF must be connected at the output port.

When the device is connected to the power supplies by means of long wires, whose inductance is higher than 1 µH, the input capacitor should be increased.

It is suggested to provide for additional protections and methods for addressing these transients, such as:

- Minimizing inductance of the input and output tracks
- TVS diodes on the input to absorb inductive spikes
- Schottky diode on the output to absorb negative spikes
- A combination of ceramic and electrolytic capacitors on the input and output.

7 Typical characteristics

The following plots refer to the typical application circuit with V_{CC_12} = 12 V, V_{CC_5} = 5 V, I_{OUT_12} = I_{OUT_5} = 0 A, SATA_IG floating, $\overline{EN}$ set to low state and unless otherwise noted, at T_A = 25 °C.

Figure 11. Quiescent current vs. temperature (ON mode)

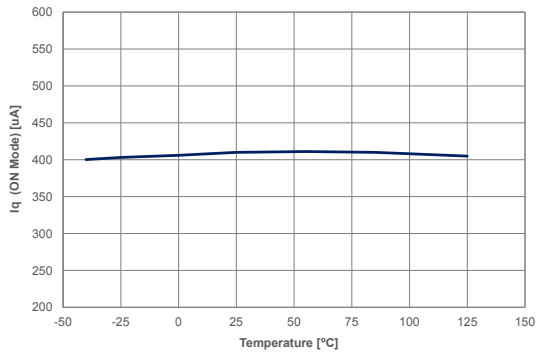


Figure 12. Quiescent current vs. temperature (OFF mode)

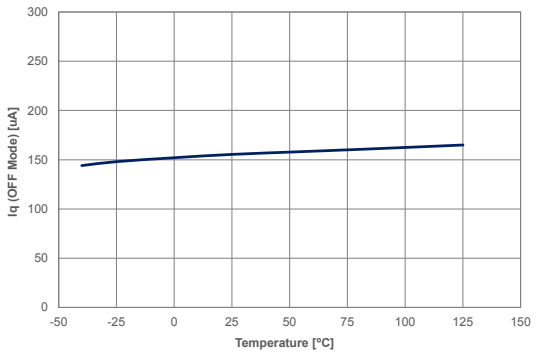


Figure 13. 12 V eFuse R_{DS_ON} vs. temperature

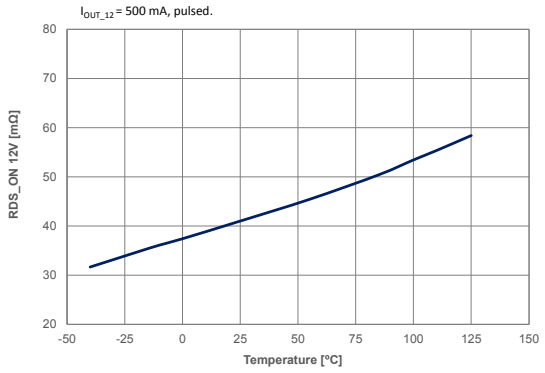


Figure 14. 5 V eFuse R_{DS_ON} vs. temperature

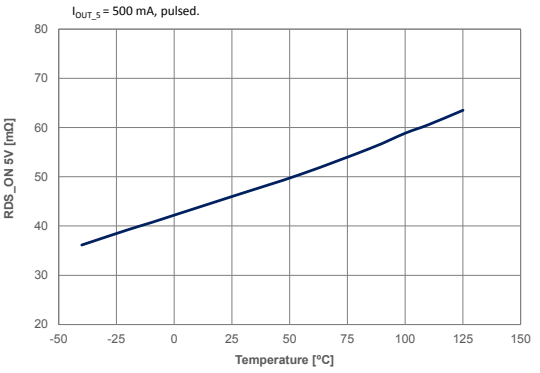


Figure 15. 12 V eFuse voltage clamp vs. temperature

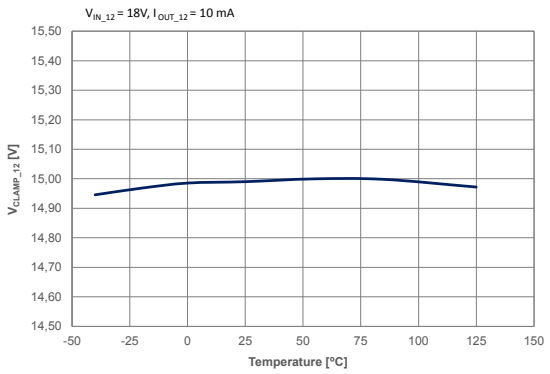


Figure 16. 5 V eFuse voltage clamp vs. temperature

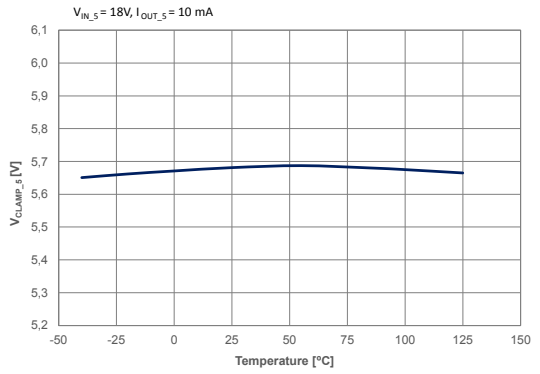


Figure 17. 12 V eFuse UVLO vs. temperature

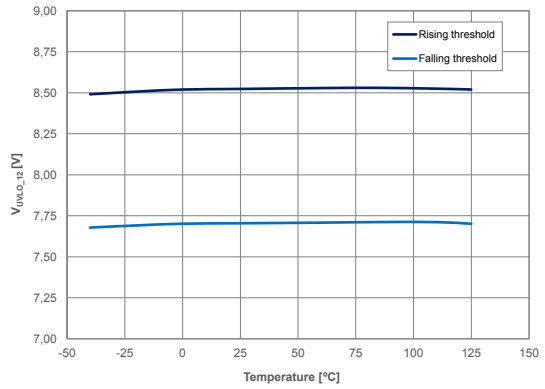


Figure 18. 5 V eFuse UVLO vs. temperature

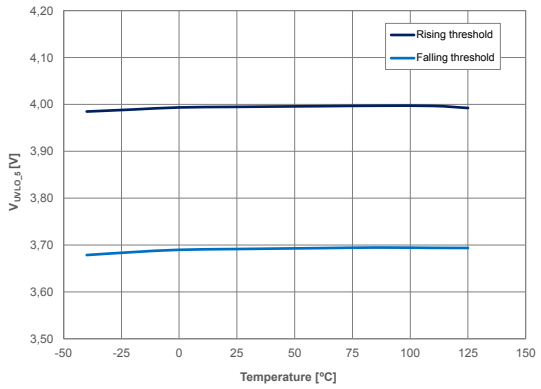


Figure 19. 12 V eFuse overload current limit vs. temperature

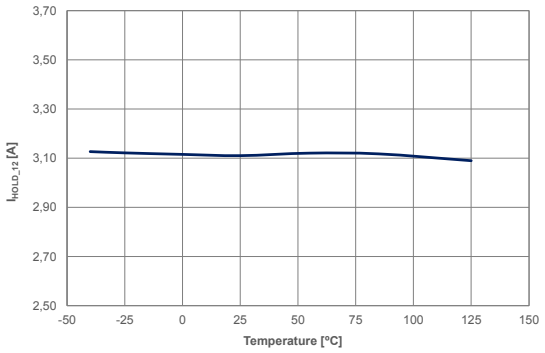


Figure 20. 5 V eFuse overload current limit vs. temperature

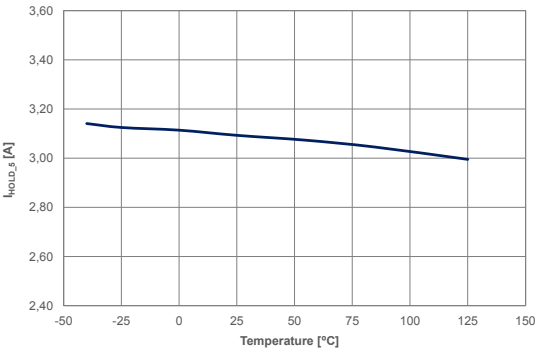


Figure 21. Soft-start time vs. temperature

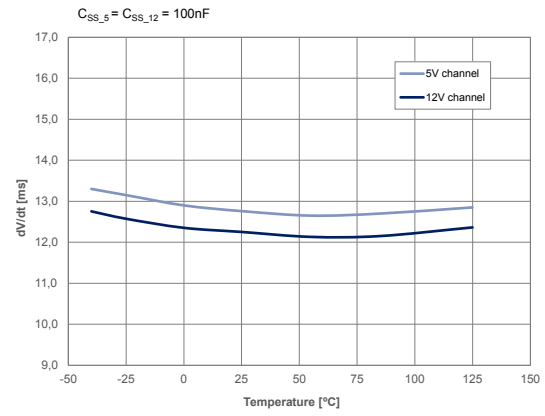


Figure 22. SAS disable pin threshold vs. temperature

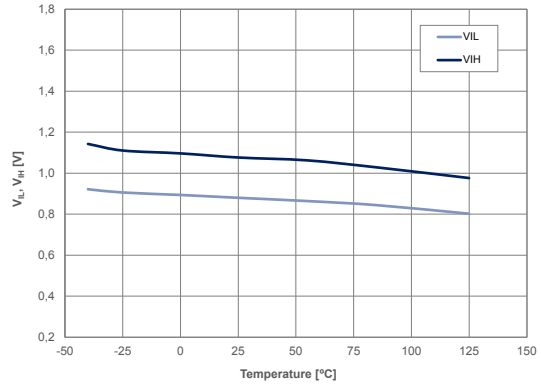


Figure 23. SATA ignore pin threshold vs. temperature

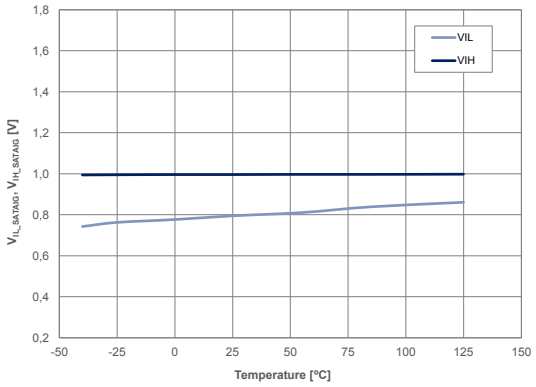


Figure 24. I_{MON_SEL} pin threshold vs. temperature

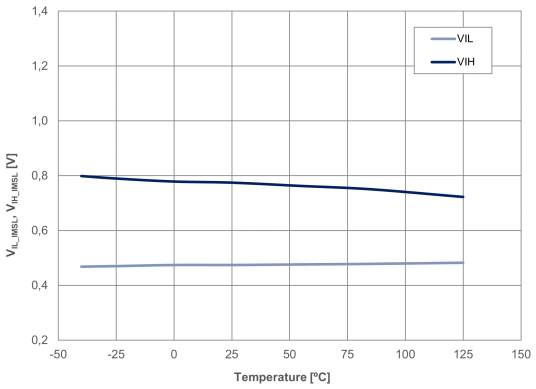


Figure 25. Current monitor gain vs. temperature

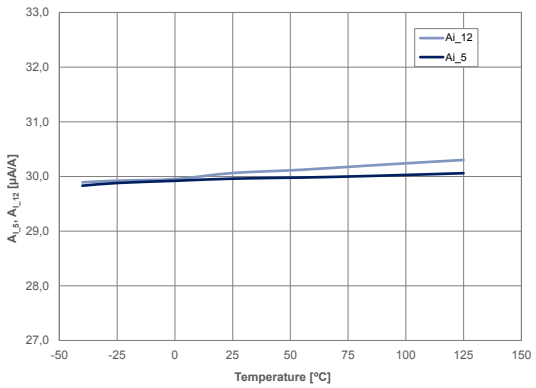


Figure 26. Current monitor gain vs. load current

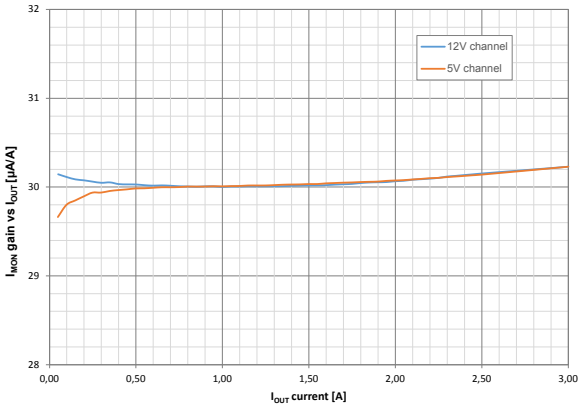


Figure 27. Startup via input voltage

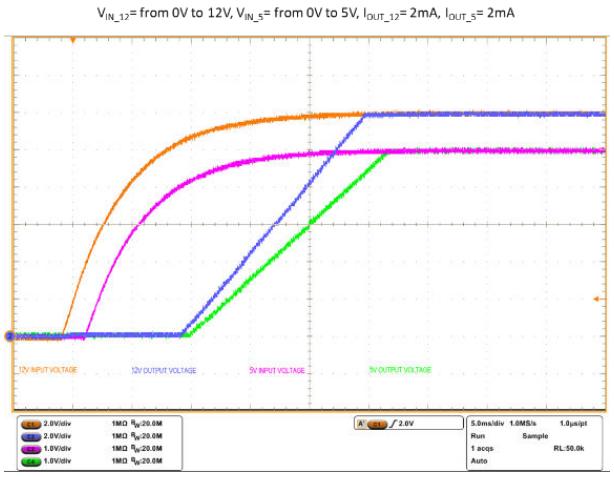


Figure 28. Startup via input voltage (hot-plug) 5 V

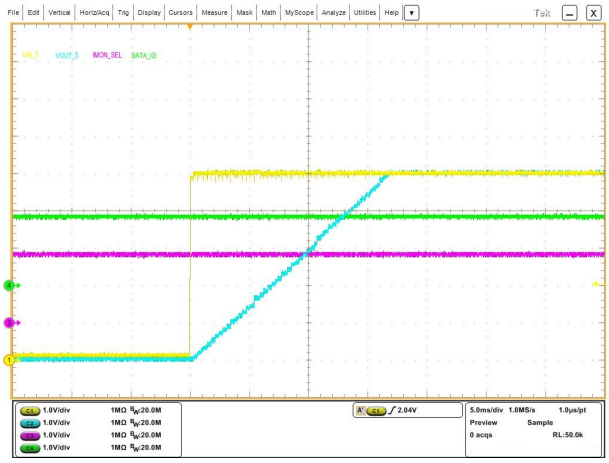


Figure 29. Startup via input voltage (hot-plug) 12 V

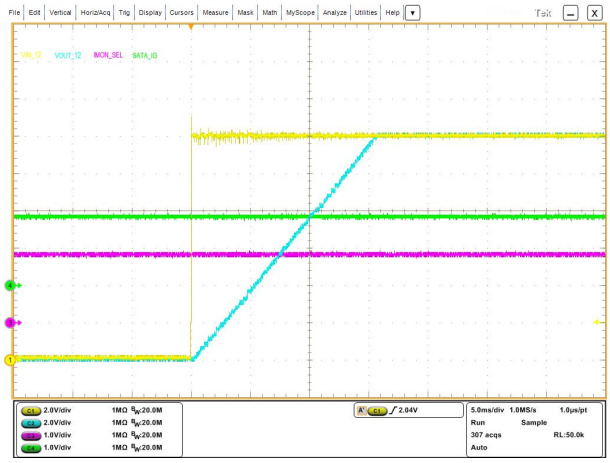


Figure 30. Startup via input voltage (hot-plug) 5 V & 12 V

V_{IN_12}= from 0V to 12V, V_{IN_5}= from 0V to 5V, I_{OUT_12}= 0mA, I_{OUT_5}= 0mA

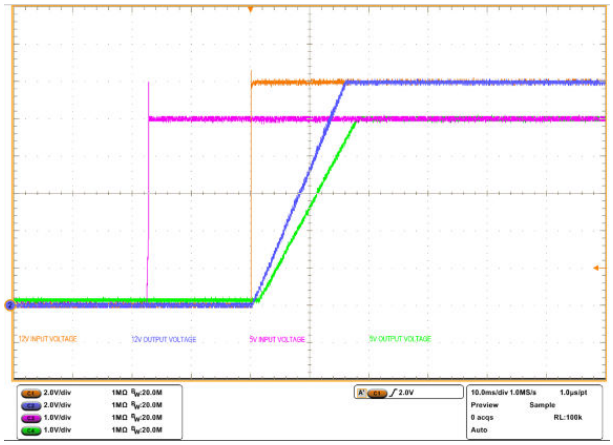


Figure 31. Startup via EN_N signal

V_{IN_12}= 12V, V_{IN_5}= 5V, V_{EN_N}= from 3.3V to 0V, I_{OUT_12}= 0mA, I_{OUT_5}= 0mA

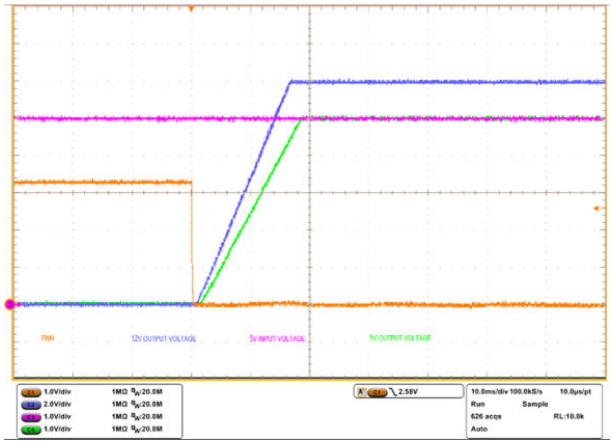


Figure 32. Shutdown via EN_N signal

V_{IN_12}= 12V, V_{IN_5}= 5V, V_{EN_N}= from 0V to 3.3V , trise=1µs, I_{OUT_12}= 200mA, I_{OUT_5}= 0mA

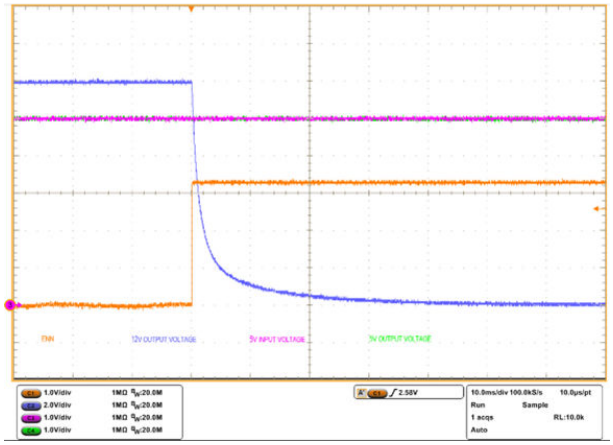


Figure 33. Startup into voltage clamp (5 V eFuse)

V_{IN_12}= from 0V to 12V, V_{IN_5}= from 0V to 12V, I_{OUT_12}= 0mA, I_{OUT_5}= 100mA

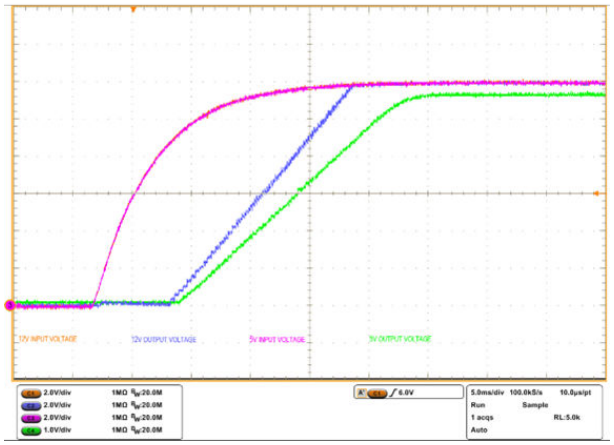


Figure 34. Startup into voltage clamp (12 V eFuse)

V_{IN_12}= from 0V to 18V, V_{IN_5}= 5V, I_{OUT_12}= 100mA, I_{OUT_5}= 0mA, trise=10µs

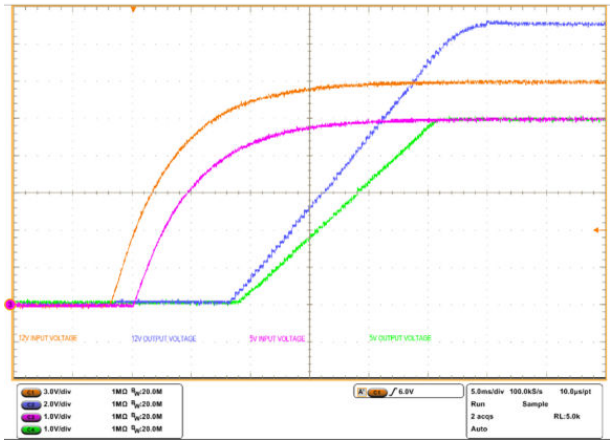


Figure 35. Voltage clamp during operation (5 V eFuse)

V_{IN_12}= 12V, V_{IN_5}= from 5V to 8V, I_{OUT_12}= 0mA, I_{OUT_5}= 400mA

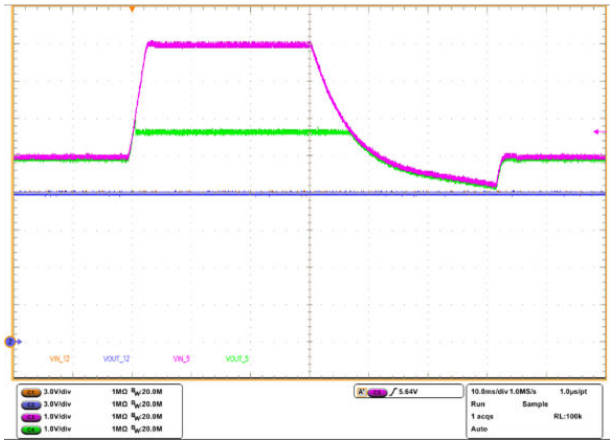


Figure 36. Voltage clamp during operation (12 V eFuse)

V_{IN_12}= from 12V to 18V, V_{IN_5}= 5V, I_{OUT_12}= 400mA, I_{OUT_5}= 0mA

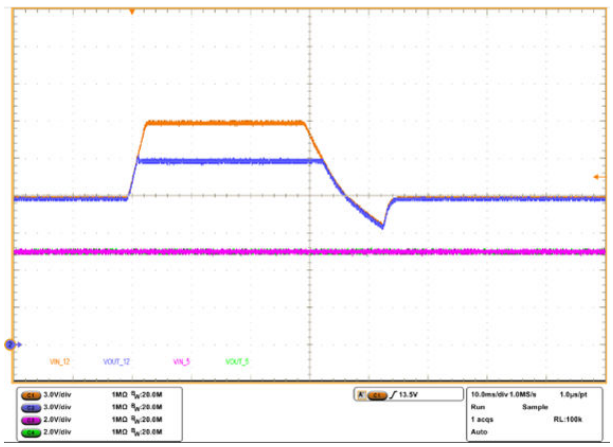


Figure 37. Startup into output short-circuit via EN_N (5 V eFuse)

V_{IN_12}= 12V, V_{IN_5}= 5V, I_{OUT_12}= 0mA, V_{OUT_5}= shorted to GND

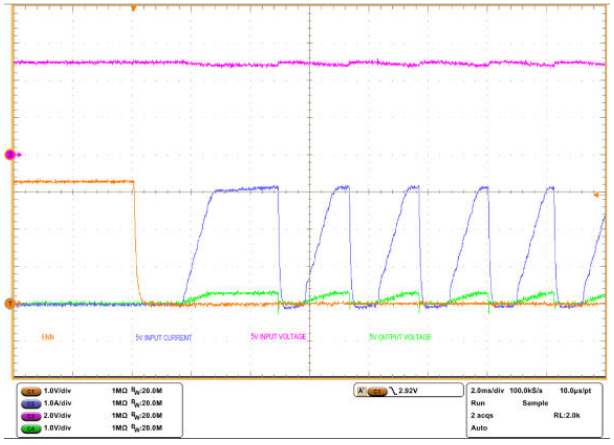


Figure 38. Startup into output short-circuit by EN_N (12 V eFuse)

V_{IN_12}= 12V, V_{IN_5}= 5V, I_{OUT_5}= 0mA, V_{OUT_12}= shorted to GND

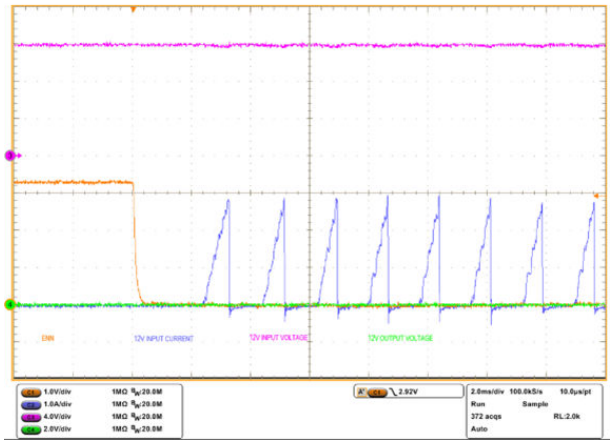


Figure 39. Startup into overload (5 V eFuse)

V_{IN_12}= from 0V to 12V, V_{IN_5}= from 0V to 5V, R_{OUT_5}= 1Ω, I_{OUT_12}= 0mA

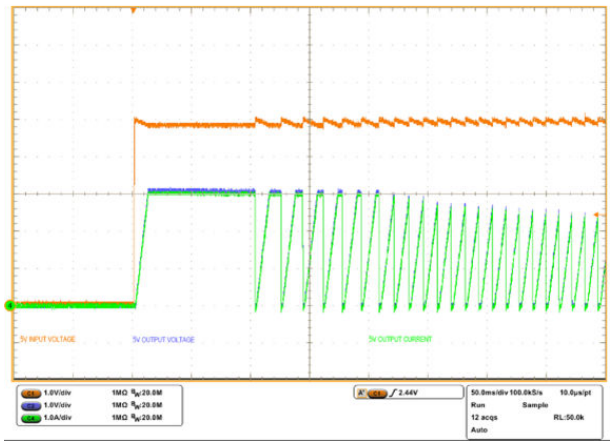


Figure 40. Startup into overload (12 V eFuse)

V_{IN_12}= from 0V to 12V, V_{IN_5}= from 0V to 5V, R_{OUT_12}= 2.2Ω, I_{OUT_5}= 0mA

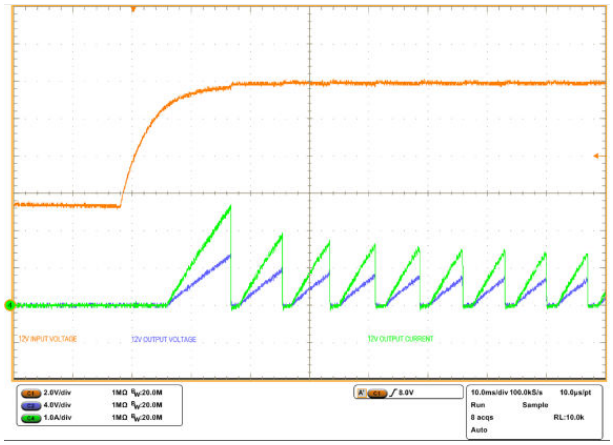


Figure 41. Overcurrent protection (5 V eFuse)

V_{IN_12}= 12V, V_{IN_5}= 5V, I_{OUT_12}= 2A, I_{OUT_5}= from 0 mA to current limit (constant voltage load)

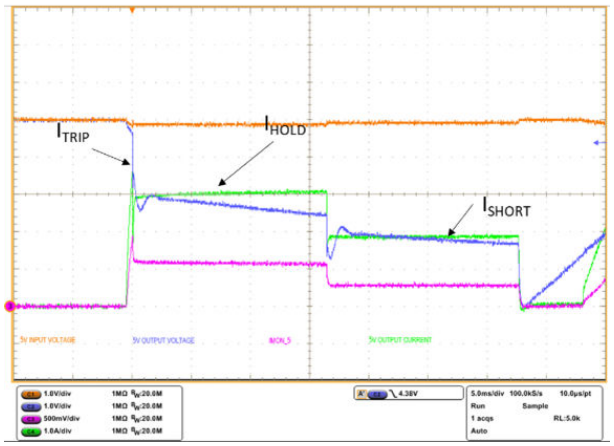


Figure 42. Overcurrent protection (12 V eFuse)

V_{IN_12}= 12V, V_{IN_5}= 5V, I_{OUT_5}= 1A, I_{OUT_12}= from 0 mA to current limit (constant voltage load)

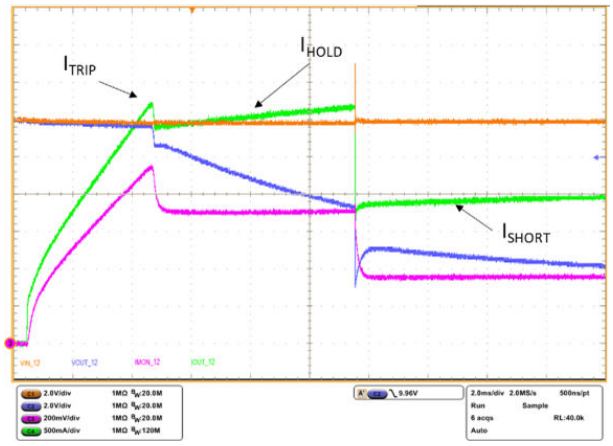


Figure 43. Power loss protection via UVLO_5

V_{IN_12}= 12V, V_{IN_5}= from 5V to floating, I_{OUT_12}= 0mA, I_{OUT_5}= 1 A

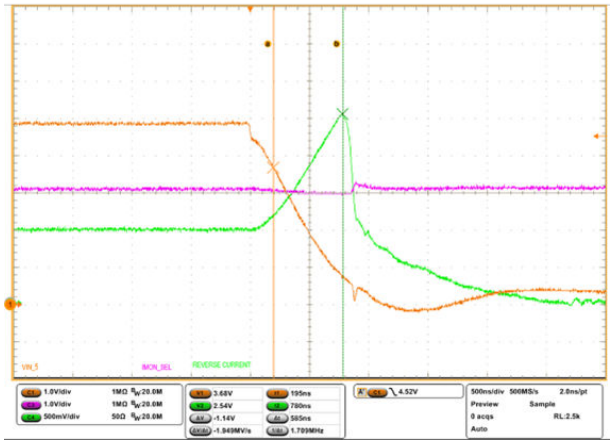


Figure 44. Current monitor response time to load step

I_{out_12}= 1A to 2A and back, R_{IMON}= 10kΩ and C_{IMON}= 10nF

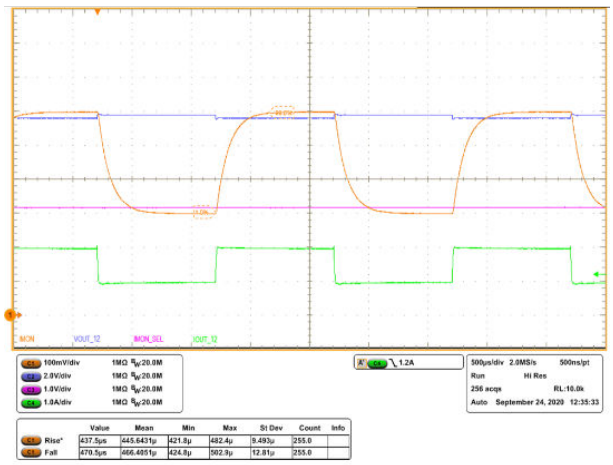
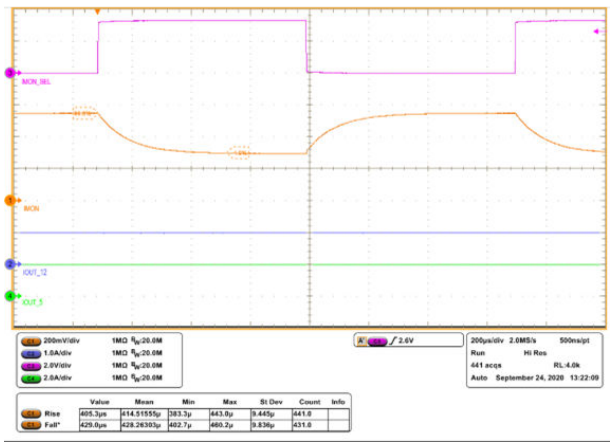


Figure 45. Current monitor response time to channel switch via I_{MON_SEL}

I_{out_12}= 1A, I_{out_5}= 2A, R_{IMON}= 10kΩ and C_{IMON}= 10nF



8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

8.1 DFN10 (2 x 3 mm) package information

Figure 46. DFN10 (2 x 3 mm) package outline

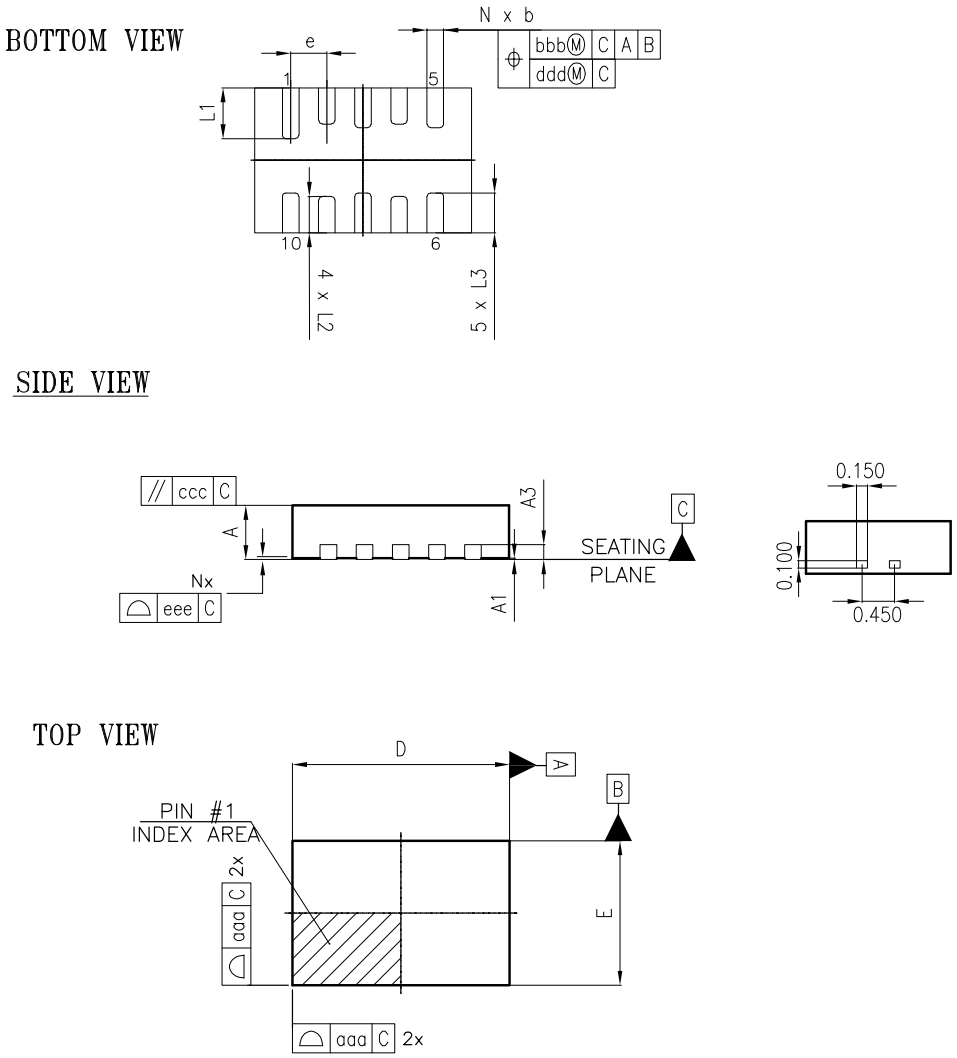
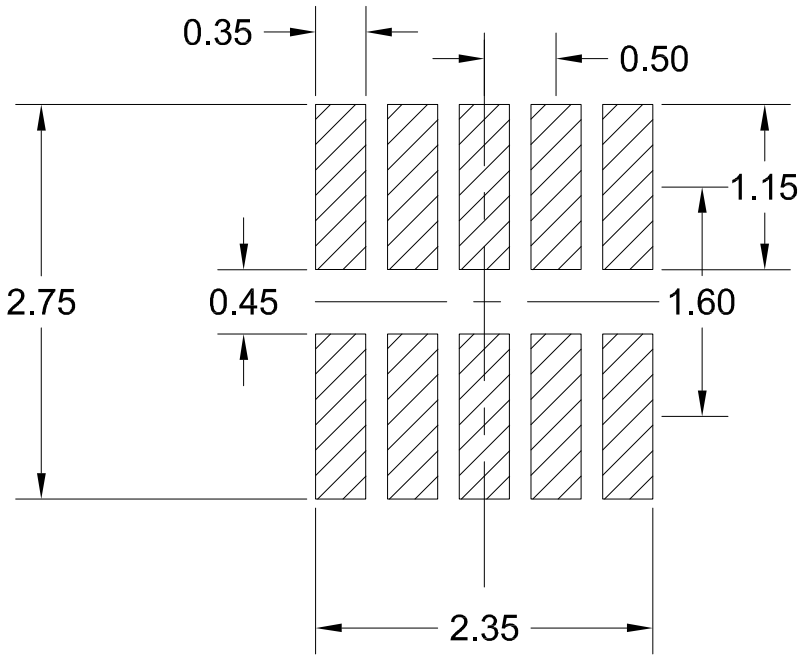


Table 8. **DFN10 (2 x 3 mm) mechanical data**

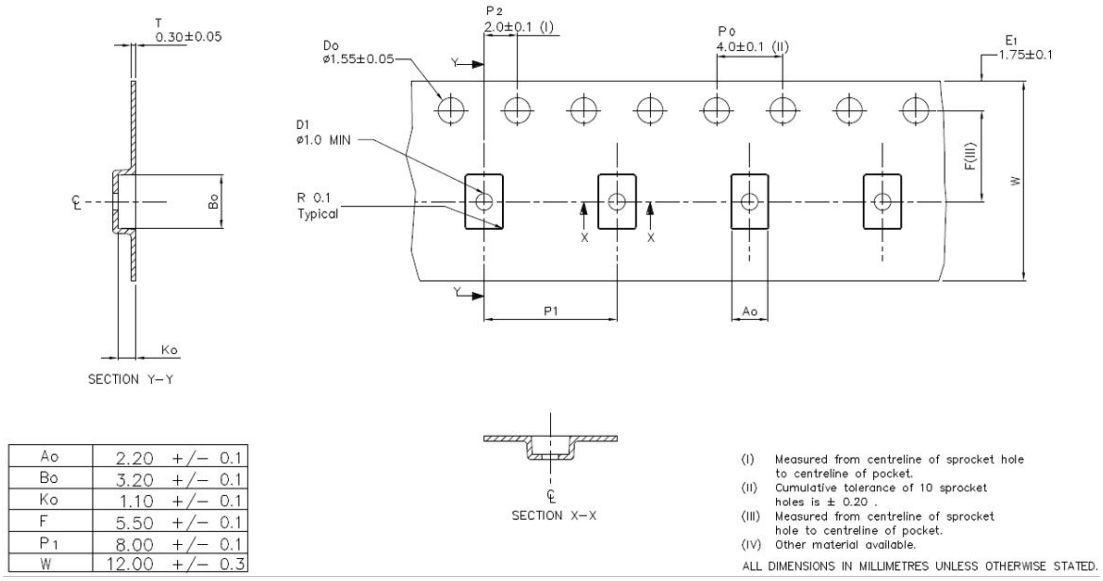
Dim.	mm		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 ref.	
b	0.180	0.230	0.280
D		3.00 BSC	
e		0.50 BSC	
E		2.00 BCS	
L1	0.60	0.70	0.80
L2	0.40	0.50	0.60
L3	0.45	0.55	0.65
K	0.20		
N		10	
aaa		0.05	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

Figure 47. **DFN10 (2 x 3 mm) recommended footprint**



8.2 Carrier tape information

Figure 48. **Carrier tape information**



Ao	2.20 +/– 0.1
Bo	3.20 +/– 0.1
Ko	1.10 +/– 0.1
F	5.50 +/– 0.1
P1	8.00 +/– 0.1
W	12.00 +/– 0.3

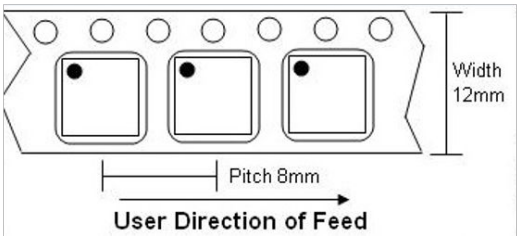


Figure 49. **Marking information**

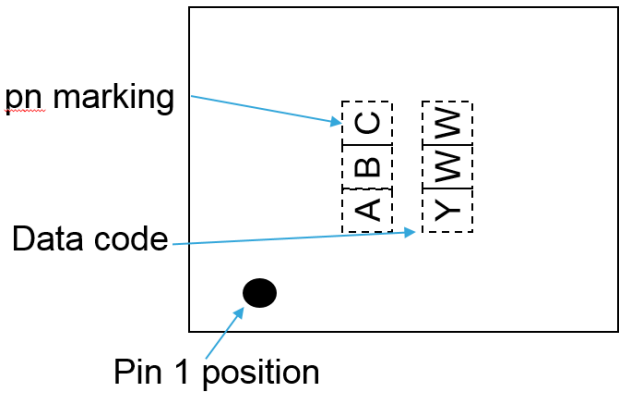
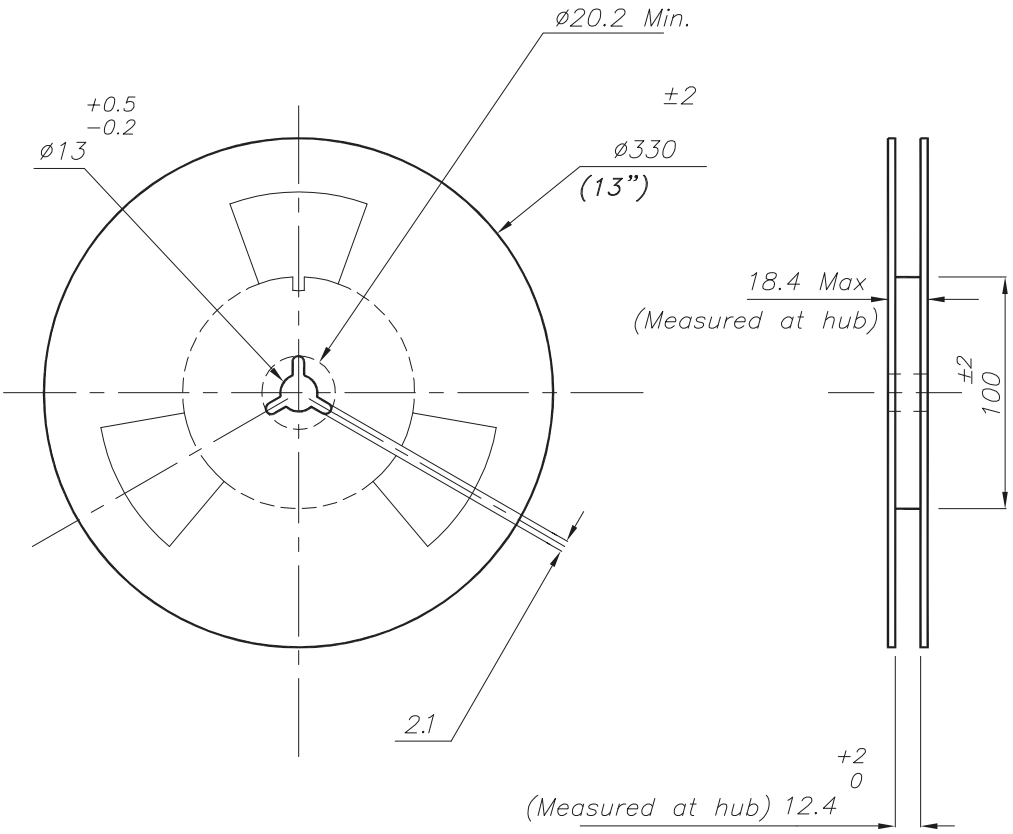


Figure 50. **Reel drawing**



9 Ordering information

Table 9. **Order codes**

Order code	Package	Marking
STEF512SRIPUR	DFN2x3	ERI

Revision history

Table 10. **Document revision history**

Date	Revision	Changes
14-Feb-2023	1	Initial release.

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