FEATURES

- CONSTRAINT LENGTH 7
- RATE 1/3 AND 1/2
- THREE BIT SOFT-DECISION IN SIGNED MAGNITUDE OR 2'S COMPLEMENT FORMAT
- UP TO 9600 BITS/SEC DATA RATE
- CODING GAIN OF 5.2 dB (AT 10^{-5} BER, RATE 1/2)
- CODING GAIN OF 6.0 dB (AT 10^{-5} BER, RATE 1/3)
- BOTH ENCODING AND DECODING FUNCTIONS PERFORMED
- LOW POWER CONSUMPTION, 40 mW
- SINGLE 5V SUPPLY
- COMMERCIAL AND MILITARY TEMPERATURE RANGES AVAILBLE
- AVAILABLE TO MIL-STD 883C

FUNCTIONAL DESCRIPTION

Convolutional Encoding and Viterbi Decoding are used to provide forward error correction (FEC) which improves digital communication performance over a noisy link. In satellite communication systems where transmitter power is limited, FEC techniques can reduce the required transmission power. The STEL-5268 is a very specialized product designed to perform this specific communications related function.

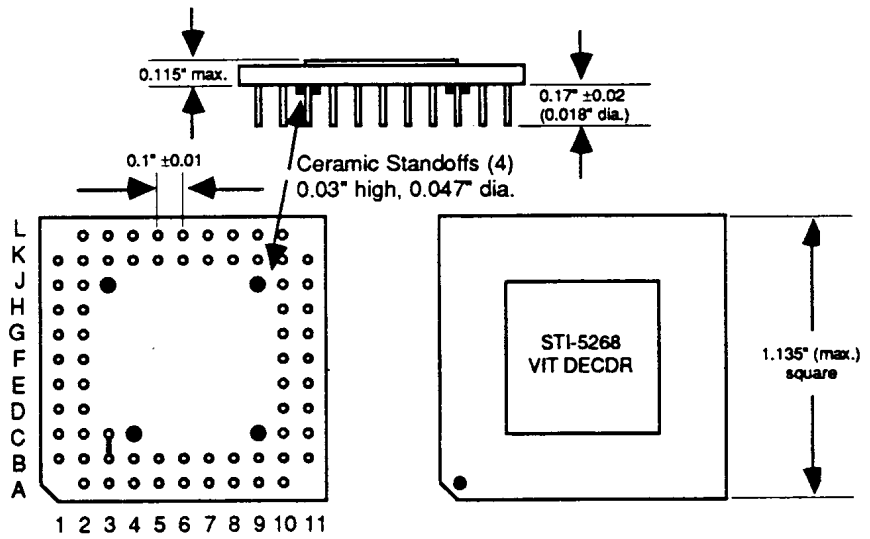
The encoder creates a stream of symbols which are transmitted at 2 (Rate 1/2) or 3 (Rate 1/3) times the information rate. This encoding introduces a high degree of redundancy which enables accurate decoding of information despite a high symbol error rate resulting from a noisy link.

The entire Convolutional Encoder/Viterbi Decoder (CODEC) is implemented with three chips; 2 RAMs are required in addition to the STEL-5268. A 128 x 8 RAM is required to store the 64 previous state metrics and the 64 current state metrics, and a 2K x 1 RAM is required to store the State Trellis information.

MECHANICAL INFORMATION

Package: 68 pin Ceramic PGA

Notes: 1. Tolerances on pin spacing are not cumulative.
2. Pins C2 and C3 (extra pin) are connected together.



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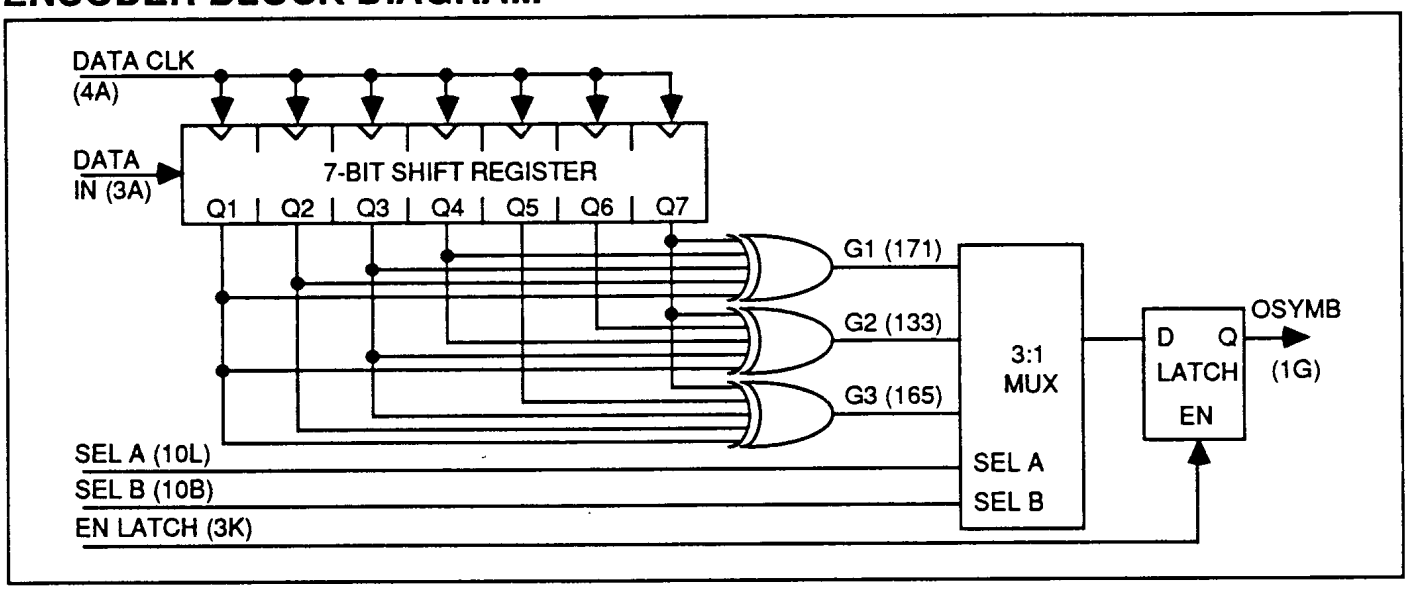
ENCODER OPERATION

The convolutional coder is functionally independent from the decoder and does not use the external RAMs. A single data bit is clocked into the 7-bit shift register on the rising edge of **DATA CLK**. The timing of the **SEL A**, **SEL B** and **EN LATCH** signals determine whether 2 or 3 symbol bits are generated for every data bit. The symbols G1, G2, and G3 are generated from the moulo-2 sum (exclusive-OR) of the inputs to the 3 generators from the taps on the shift register. The 3 polynomials are 171_8 (G1), 133_8 (G2), and 165_8 (G3). Example inputs are shown in the timing diagram for both rate $1/2$ and rate $1/3$ operation. Note that the output latch is transparent, so the **EN LATCH** input should only be pulsed high when the other inputs are stable.

ENCODER BLOCK DIAGRAM



INPUT SIGNALS

DATA CLK (pin 4A)
Encoder Shift Register Clock. A rising edge on this clock latches DATA IN into the encoder shift register. This signal should nominally be a square wave with a maximum frequency of 5.4 MHz.

DATA IN (pin 3A)
Encoder input. The data to be encoded is loaded into this pin and latched into the shift register on the rising edge of DATA CLK. This signal should be stable at the rising edge of **DATA CLK**.

SEL A (pin 10L), **SEL B** (pin 10B)
SEL A and **SEL B** select the encoded symbol, G1, G2 or G3, which will appear on the **OSYMB** pin on the next rising edge of **EN LATCH** according to the table below.

SEL A	SEL B	SYMBOL	POLYNOMIAL
0	1	G1	171_8 (1111001_2)
1	0	G2	133_8 (1011011_2)
0	0	G3	165_8 (1110101_2)

EN LATCH (pin 3K)
Encoder Output Latch Enable. A logic high on this pin enables the latch which outputs the encoder symbols. To avoid glitches on the encoder output this input should only be high when **DATA CLK** is not rising and **SEL A** and **SEL B** are stable.

MRESET (pin 8L)
Asynchronous Master Reset. A logic low on this pin will clear all registers on the STEL-5268 in both the encoder and decoder sections of the chip.

OUTPUT SIGNALS

OSYMB (pin 1G)
Output Symbol from the Encoder. This output depends on the seven most recent data bits (**DATA IN**) clocked into the encoder shift register and on the select lines **SEL A** and **SEL B**. The individual symbols are formed by the modulo-2 sum of the inputs to the generators from the 7-bit shift register.

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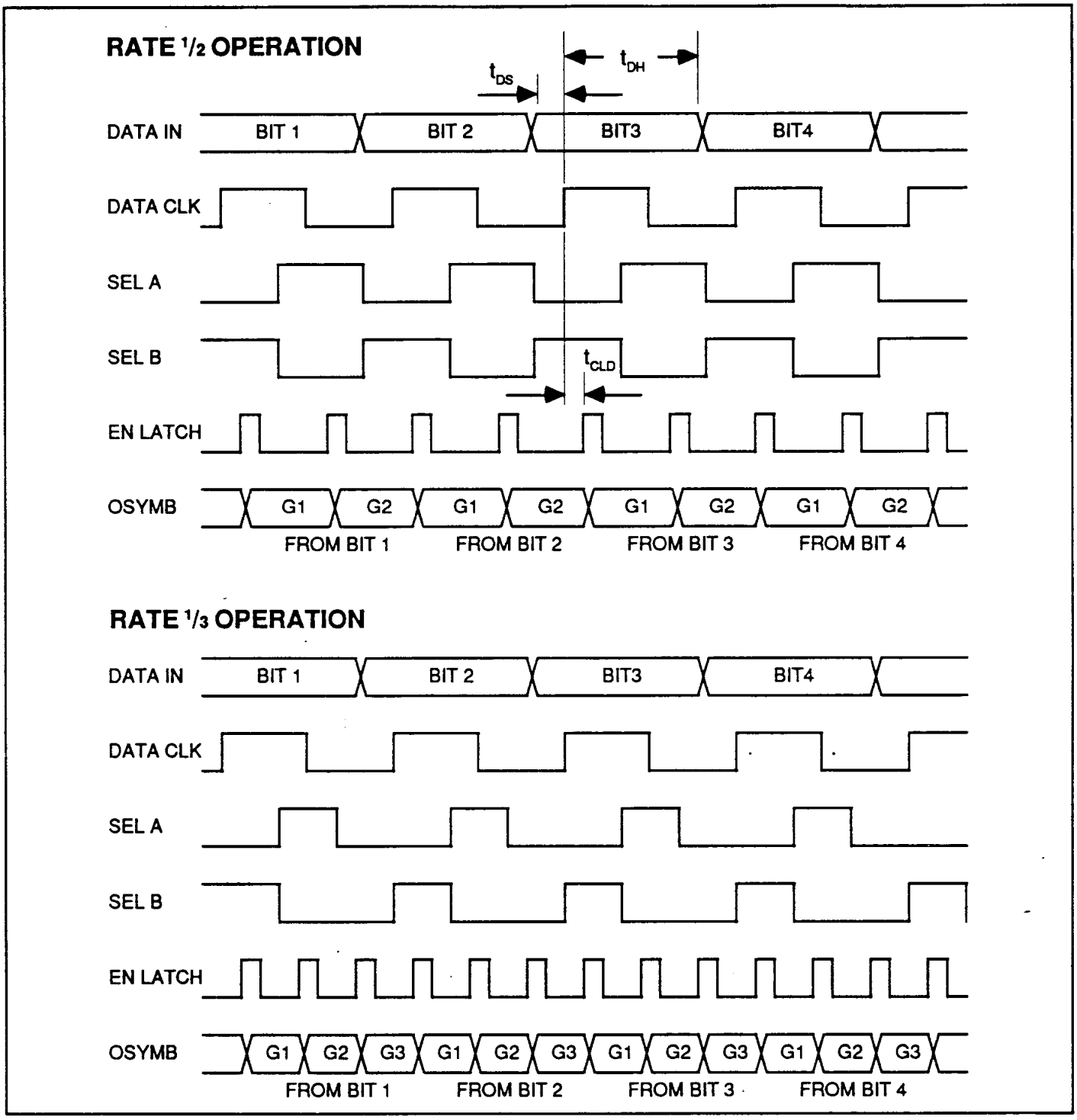
ENCODER TIMING



ENCODER A.C. CHARACTERISTICS (Operating Conditions: V_{DD}=5.0 volts, V_{SS}=0 volts, T_a=25°C)

Symbol	Parameter	Min.	Units
t_{DS}	**DATA IN** to **DATA CLK** setup	50	nsec.
t_{DH}	**DATA IN** to **DATA CLK** hold	0	nsec.
t_{CLD}	**DATA CLK** to **EN LATCH** delay	150	nsec.

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DECODER OPERATION

The STEL-5268 is designed to accept symbols in a handshake mode. The **DATA READY** input is used to indicate that valid symbols are ready. **ACK** is returned by the decoder to indicate that the symbols have been accepted, at which time **DATA READY** should be set to a logic 1. Symbols can also be supplied to the decoder in a non-handshake mode by pulsing **DATA READY** low. In this case the **DATA READY** pulse must be between 2 and 550 clock pulses wide. In either case the maximum input symbol rate is that corresponding to an output data rate of 9.6Kbps when operating at a clock frequency of 5.4 MHz.

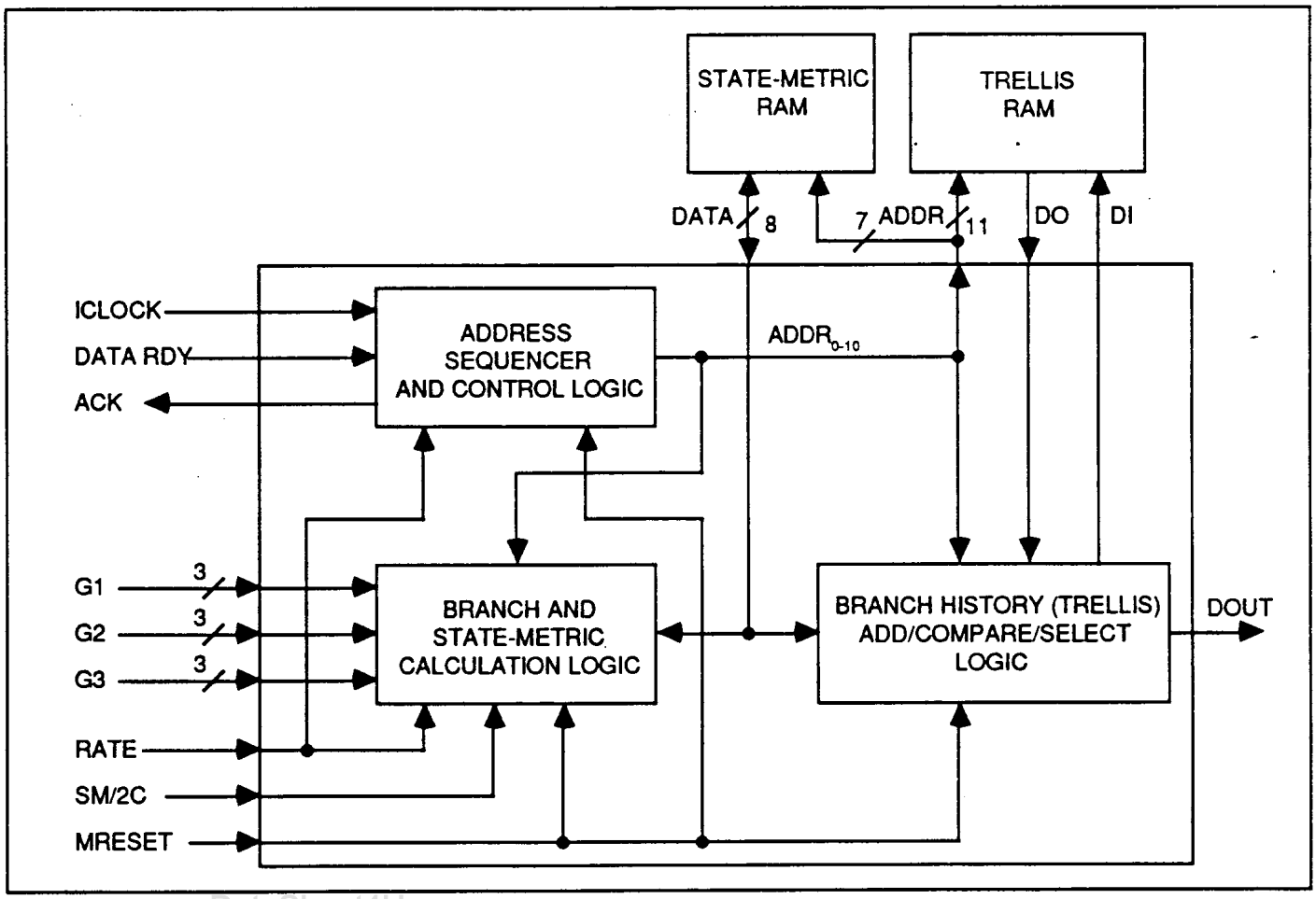
The **RATE** $^1/_2$-$^1/_3$ input determines whether the decoder will operate in rate $^1/_2$ or rate $^1/_3$ mode. When operating at rate $^1/_2$ the G3 symbol (pins **D6**, **D7**, and **D8**) is ignored by the decoder.

For hard decision binary symbols the G1, G2, G3 symbol bits should be connected to pins **D0**, **D3**, **D6** respectively, and pins **D1**, **D2**, **D4**, **D5**, **D7**, and **D8** should be tied to ground. Three-bit soft decision symbols may be input in Signed Magnitude or 2's Complement code, according to the setting of the code control pin.

A single decoded data bit is output for every set of input symbols. The data bit corresponding to a particular symbol set will be output after a delay of 38 symbols. Therefore, when using the STEL-5268 to decode blocks of data 38 additional dummy symbols and 38 **DATA READY** signals need to be added to the data stream to flush the last 38 decoded data bits out of the decoder.

Node synchronization (correctly grouping incoming symbols into G1, G2, and G3 blocks) is inherent with many communication techniques such as TDMA and spread spectrum systems. If node synchronization is not an inherent property of the communications link then additional circuitry will be required at the receiver to do this so that the symbols are loaded into the correct inputs.

DECODER BLOCK DIAGRAM (INCLUDING EXTERNAL RAMS)



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INPUT SIGNALS

MRESET (pin 8L)
Asynchronous Master Reset. A logic low on this pin will clear all registers in both the encoder and decoder sections of the chip.

RESET (pin 9L)
A logic low on this pin for 530 cycles of the system clock will completely clear the external RAMs.

ICLOCK (pin 9B), **OCLOCK** (pin 9A)
System Clock. A crystal may be connected between **ICLOCK** and **OCLOCK** or a CMOS level clock fed into **ICLOCK** only. The clock frequency should be at least 556 times the data rate but no more than the maximum clock frequency.

Rate 1/2-1/3 (pin 9K)
Selects whether the decoder will read two symbols (**Rate 1/2-1/3** set high) or three symbols (**Rate 1/2-1/3** set low)) for every data bit decoded. During rate 1/2 operation the symbol G3 on inputs **D6, D7** and **D8** is completely ignored by the decoder.

D0 (pin 2L), **D1** (pin 2K), **D2** (pin1K) (G1)
D3 (pin 1J), **D4** (pin 2J), **D5** (pin 1H) (G2)
D6 (pin 2C), **D7** (pin 1B), **D8** (pin 2B) (G3)
The three 3-bit soft decision symbols are connected to these inputs. If hard decision (single bit) symbols are used the G1 symbol is connected to **D0**, G2 to **D3** and G3 to **D6**. The decoder can make use of soft decision information, which includes both polarity information and a confidence measure, to improve the decoder performance. See **SIGN-MAG/2's COMP** for a description of the input data codes acceptable.

SIGN MAG/2's COMP (pin 10A)
Determines the format of the incoming soft-decision symbols according to the following table:

SYMBOL INPUT: D0, D1, D2 (G1) or D3, D4, D5 (G2) or D6, D7, D8 (G3)	CODE CONTROL SIGN MAG/2's COMP '1'	CODE CONTROL SIGN MAG/2's COMP '0'
Most Confident '1' level	1 1 1	1 0 0
	1 1 0	1 0 1
	1 0 1	1 1 0
Least Confident '1' level	1 0 0	1 1 1
Least Confident '0' level	0 0 0	0 0 0
	0 0 1	0 0 1
	0 1 0	0 1 0
Most Confident '0' level	0 1 1	0 1 1

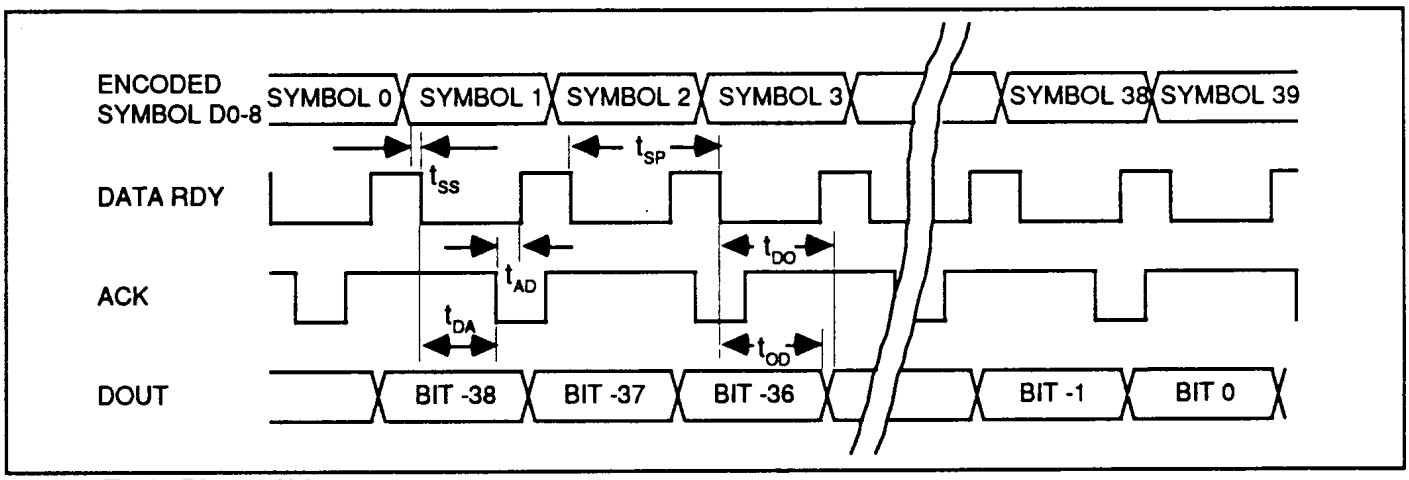
DATA READY (pin 3B)
When this pin is set at a low level it indicates to the decoder that 2 or 3 new symbols are ready to be loaded. This pin should be set high when **ACK** goes low.

OUTPUT SIGNALS

ACK (pin 6A)
A low level pulse on this pin indicates the decoder has input the current set of two or three symbols.

DOUT (pin 2G)
Decoded data bit. There is a delay of 38 data bits from the time a set of symbols is input to the time the corresponding data bit is output. Consequently, in order to flush the last 38 bits of data out of the system at the end of a burst it is necessary to continue pulsing the **DATA READY** line for 38 symbol periods after the last valid symbol has been entered.

DECODER TIMING



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DECODER A.C. CHARACTERISTICS

(Operating Conditions: f_{CLK}=5.4 MHz, V_{DD}=5.0 volts, V_{SS}=0 volts, T_a=25°C)

Symbol	Parameter	Min.	Max.	Units
t_{SS}	**SYMBOL** to **DATA RDY** setup	0		nsecs.
t_{SP}	**SYMBOL** Period	104		µsecs.
t_{DA}	**DATA RDY** to **ACK**	94	96	µsecs.
t_{AD}	**ACK** to **DATA RDY**		7	µsecs.
t_{DO}	**DATA RDY** to **DOUT**		103	µsecs.
t_{OD}	**DOUT** hold after **DATA RDY**	102		µsecs.

Note: All the above times should be pro-rated when operating at clock frequencies other than 5.4 MHz.

EXTERNAL RAM INTERFACE

The Viterbi decoder portion of the STEL-5268 requires 2 external RAMs for its operation. The connection diagram is shown on page 8. The State Metric RAM should be a 256 x 8 device with an access time of 25 nsecs. or less, e.g., Signetics 82S212. The Branch History (Trellis) RAM should be a 2K x 1 or 4K x 1 device (only 2K bits are actually needed) with an access time of 45 nsecs. or less, e.g., Intel 2147H-2 or an AMD AM2147-45 or equivalent. (The access times quoted apply to operation at a clock frequency of 5.4 MHz. The access times may be derated proportionally for lower clock frequencies.) The ordering of the address connections to the RAMs is arbitrary, the true addresses used are irrelevant to the operation of the system, and the same applies to the data bit connections for the State Metric RAM.

RAM INTERFACE I/O SIGNALS

(See connection diagram on page 8)

P (2H), **A0** (5B), **A1** (5A), **A2** (4B),
A3 (1C), **A4**(2D), **A5**(1D)
Address Lines common to both RAMs. These 7 address lines from the complete address for the State Metric RAM and the 7 MSBs for the Branch History/ Trellis RAM.

HIST0 (3L), **HIST1** (4K), **HIST2** (4L), **HIST3** (5K)
Additional Branch History/Trellis Address Lines. These 4 address lines complete the addressing to the Branch History/Trellis RAM.

Q (6L)
Branch History/Trellis Data Output. This is the output from the STI-5268 to the Branch History/Trellis RAM. See Branch History/Trellis RAM timing diagram for more information.

IDOUT (2A)
Branch History/Trellis Data Input. This is the output from the Branch History/Trellis RAM to the STI-5268. See Branch History/Trellis RAM timing diagram for more information.

RD ST (7K)
State Metric RAM Read Strobe. This active-low line is used to control the 3-state output buffers on the State Metric RAM chip.

WR ST (7L)
State Metric RAM Write Strobe. This active-low line is used to control the writing of data to the State Metric RAM.

WR TR (8K)
Branch History /Trellis RAM Write Strobe. This active-low line is used to control the writing of data to the Branch History /Trellis RAM

SMD0 (10K), **SMD1** (11K), **SMD2** (10J),
SMD3 (11J), **SMD4** (10G), **SMD5** (11G),
SMD6 (10F), **SMD7** (11F)
State Metric I/O Data bus. Data to and from the State Metric RAM is passed between the STEL-5268 and the State Metric RAM on this bus.

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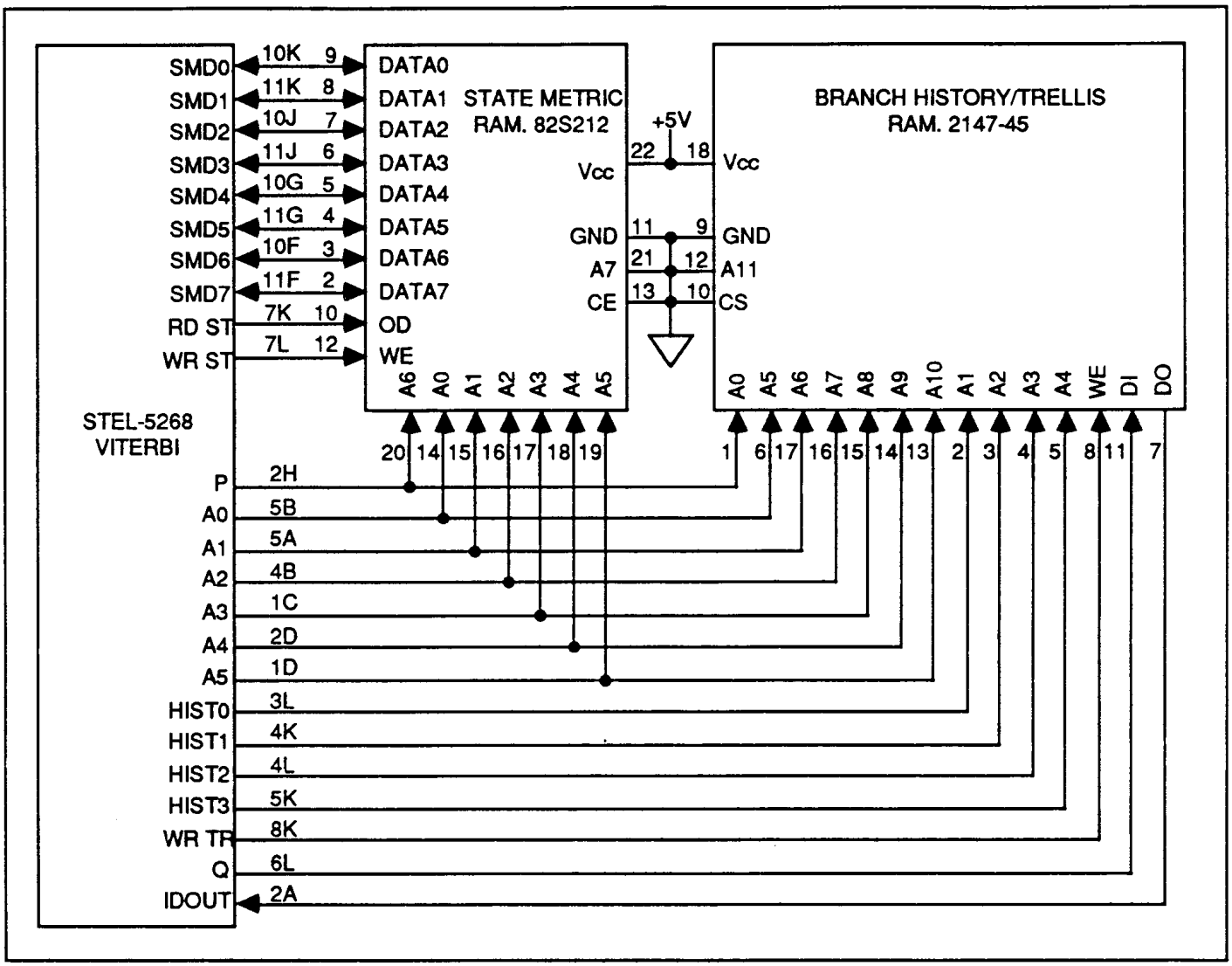
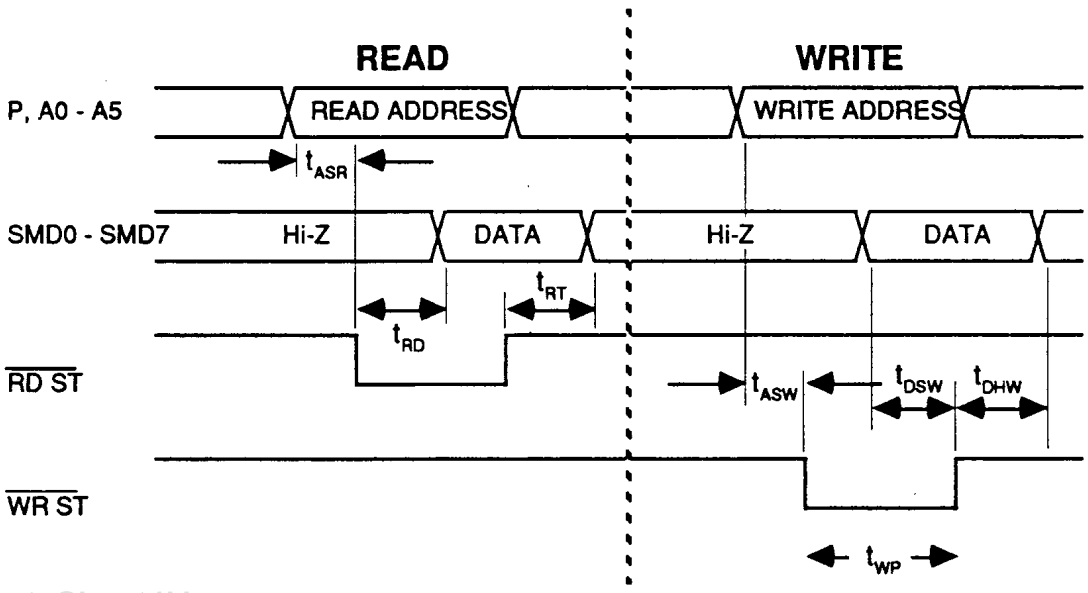
STI-5268 / RAM INTERFACE



STATE METRIC RAM TIMING



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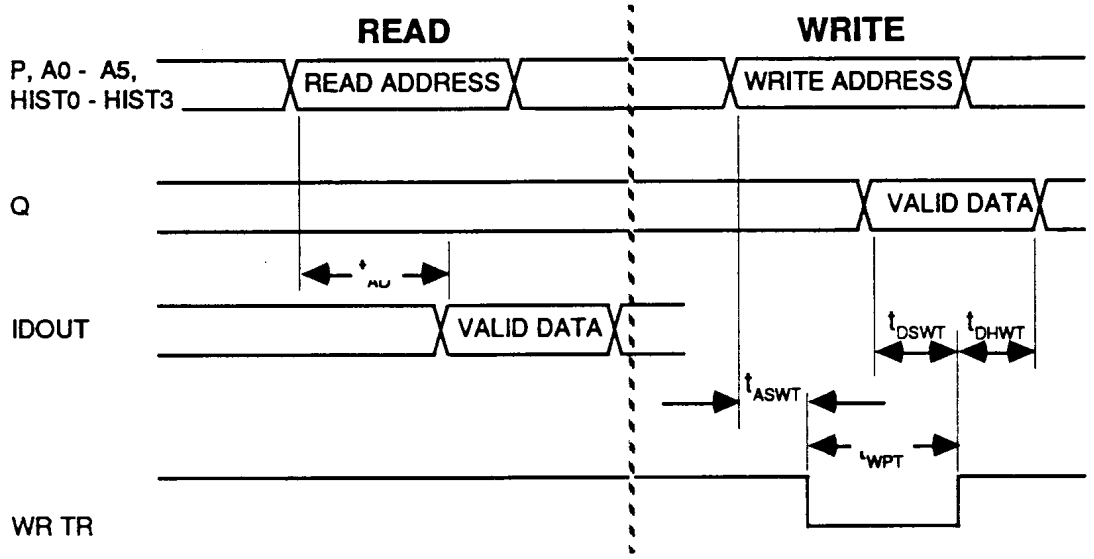
BRANCH HISTORY/TRELLIS RAM TIMING



RAM INTERFACE A.C. CHARACTERISTICS

(Operating Conditions: f_{CLK}=5.4 MHz, V_{DD}=5.0 volts, V_{SS}=0 volts, T_a=25°C)

STATE METRIC RAM

Symbol	Parameter	Min.	Max.	Units
t_{ASR}	Address Set up before **RD**	45		nsecs.
t_{RD}	Leading edge of **RD** to valid **DATA IN**	5	25	nsecs.
t_{RT}	Data bus tristated after trailing edge of **RD**		25	nsecs.
t_{ASW}	Address setup before leading edge **WR**	5		nsecs.
t_{WP}	**WR** pulse width	25		nsecs.
t_{DSW}	Data setup before trailing edge of **WR**	25		nsecs.
t_{DHW}	Data hold after trailing edge of **WR**	5		nsecs.

TRELLIS RAM

Symbol	Parameter	Min.	Max.	Units
t_{AD}	Valid data in from valid address		45	nsecs.
t_{ASWT}	Address setup before leading edge of **WR TR**	0		nsecs.
t_{WPT}	**WR TR** pulse width	25		nsecs.
t_{DSWT}	Data setup to trailing edge of **WR TR**	25		nsecs.
t_{DHWT}	Data hold after trailing edge of **WR TR**	10		nsecs.

Note: The RAM Interface timing parameters shown apply to operation at a clock frequency of 5.4 MHz.

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ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Note: Stresses greater than those shown below may cause permanent damage to the device. Exposure of the device to these conditions for extended periods may also affect device reliability.

Symbol	Parameter	Range	Units
T_{stg}	Storage Temperature	–65 to +150	°C
T_a	Operating Temperature	–25 to +85 –55 to +125	°C (Commercial) °C (Mil Screened)
V_{DDmax}	Max. voltage between V_{DD} and V_{SS}	+7 to –0.7	volts
$V_{I/O(max)}$	Max. voltage on any input or output pin	V_{DD}+0.7	volts
$V_{I/O(min)}$	Min. voltage on any input or output pin	V_{SS}–0.7	volts

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Range	Units
V_{DD}	Supply Voltage	+5 ± 10%	volts
T_a	Operating Temperature (Ambient)	–25 to + 85 –55 to +125	°C (Commercial) °C (Mil Screened)

D.C. CHARACTERISTICS (Operating Conditions: V_{DD}=5.0 volts, V_{SS}=0 volts, T_a=25°C)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_{DD(Q)}$	Supply Current, Quiescent			1.0	mA	Static, no clock
I_{DD}	Supply Current, Operational			20.0	mA	@ 5.4 MHz
$V_{IH(min)}$	Min. High Level Input Voltage	2.0			volts	Guaranteed Logic '1'
$V_{IL(max)}$	Max. Low Level Input Voltage			0.8	volts	Guaranteed Logic '0'
$V_{OH(min)}$	Min. High Level Output Voltage	2.4			volts	I_O = –1.6 mA
$V_{OL(max)}$	Max. Low Level Output Voltage			0.4	volts	I_O = 1.6 mA
$I_{IH(max)}$	Max. High Level Input Current			2.0	µA	V_{IN} = +5.0 volts
$I_{IL(max)}$	Max. Low Level Input Current			–2.0	µA	V_{IN} = 0 volts
$I_{OH(min)}$	Min. High Level Output Current	–1.5			mA	V_{OUT} = 2.8 volts
$I_{OL(min)}$	Min. Low Level Output Current	1.2			mA	V_{OUT} = 0.4 volts

POWER CONNECTIONS

V_{DD} (pins 1E, 5L, 7A, 10H, 11E)
Positive supply voltage, +5 volts.

V_{SS} (pins 2F, 6B, 6K, 10D, 11H)
Negative supply voltage, ground.

Note: Leave all pins not specifically labelled unconnected. Do not use for vias.

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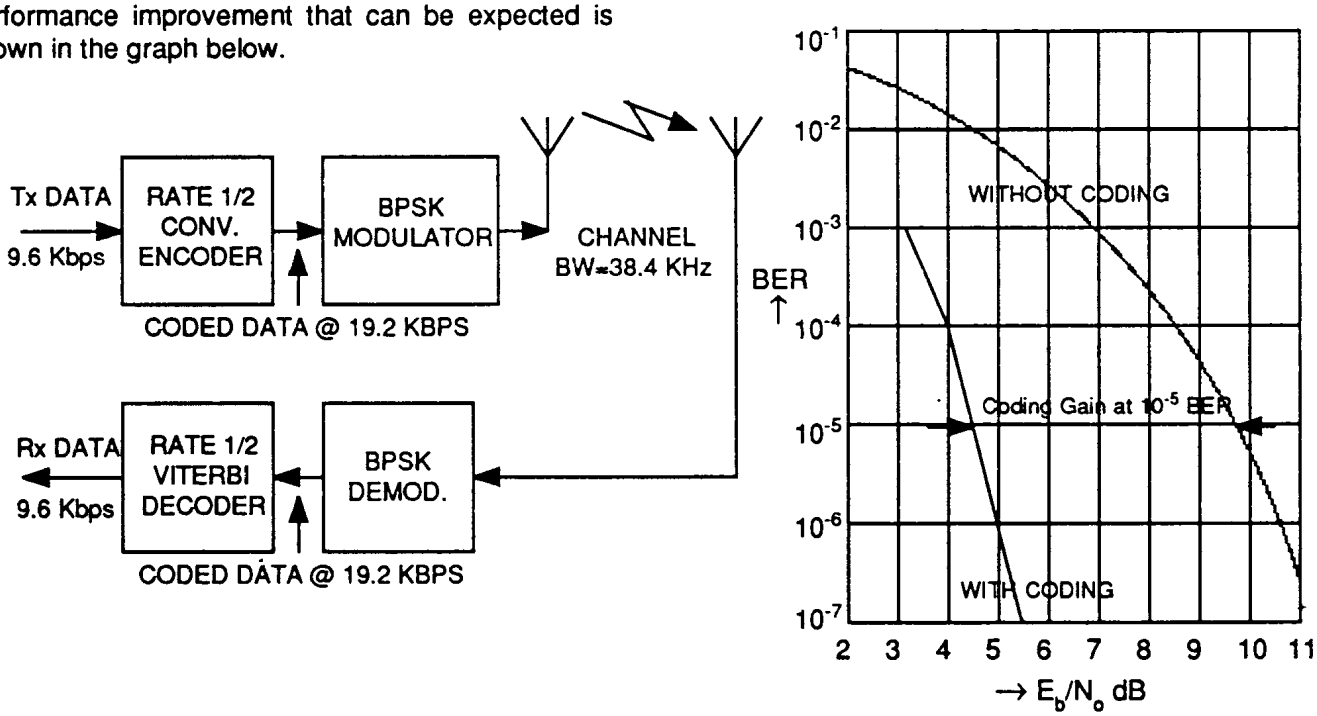
APPLICATION INFORMATION

The entire Convolutional Encoder/Viterbi Decoder (CODEC) is implemented with three integrated circuits. In addition to the STEL-5268 two memory chips are required. One 128 x 8 memory is required to store the 64 previous state metrics and the 64 current state metrics. A second 2K x 1 memory is required to store the state trellis information.

An example of a system using the convolutional coder and Viterbi decoder is illustrated here. The system modulates a data stream of rate 19.2 Kbps using binary PSK (BPSK). To be able to use convolutional coding/decoding, the system must have available the additional bandwidth needed to transmit symbols at twice the data rate (for rate $^1/_2$ encoding). Alternatively, the system could make use of two parallel channels to transmit two streams of symbols at the data rate. The performance improvement that can be expected is shown in the graph below.

The convolutional encoder is functionally independent from the decoder and does not use the auxiliary RAMs. A single data bit is clocked into the 7 bit shift register on the rising edge of **DATA CLK**. It is up to the user to provide the proper **SELECT** and **EN LATCH** signals to create the serial output stream of two or three symbol bits for every data bit clocked in.

The STEL-5268 is designed to accept symbols in a handshake mode. **DATA RDY** is supplied by the user. **ACK** returned by the STEL-5268 indicates the symbols have been accepted. Symbol information can also be supplied to the STEL-5268 in a non-handshake mode. The maximum data rate is 9.6 Kbps, using a clock frequency of 5.4 MHz. This corresponds to 19.2K symbols per second at rate $^1/_2$ and 28.8K symbols per second at rate $^1/_3$.



BPSK COMMUNICATION SYSTEM USING CONVOLUTIONAL ENCODING AND VITERBI DECODING. RATE = $^1/_2$

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