STEL-5269+512

Data Sheet

STEL-5269+512

Convolutional Encoder

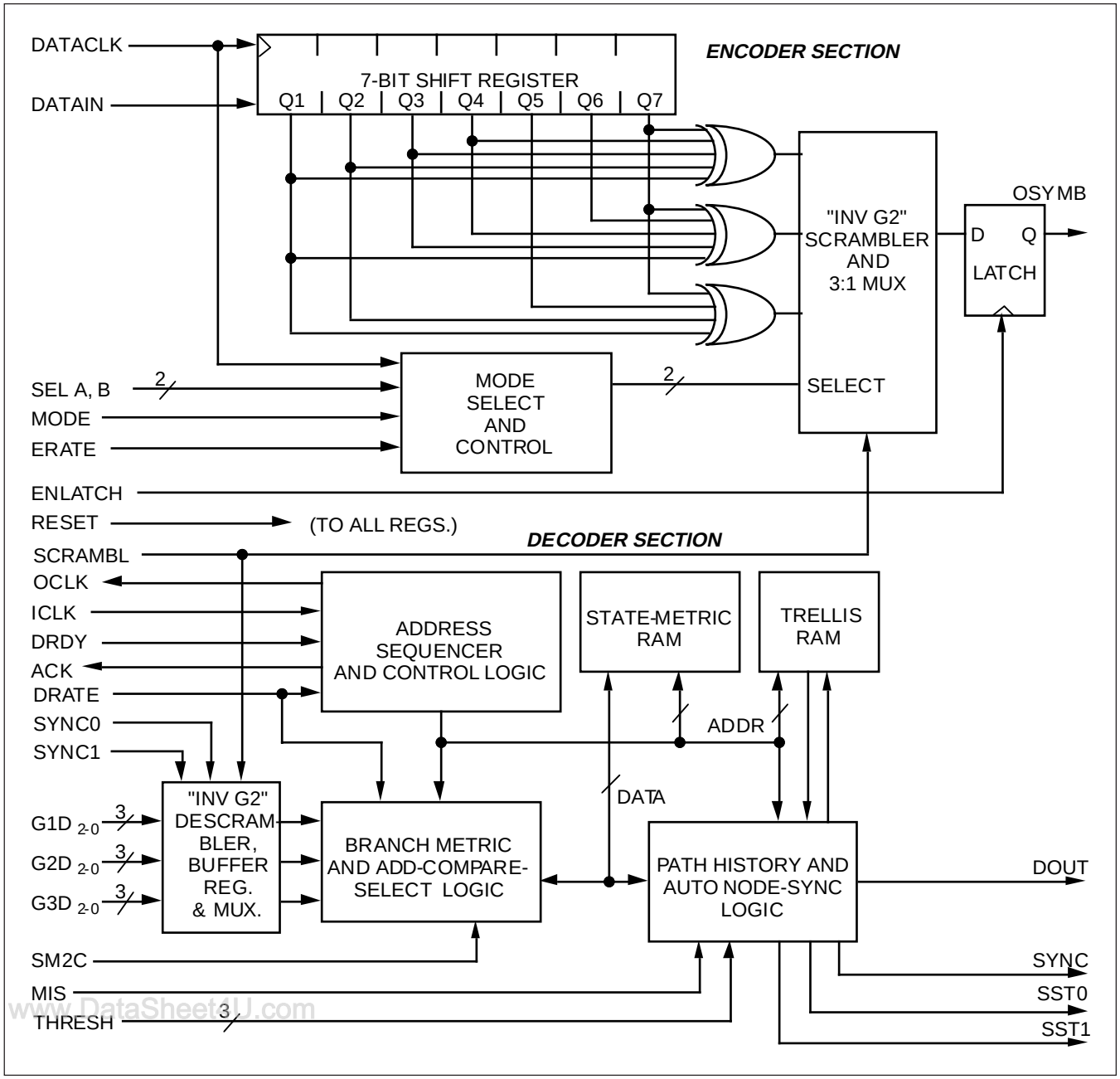
Viterbi Decoder

intel

FEATURES

- **CONSTRAINT LENGTH 7**
- **CODING RATES $^1/_2$ AND $^1/_3$**
- **THREE BIT SOFT-DECISION INPUTS IN SIGNED MAGNITUDE OR 2's COMPLEMENT FORMAT**
- **512 Kbps DATA RATE (0° to 70° C)**
- **CODING GAIN OF 5.2 dB (AT 10-5 BER, RATE $^1/_2$)**
- **CODING GAIN OF 6.0 dB (AT 10^{-5} BER, RATE $^1/_3$)**
- **INDUSTRY STANDARD POLYNOMIALS G1 = 171_8, G2 = 133_8, G3 = 145_8,**
- **LOW POWER CONSUMPTION**
- **44 PIN PLCC AND CLDCC PACKAGES**
- **AVAILABLE TO MIL-STD 883C**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Convolutional Encoding and Viterbi Decoding are used to provide forward error correction (FEC) which improves digital communication performance over a noisy link. In satellite communication systems where transmitter power is limited, FEC techniques can reduce the required transmission power. The STEL-5269+512 is a specialized product designed to perform this specific communications related function.

The encoder creates a stream of symbols which are transmitted at 2 (Rate $^1/_2$) or 3 (Rate $^1/_3$) times the information rate. This encoding introduces a high degree of redundancy which enables accurate decoding of information despite a high symbol error rate resulting from a noisy link.

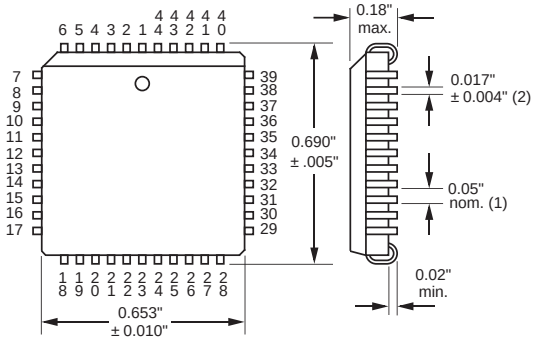
The STEL-5269+512 incorporates all the memories required to perform these functions. The STEL-5269+512 is available in a 44-pin PLCC (plastic leaded chip carrier) and also in a ceramic leaded chip carrier (J-bend leads). A 256 Kbps version, the STEL-5269, is also available at a lower cost.

ENCODER OPERATION

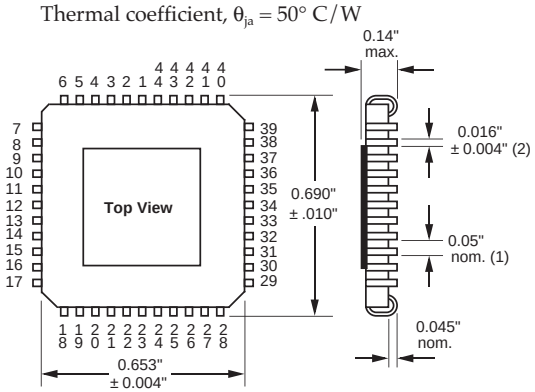
The convolutional coder is functionally independent of the decoder. A single data bit is clocked into the 7-bit shift register on the rising edge of **DATACLK**. There are two modes of operation, controlled by the **MODE** input. When **MODE** is low the timing of the **SEL A**, **SEL B** and **ENLATCH** signals determine whether 2 or 3 symbol bits are generated for every data bit. When **MODE** is high the symbols are automatically generated sequentially every clock cycle. In this case, the state of **ENRATE** determines whether the device generates symbols for Rate $^1/_2$ or Rate $^1/_3$ operation. The symbols G1, G2, and G3 are generated from the modulo-2 sum (exclusive-OR) of the inputs to the 3 generators from the taps on the shift register. The 3 polynomials are 171_8 (G1), 133_8 (G2), and 145_8 (G3). Example inputs are shown in the timing diagram for both rate $^1/_2$ and rate $^1/_3$ operation.

PIN CONFIGURATION

Package: 44 pin PLCC
Thermal coefficient, θ_{ja} = 40°C/W



Package: 44 pin CLDCC
Thermal coefficient, θ_{ja} = 50° C/W



Notes: (1) Tolerances on pin spacing are not cumulative.
(2) Dimensions apply at seating plane.
(3) PLCC and CLDCC packages have different corners and may not fit into sockets designed for the other type. Universal sockets are available without alignment locators.

PIN CONNECTIONS

1	SYNC	12	MIS	23	V_{SS}	34	V_{SS}
2	V_{SS}	13	DOUT	24	$THRESH_0$	35	SST1
3	ACK	14	OSYMB	25	$THRESH_1$	36	SYNC1
4	DATACLK	15	$G2D_0$	26	RESET	37	SST0
5	DRDY	16	$G2D_1$	27	DRATE	38	SYNC0
6	DATAIN	17	$G2D_2$	28	SEL A	39	SEL B
7	$G3D_0$	18	$G1D_0$	29	$THRESH_2$	40	SM2C
8	$G3D_1$	19	$G1D_1$	30	V_{DD}	41	ICLK
9	$G3D_2$	20	$G1D_2$	31	V_{SS}	42	OCLK
10	MODE	21	ENLATCH	32	I.C.	43	SCRAMBL
11	V_{SS}	22	V_{DD}	33	ERATE	44	I.C.

Note: I.C. denotes Internal Connection. These pins must be left unconnected. Do not use for vias.

DECODER OPERATION

The STEL-5269+512 is designed to accept symbols either synchronously or in a handshake mode. Symbols are latched into the decoder input registers on the falling edge of the **DRDY** input. **ACK** is returned by the decoder to indicate that the symbols have been accepted.

The **RATE** input determines whether the decoder will operate in Rate $^1/_2$ or Rate $^1/_3$ mode. When operating at Rate $^1/_2$ the G3 symbol is ignored by the decoder.

For hard decision binary symbols the G1, G2, G3 symbol bits should be connected to pins $\mathbf{G1D_2}$, $\mathbf{G2D_2}$ and $\mathbf{G3D_2}$ respectively, and the other symbol input pins should be tied high (V_{DD}). Three-bit soft decision symbols may be input in Signed Magnitude or Inverted Two's Complement code, according to the setting of the code control pin, **SM2C**. The code should be set to Signed Magnitude when using hard decision data.

A single decoded data bit is output for every set of input symbols. The data bit corresponding to a particular symbol set will be output after a delay of 42 symbols. Therefore, when using the STEL-5269+512 to decode blocks of data 42 additional dummy symbols and 42 **DRDY** signals need to be added to the data stream to flush the last 42 decoded data bits out of the decoder.

Node synchronization (correctly grouping incoming symbols into G1, G2, and G3 sets) is inherent with many communication techniques such as TDMA and spread spectrum systems. If node synchronization is not an inherent property of the communications link then the internal auto node sync circuit can be used to do this. This is accomplished by connecting the node sync outputs (**SST0** and **SST1**) to the node sync inputs (**SYNC0** and **SYNC1**). The threshold for determining the out of sync condition is user selectable by means of the $\mathbf{THRESH_{2\text{-}0}}$ inputs. Alternatively, the **SYNC0** and **SYNC1** pins can be used with an external algorithm to achieve the same result.

Further information on the theory of operation of Viterbi decoders may be obtained from text books such as "Error-Correcting Codes", by Peterson and Weldon (MIT Press), or "Error Control Coding", by Lin and Costello (Prentice-Hall). An alternative source of information is the many papers on this subject that have appeared in the IEEE transactions, such as "Convolutional Codes and their Performance in Communication Systems", by Dr. A. J. Viterbi, IEEE Trans. on Communications Technology, October 1971.

INPUT SIGNALS

RESET

Asynchronous master **Reset**. A logic low on this pin will clear all registers on the STEL-5269+512 in both the encoder and decoder sections of the chip. **RESET** should remain low for at least 3 cycles of **ICLK**.

DATACLK

This is the encoder Shift Register Clock. A rising edge on this clock latches **DATAIN** into the encoder shift register. This signal should nominally be a square wave with a maximum frequency of 512 KHz.

DATAIN

This is the encoder input. The data present at this pin is latched into the encoder shift register on the rising edge of **DATACLK**. This signal should be stable at the rising edge of **DATACLK**.

MODE

The state of the **MODE** input determines the method of symbol sequencing in the encoder. When **MODE** is set low the sequencing is generated externally under the control of the **SEL A** and **SEL B** inputs, and when **MODE** is set high it is generated automatically.

SEL A, SEL B

When **MODE** is set low **SEL A** and **SEL B** select the encoded symbol, G1, G2 or G3, which will appear on the **OSYMB** pin on the next rising edge of **ENLATCH** according to the table:

SEL A	SEL B	SYMBOL	POLYNOMIAL
0	1	G1	171_8 (1111001_2)
1	0	G2	133_8 (1011011_2)
0	0	G3	145_8 (1100101_2)

When **MODE** is set high the symbol sequence is generated automatically and the **SEL A** and **SEL B** inputs are inactive.

ERATE

When **MODE** is high the **E**ncoder **Rate** input determines whether symbols for Rate $^1/_2$ (ERATE = 1) or Rate $^1/_3$ (ERATE = 0) operation are generated. When **MODE** is low this input is inactive.

SCRAMBL

When the **Scrambl**e input is set high the G2 symbol generated at the encoder and the G2 symbol received at the decoder will be inverted. This ensures that the output symbol stream is not a string of zeroes when the input data stream is all zeroes, thereby making it easier for the demodulator to recover the clock information under these conditions. When **SCRAMBL** is set low the normal symbol stream is generated.

ENLATCH

This is the **en**coder Output **Latch** Enable. The new symbol is clocked into the output latch and appears on the **OSYMB** pin on the rising edge of **ENLATCH**. When **MODE** is low the symbol selected will depend on the states of the **SEL A** and **SEL B** lines, which should be stable on the rising edge of **ENLATCH**. When **MODE** is high the symbol selection is internal, and the frequency of the **ENLATCH** signal should be 2 or 3 times the frequency of the **DATACLK**, depending on the rate selected.

ICLK, OCLK

System Clock. A crystal may be connected between **ICLK** and **OCLK** or a CMOS level clock may be fed into **ICLK** only. The clock frequency should be at least 70 times the data rate but no more than 36 MHz.

DRATE

The **D**ecoder **Rate** input selects whether the decoder will read two symbols (**DRATE** set high) or three symbols (**DRATE** set low)) for every data bit decoded. During rate $^1/_2$ operation the symbol G3 on inputs $\mathbf{G3D_{2\text{-}0}}$ is completely ignored by the decoder.

$\mathbf{G1D_{2\text{-}0}}$, $\mathbf{G2D_{2\text{-}0}}$, $\mathbf{G3D_{2\text{-}0}}$

The three 3-bit soft decision symbols are connected to these inputs and loaded into the input registers on the falling edge of **DRDY**. The order in which the symbols are entered into the decoder from the registers depends on the state of the **SYNC0** and **SYNC1** inputs. The decoder can make use of soft decision information, which includes both polarity information and a confidence measure, to improve the decoder performance. If hard decision (single bit) symbols are used the signals are connected to pins $\mathbf{G1D_2}$, $\mathbf{G2D_2}$ and $\mathbf{G3D_2}$ and the other inputs are connected to V_{DD}. See **SM2C** for a description of the input data codes.

DRDY

The **D**ata **R**ea**d**y signal is used to load symbols into the decoder. This signal is edge triggered and a new set of symbols is latched into the input registers on each falling edge of the **DRDY** input.

SM2C

The state of the **S**igned **M**agnitude/**2**'s **C**omplement input determines the format of the incoming soft-decision symbols into the decoder. When SM2C is high the input code is Signed Magnitude, and when it is low the code is Two's Complement. The codes are shown in the following table:

CODE CONTROL: SYMBOL INPUT:	SM2C = 1 $GxD_{2\text{-}0}$	SM2C = 0 $GxD_{2\text{-}0}$
Most Confident '+' level	0 1 1	0 1 1
Data = 0	0 1 0	0 1 0
	0 0 1	0 0 1
Least Confident '+' level	0 0 0	0 0 0
Least Confident '–' level	1 0 0	1 1 1
Data = 1	1 0 1	1 1 0
	1 1 0	1 0 1
Most Confident '–' level	1 1 1	1 0 0

When using hard decision data, SM2C should be set high, the $G1_2$ and $G2_2$ input pins used for the symbol signals and $G1_{1\text{-}0}$ and $G2_{1\text{-}0}$ tied high.

SYNC0, SYNC1

The Symbol **Sync** inputs are used for auto node sync operation. When using the internal auto node sync mode these two pins are connected to **SST0** and **SST1**, respectively. The operation of the decoder is affected in the following way by the **SYNC0** and **SYNC1** inputs:

			Symbol entered into decoder inputs during symbol period N		
RATE	SYNC0	SYNC1	$G1_{2\text{-}0}$	$G2_{2\text{-}0}$	$G3_{2\text{-}0}$
1	0	0	$G1_N$	$G2_N$	–
1	1	0	$G2_{N-1}$	$G1_N$	–
1	0	1	$\overline{G2_N}$	$G1_N$	–
1	1	1	Invalid state		
0	0	0	$G1_N$	$G2_N$	$G3_N$
0	1	0	$G3_{N-1}$	$G1_N$	$G2_N$
0	0	1	$G2_{N-1}$	$G3_{N-1}$	$G1_N$
0	1	1	Invalid state		

When RATE = 1 (rate $^1/_2$ operation) only one possible alternative state exists in any given situation. This depends on whether the modulation format used was BPSK (sequential symbols) or QPSK (parallel symbol pairs). In this case the node sync process can be improved by only using the SYNC input applicable for the corresponding alternative sync state (i.e., SYNC0 for BPSK, SYNC1 for QPSK) and tying the other low to prevent the node sync circuit from inadvertently selecting the non-applicable state. When RATE = 0 (rate $^1/_3$ operation) both alternative sync states correspond to those possible with BPSK modulation.

Note that whenever the states of the **SYNC0** and **SYNC1** inputs are changed there will be a delay of 42 bit periods before valid data starts appearing at **DOUT**.

MIS

Two algorithms for auto node-sync are incorporated into the STEL-5269+512. When **MIS** is set high the Traceback **Mis**match algorithm is selected, and when **MIS** is set low the Metric Renormalization algorithm is selected. The Traceback Mismatch algorithm is recommended for most applications since it generates a better discrimination function between the in-sync and out-of-sync conditions, especially at high error rates ($E_b/N_0 \leq 3$ dB).

$THRESH_{2-0}$

A counter is used to determine the number of either traceback mismatches or metric renormalizations per 256 bits in the auto node-sync circuit, and the threshold at which the counter triggers the **SST0** and **SST1** outputs to change states is set with the data on the $THRESH_{2-0}$ inputs. The threshold values will be as shown in the table below.

$THRESH_{2-0}$	Threshold value
0	1
1	2
2	4
3	8
4	16
5	32
6	64
7	128

Since the actual error rate obtained will depend on the signal to noise ratio (E_b/N_o) in the signal, the optimum value of the threshold will also depend on E_b/N_o and should be set accordingly. Suggested initial values for $THRESH_{2-0}$ are 5 for the Mismatch algorithm and 3 for the Renormalization algorithm.

OUTPUT SIGNALS

OSYMB

Output Symbol from the Encoder. This output depends on the seven most recent data bits (**DATAIN**) clocked into the encoder shift register and on the select lines **SEL A** and **SEL B**. The individual symbols are formed by the modulo-2 sum of the inputs to the generators from the 7-bit shift register.

ACK

A low level pulse on the **Ack**nowledge pin indicates that the decoder has input the current set of two or three symbols. The signal will pulse low between 68 and 69 clock cycles after the falling edge of **DRDY**.

DOUT

Decoded **D**ata **Out**. The signal is latched into the output register on the falling edge of **DRDY**. There is a delay of 42 data bits from the time a set of symbols is input to the time the corresponding data bit is output. Consequently, in order to flush the last 42 bits of data out of the system at the end of a burst it is necessary to continue pulsing the **DRDY** line for 42 symbol periods after the last valid symbol has been entered.

SST0, SST1

The **S**ync **St**ate **0** and **S**ync **St**ate **1** signals are the outputs of the internal auto node sync circuit. They should be connected to **SYNC0** and **SYNC1** respectively to use the internal auto node sync capability. They may also be used in conjunction with an external node sync algorithm implementation which can use the **SST0** and **SST1** outputs.

SYNC

The **Sync** output provides an indication of the status of the internal auto node sync circuit. When it is high it indicates that node sync has been lost, and when it is low it indicates that the system is assumed to be in sync, as determined by the error rate estimate.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Warning: ***Stresses greater than those shown below may cause permanent damage to the device. Exposure of the device to these conditions for extended periods may also affect device reliability.***

Symbol	Parameter	Range	Units
T_s	Storage Temperature	–40 to +125	°C (Plastic package)
		–55 to +125	°C (Ceramic package)
T_a	Operating Temperature	–40 to +85	°C (Plastic package)
		–55 to +125	°C (Ceramic package)
V_{DDmax}	Max. voltage between V_{DD} and V_{SS}	+7 to –0.7	volts
$V_{I/O(max)}$	Max. voltage on any input or output pin	V_{DD} + 0.3	volts
$V_{I/O(min)}$	Min. voltage on any input or output pin	V_{SS} – 0.3	volts

RECOMMENDED OPERATING CONDITIONS

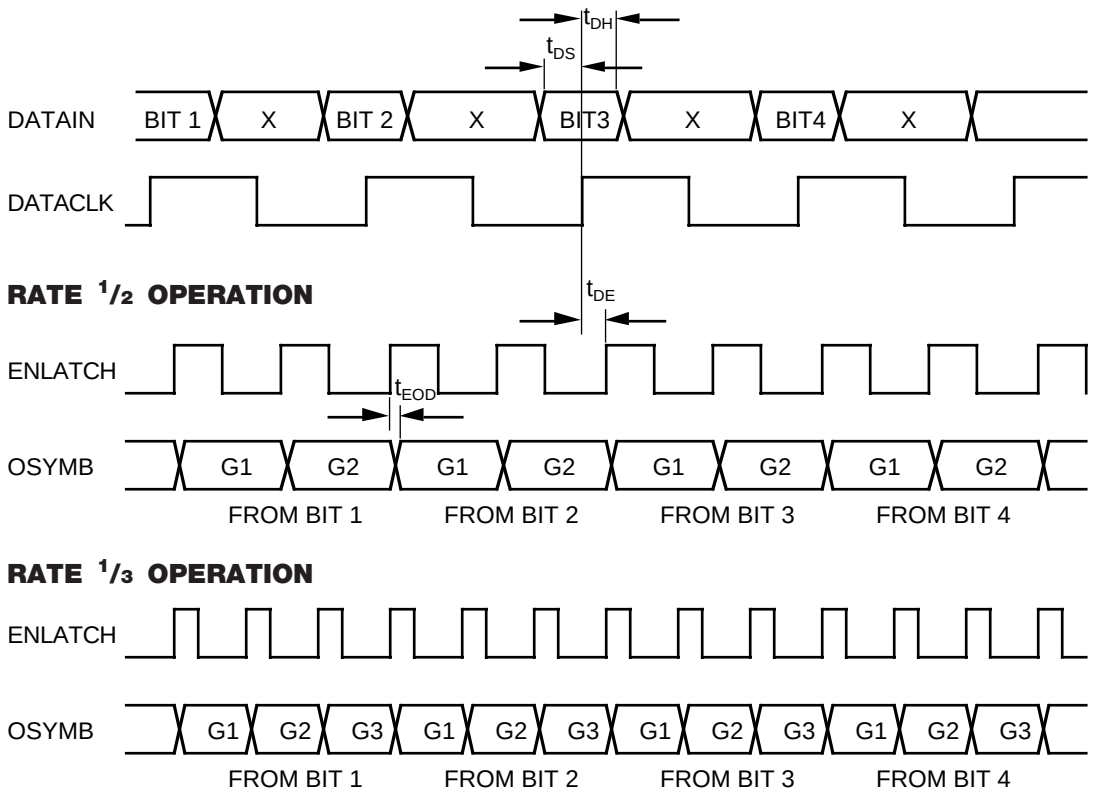
Symbol		Parameter	Range	Units
T_a	Operating Temperature (Ambient)	0 to +70	°C	(Plastic package)
		–55 to +125	°C	(Ceramic package)
V_{DD}	Supply Voltage	+5 ± 5%	volts	(Commercial grade)
		+5 ± 5%	volts	(Military grade)

D.C. CHARACTERISTICS

(Standard Operating Conditions: V_{DD} = 5.0 ± 5% volts, T_a = 0° to 70° C,
Military Operating Conditions: V_{DD} = 5.0 ± 5% volts, T_a = –55° to 125° C)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_{DD(Q)}$	Supply Current, Quiescent			1.0	mA	Static, no clock
I_{DD}	Supply Current, Operational		2.0		mA/Mbps	f_{CLK} = 36 MHz
I_{DD}	Supply Current, Operational		6		mA/Mbps	All other modes
$V_{IH(min)}$	Min. High Level Input Voltage					
	Commercial Operating Cond.	2.0			volts	Guaranteed Logic '1'
	Military Operating Cond.	2.25			volts	Guaranteed Logic '1'
$V_{IL(max)}$	Max. Low Level Input Voltage			0.8	volts	Guaranteed Logic '0'
$V_{OH(min)}$	Min. High Level Output Voltage	2.4			volts	I_O = –4.0 mA
$V_{OL(max)}$	Max. Low Level Output Voltage			0.4	volts	I_O = +4.0 mA
$I_{IH(min)}$	High Level Input Current	10	35	110	µA	**DRDY**, $V_{IN} = V_{DD}$
$I_{IL(max)}$	Low Level Input Current	–15	–45	–130	µA	All other inputs, $V_{IN} = V_{SS}$
I_{OS}	Output Short Circuit Current	20	65	130	mA	$V_{OUT} = V_{DD}$, V_{DD} = max
		–10	–45	–130	mA	$V_{OUT} = V_{SS}$, V_{DD} = max
C_{IN}	Input Capacitance			2	pF	All inputs
C_{OUT}	Output Capacitance			4	pF	All outputs

ENCODER TIMING. MODE = 1



ENCODER ELECTRICAL CHARACTERISTICS

A.C. CHARACTERISTICS

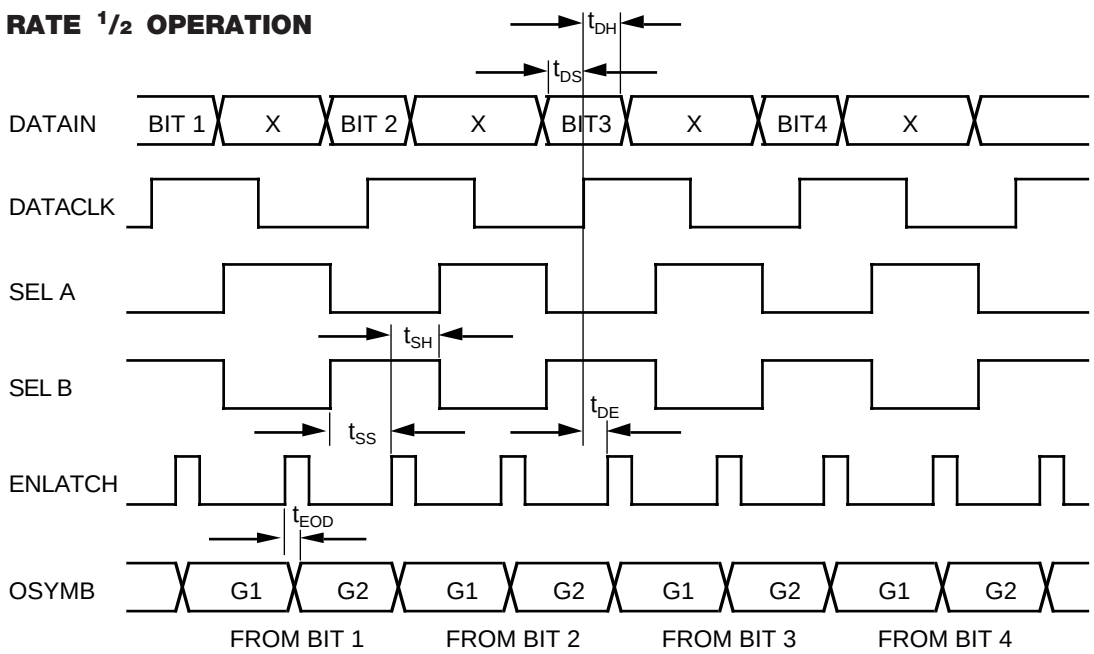
(Standard Operating Conditions: V_{DD} = 5.0 ± 5% volts, T_a = 0° to 70° C,
Military Operating Conditions: V_{DD} = 5.0 ± 5% volts, T_a = –55° to 125° C)

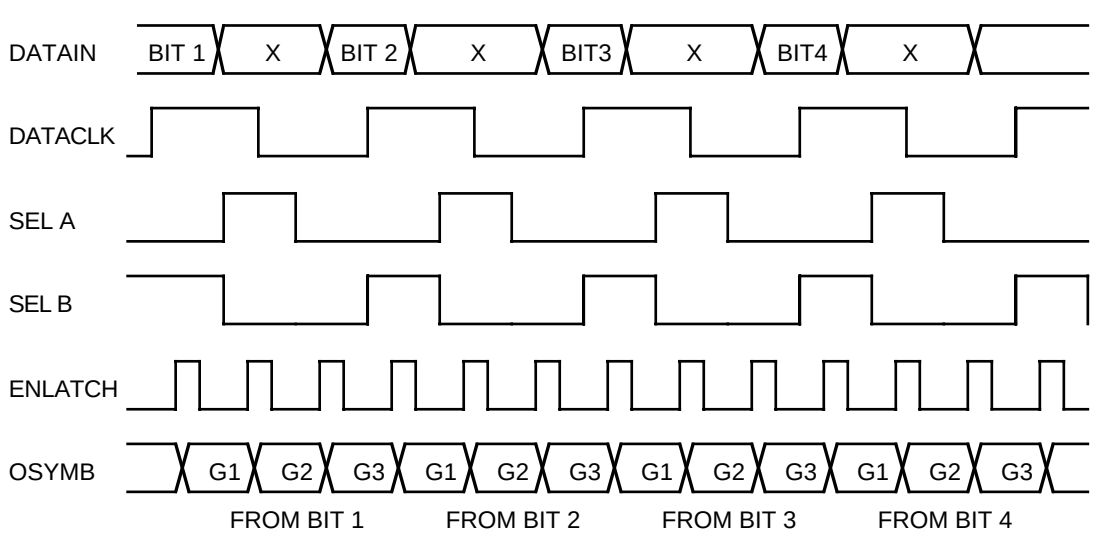
Symbol	Parameter	Commercial		Military		Units
		Min.	Max.	Min.	Max.	
t_{RS}	**RESET** pulse width	$3*t_{CLK}$		$3*t_{CLK}$		nsec.
t_{SR}	**RESET** to **ICLK** setup	2		3		nsec.
t_{DS}	**DATAIN** to **DATACLK** setup	8		10		nsec.
t_{DH}	**DATAIN** to **DATACLK** hold	8		10		nsec.
t_{SS}	**SEL A** or **SEL B** to **ENLATCH** setup	8		10		nsec.
t_{SH}	**SEL A** or **SEL B** to **ENLATCH** hold	4		6		nsec.
t_{DE}	**DATACLK** to **ENLATCH** delay	8		10		nsec.
t_{EOD}	**ENLATCH** to **OSYMB** stable delay		8		10	nsec.

Notes: t_{CLK} = Period of **ICLK** =(1 / f_{CLK}).

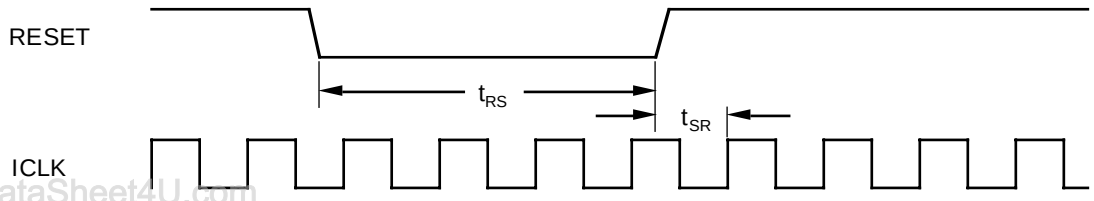
t_{SR} is only relevant if operation is to commence during the first clock cycle after **RESET** goes high.

ENCODER TIMING. MODE = 0 (STEL-5268 EMULATION MODE)

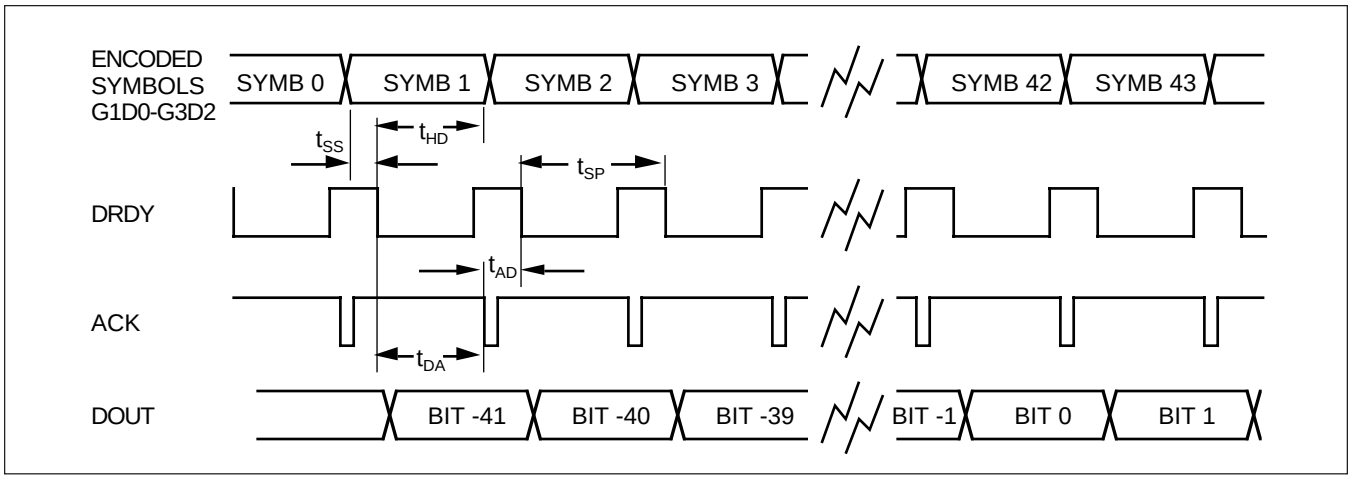


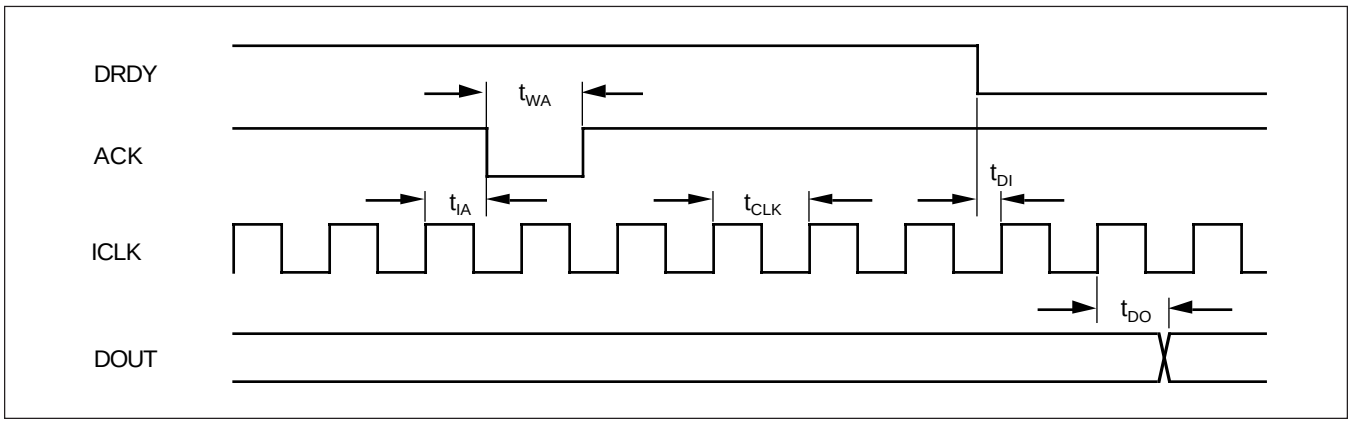


RESET TIMING



DECODER TIMING





DECODER ELECTRICAL CHARACTERISTICS

A.C. CHARACTERISTICS

(Standard Operating Conditions: V_{DD} = 5.0 ± 5% volts, T_a = 0° to 70° C,
Military Operating Conditions: V_{DD} = 5.0 ± 5% volts, T_a = –55° to 125° C)

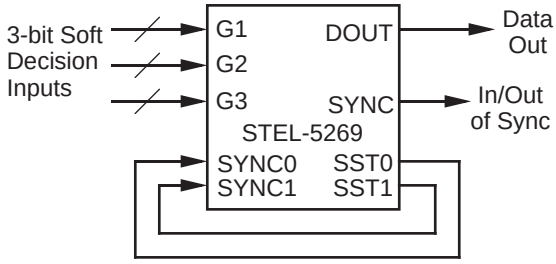
Symbol	Parameter	Commercial		Military		Units
		Min.	Max.	Min.	Max.	
f_{CLK}	**ICLK** Frequency	70*f_{DRDY}	36	70*f_{DRDY}	28	MHz
t_{SS}	**SYMBOL** to **DRDY** setup	16		21		nsec.
t_{HD}	**SYMBOL** to **DRDY** hold	4		6		nsec.
t_{SP}	**SYMBOL** Period	2		2.5		µsec.
t_{DA}	**DRDY** to **ACK**	30 + 68*t_{CLK}	26 + 69*t_{CLK}	30 + 68*t_{CLK}	26 + 69*t_{CLK}	nsec.
t_{AD}	**ACK** to **DRDY**	2*t_{CLK}		2*t_{CLK}		nsec.
t_{WA}	**ACK** pulse width	t_{CLK}		t_{CLK}		nsec.
t_{DI}	**DRDY** to **ICLK** setup	4		6		nsec.
t_{IA}	**ICLK** to **ACK**	8	26	12	32	nsec.
t_{DO}	**ICLK** to **DOUT**	8	30	12	35	nsec.
t_{SR}	**RESET** to **ICLK** setup	2		3		nsec.

Notes: f_{DRDY} = Frequency of **DRDY**, t_{CLK} = Period of **ICLK** =(1/ f_{CLK}).
t_{SR} is only relevant if operation is to commence during the first clock cycle after **RESET** goes high.

APPLICATIONS INFORMATION

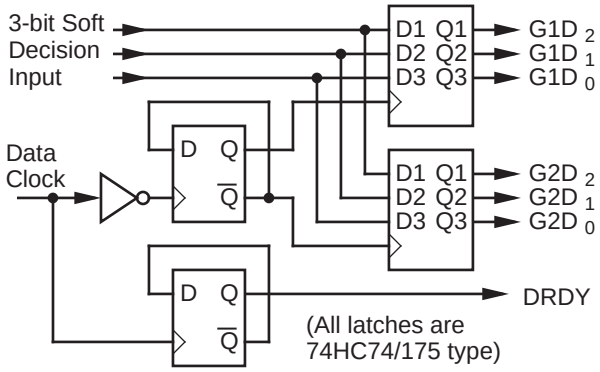
USING AUTOMATIC NODE SYNC

The automatic node sync circuit built into the STEL-5269+512 can be used to provide node sync in applications where this is not intrinsic to the nature of the operation. The automatic node sync is enabled by connecting the **SST1** and **SST0** outputs to the **SYNC1** and **SYNC0** inputs, as shown below. The threshold should be set according to the expected signal to noise ratio of the input signal for optimum operation of the system (see page 6). When **RATE** = 1 (rate $^1/_2$) only one possible alternative state exists in any given situation. This depends on whether the modulation format used was BPSK (sequential symbols) or QPSK (parallel symbol pairs). In this case the node sync process can be improved by only using the **SYNC** input applicable for the corresponding alternative sync state (i.e., **SYNC0** for BPSK, **SYNC1** for QPSK) and tying the other low to prevent the node sync circuit from inadvertently selecting the non-applicable state. When RATE = 0 (rate $^1/_3$) both alternative sync states correspond to those possible with BPSK modulation. Note that whenever the states of the **SYNC0** and **SYNC1** inputs are changed there will be a delay of 42 bit periods before valid data starts appearing at **DOUT**.



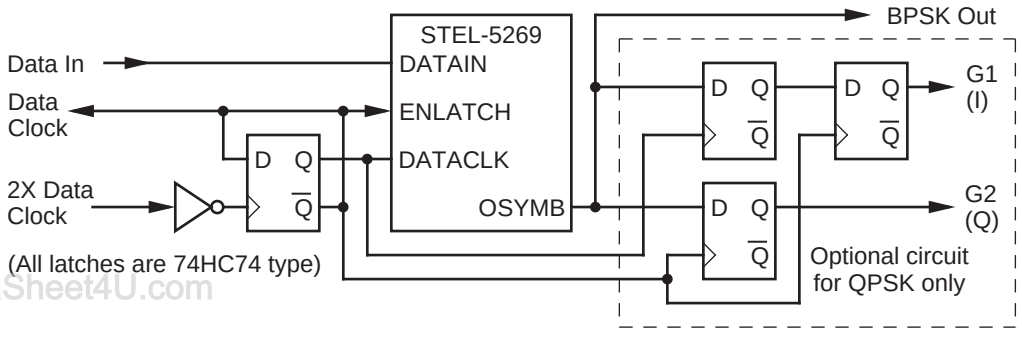
DECODER OPERATION WITH BPSK

The Viterbi decoder is designed to operate with a QPSK demodulator, which provides the G1 and G2 symbols as parallel pairs from the I and Q channels. Operating the device with a BPSK demodulator, which provides the G1 and G2 symbols as sequential pairs, requires some external circuitry to convert the sequential pairs into parallel pairs. The circuit shown here assumes that the symbols are clocked out of the demodulator on the rising edges of the clock signal. The symbol rate clock is divided by 2 to generate a bit rate clock. One phase of the clock is used to latch alternate symbols into the upper 3-bit latch and the opposite phase latches the interleaving symbols into the lower 3-bit latch. The automatic node sync circuit in the STEL-5269 will take care of the symbol ambiguity which occurs in this system. A third clock phase provides the **DRDY** signal to the STEL-5269. Again, the phase ambiguity will be taken care of by the automatic node sync circuit.



ENCODER OPERATION

The encoder section requires a clock at twice the data rate when operating at rate $^1/_2$. A suitable circuit is shown below. The input clock runs at twice the data rate and is divided to produce the data clock itself. The encoder produces serialized symbol pairs suitable for BPSK modulation directly. The optional circuit shown will convert these into parallel pairs suitable for QPSK modulation.

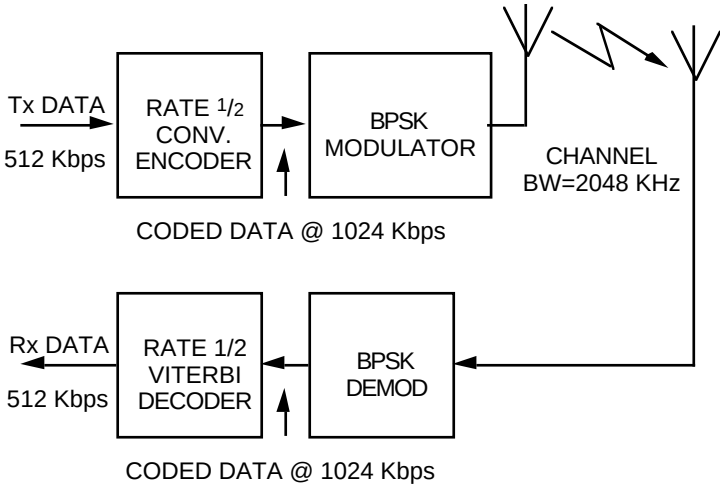


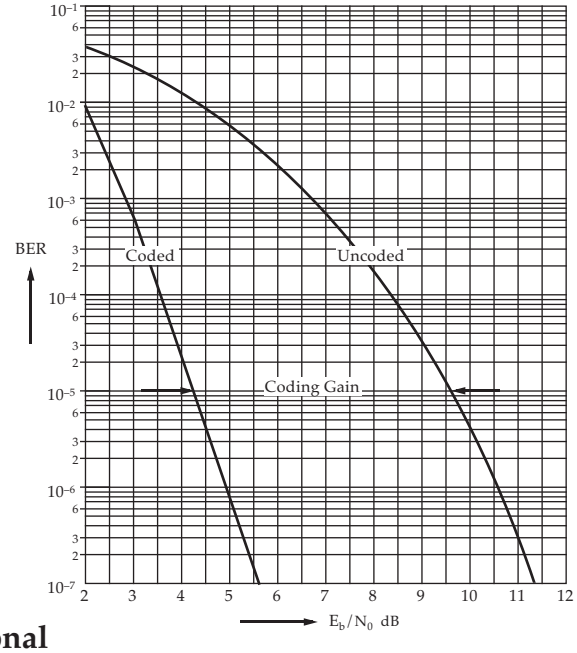
BPSK COMMUNICATION SYSTEM USING CONVOLUTIONAL ENCODING AND VITERBI DECODING. RATE = 1/2

The STEL-5269+512 can be used in a variety of different environments. One example is shown below. It cannot be used as a common encoder or decoder in multichannel applications because of the memory incorporated on the chip which is dedicated to a single channel.

An example of a system using the convolutional coder and Viterbi decoder is illustrated here. The system modulates a data stream of rate 512 Kbps using binary PSK (BPSK). To be able to use convolutional coding/decoding, the system must have available the additional bandwidth needed to transmit symbols at twice the data rate (for rate 1/2 encoding). Alternatively, the system could make use of two parallel channels to transmit two streams of symbols at the data rate. The performance improvement that can be expected is shown in the graph below.

The convolutional encoder is functionally independent from the decoder. A single data bit is clocked into the 7-bit shift register on the rising edge of **DATA CLK**. The decoder portion of the STEL-5269+512 is designed to accept symbols synchronously. **DRDY** is supplied by the user to clock in the symbols. The maximum data rate is 512 Kbps, using a clock frequency of 36 MHz. This corresponds to 512 K symbols per second at rate 1/2 and 768 K symbols per second at rate 1/3. 36 MHz crystals are readily available, and this clock frequency can be used at all data rates, although the power consumption can be reduced by using lower clock frequencies.





BPSK Communication System Using Convolutional Encoding and Viterbi Decoding. Rate = 1/2

For Further Information Call or Write

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