

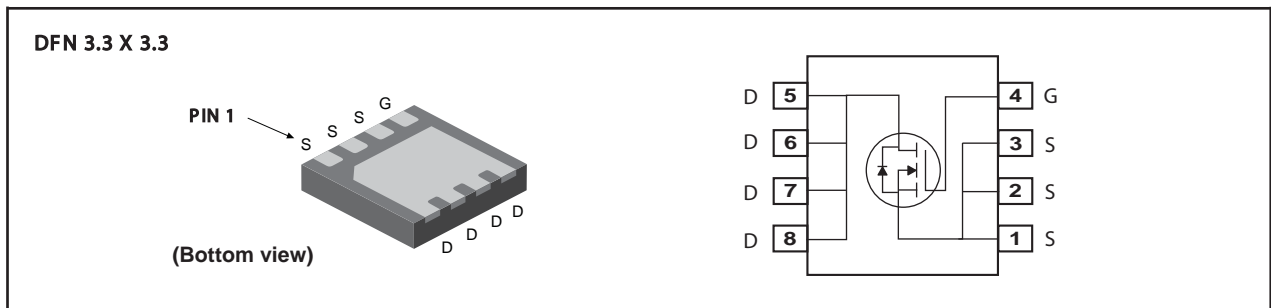


## N-Channel Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY		
V <sub>DSS</sub>	I <sub>D</sub>	R <sub>DS(ON)</sub> (mΩ) Typ
100V	40A	17 @ V <sub>GS</sub> =10V
		19 @ V <sub>GS</sub> =4.5V

### FEATURES

- Super high dense cell design for low R<sub>DS(ON)</sub>.
- Rugged and reliable.
- Surface Mount Package.



### ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub>=25°C unless otherwise noted)

Symbol	Parameter	Limit	Units
V <sub>DS</sub>	Drain-Source Voltage <sup>d</sup>	100	V
V <sub>GS</sub>	Gate-Source Voltage	±20	V
I <sub>D</sub>	Drain Current-Continuous <sup>c</sup>	T <sub>C</sub> =25°C	40
		T <sub>C</sub> =100°C	25.3
		T <sub>A</sub> =25°C	8
I <sub>DM</sub>	-Pulsed <sup>a,c</sup>	160	A
E <sub>AS</sub>	Single Pulse Avalanche Energy <sup>e</sup>	196	mJ
P <sub>D</sub>	Maximum Power Dissipation	T <sub>C</sub> =25°C	62.5
		T <sub>A</sub> =25°C	1.92
T <sub>J</sub> , T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to 150	°C

### THERMAL CHARACTERISTICS

R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient	65	°C/W
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case	2	°C/W

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## ELECTRICAL CHARACTERISTICS (T<sub>C</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage <sup>d</sup>	V <sub>GS</sub> =0V , I <sub>D</sub> =250uA	100			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =80V , V <sub>GS</sub> =0V			1	uA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> = ±20V , V <sub>DS</sub> =0V			±100	nA
<b>ON CHARACTERISTICS</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	1	2	3	V
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance	V <sub>GS</sub> =10V , I <sub>D</sub> =20A		17	19.5	m ohm
		V <sub>GS</sub> =4.5V , I <sub>D</sub> =19A		19	23	m ohm
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =10V , I <sub>D</sub> =20A		71		S
<b>DYNAMIC CHARACTERISTICS <sup>b</sup></b>						
C <sub>ISS</sub>	Input Capacitance	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V f=1.0MHz		2568		pF
C <sub>OSS</sub>	Output Capacitance			190		pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			158		pF
<b>SWITCHING CHARACTERISTICS <sup>b</sup></b>						
t <sub>D(ON)</sub>	Turn-On Delay Time	V <sub>DD</sub> =50V I <sub>D</sub> =1A		48		ns
t <sub>r</sub>	Rise Time			53		ns
t <sub>D(OFF)</sub>	Turn-Off Delay Time	V <sub>GS</sub> =10V R <sub>GEN</sub> = 6 ohm		115		ns
t <sub>f</sub>	Fall Time			24		ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =50V, I <sub>D</sub> =5A, V <sub>GS</sub> =10V		42		nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =50V, I <sub>D</sub> =5A, V <sub>GS</sub> =10V		4		nC
Q <sub>gd</sub>	Gate-Drain Charge			12		nC
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
V <sub>SD</sub>	Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =8A		0.77	1.2	V
<b>Notes</b>						
<p>a. Pulse Test: Pulse Width ≤ 10us, Duty Cycle ≤ 1%.</p> <p>b. Guaranteed by design, not subject to production testing.</p> <p>c. Drain current limited by maximum junction temperature.</p> <p>d. Pulse Test: Pulse Width &lt; 1us, Duty Cycle &lt; 1%.</p> <p>e. Starting T<sub>J</sub>=25°C, L=0.5mH, V<sub>DD</sub> = 50V. (See Figure13)</p> <p>f. Mounted on FR4 Board of 1 inch<sup>2</sup> , 2oz.</p>						

Jul,21,2015

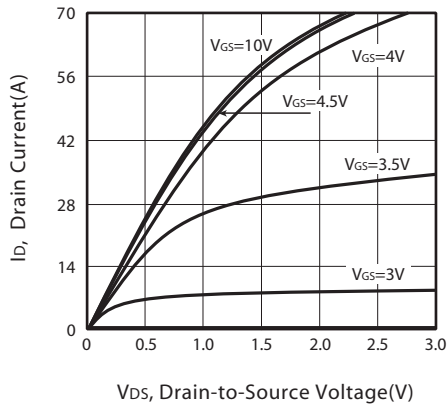


Figure 1. Output Characteristics

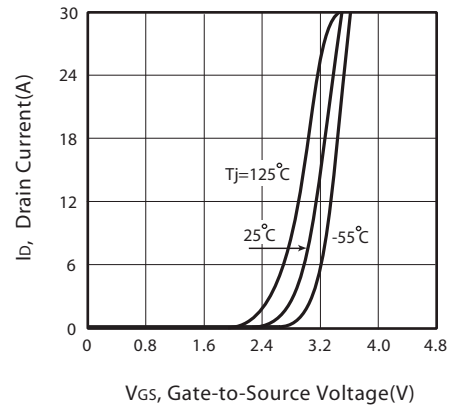


Figure 2. Transfer Characteristics

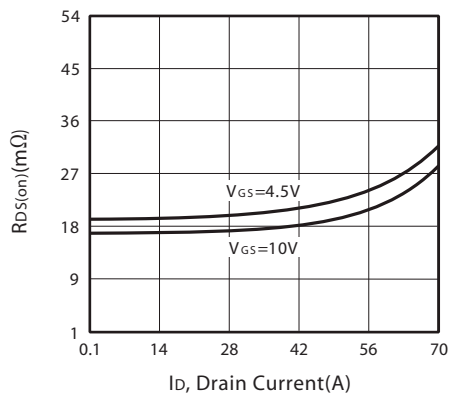


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

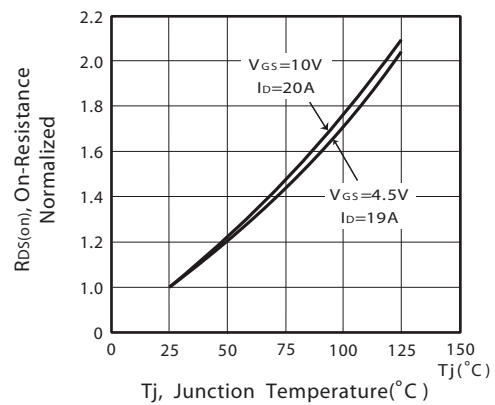


Figure 4. On-Resistance Variation with Drain Current and Temperature

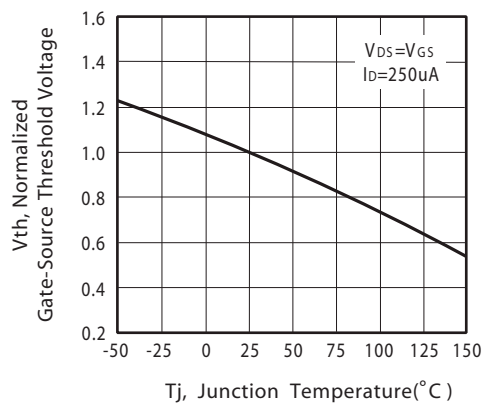


Figure 5. Gate Threshold Variation with Temperature

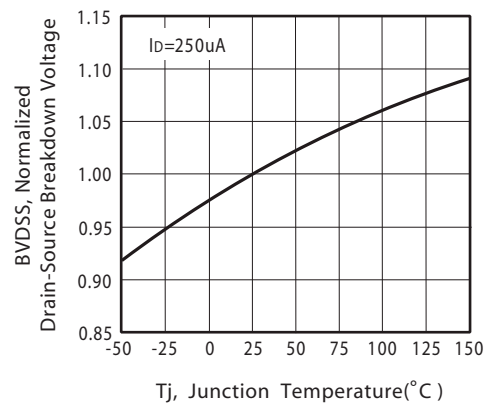


Figure 6. Breakdown Voltage Variation with Temperature

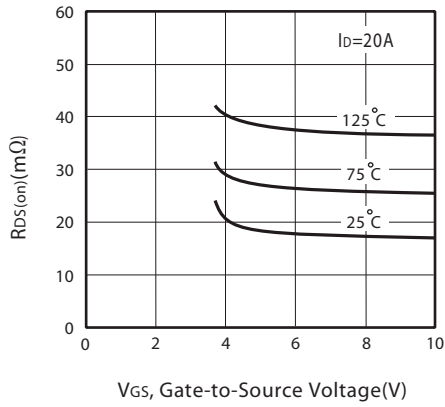


Figure 7. On-Resistance vs. Gate-Source Voltage

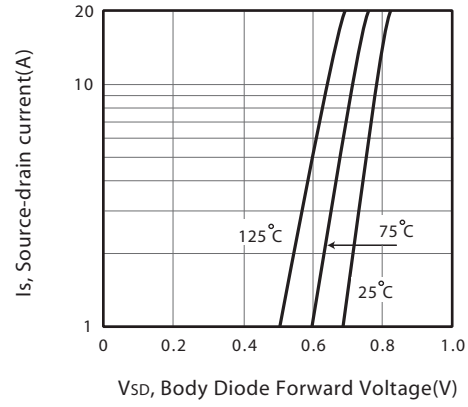


Figure 8. Body Diode Forward Voltage Variation with Source Current

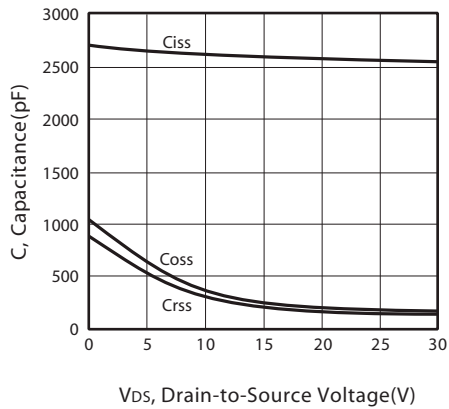


Figure 9. Capacitance

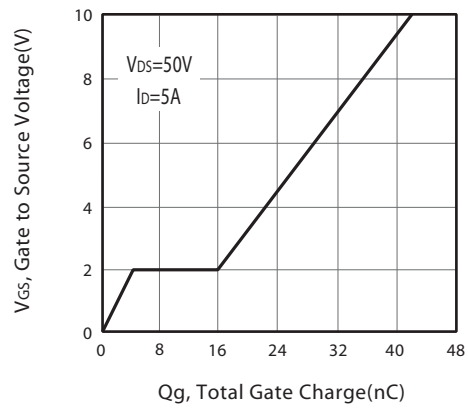


Figure 10. Gate Charge

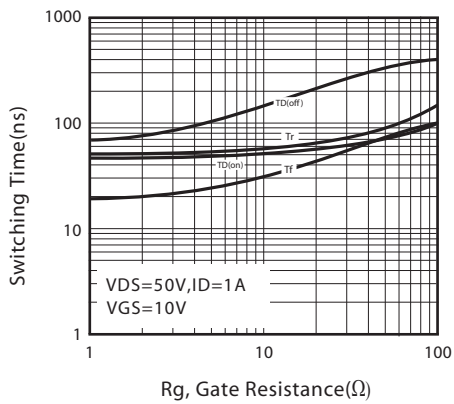


Figure 11. switching characteristics

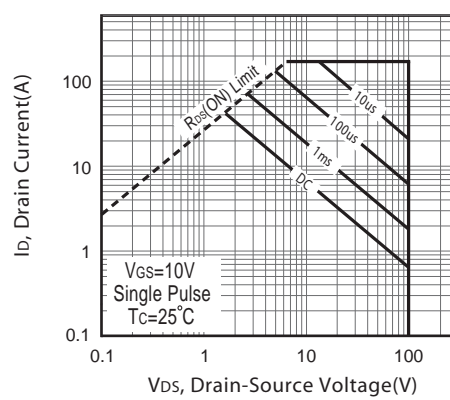
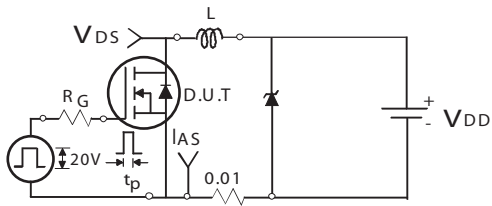
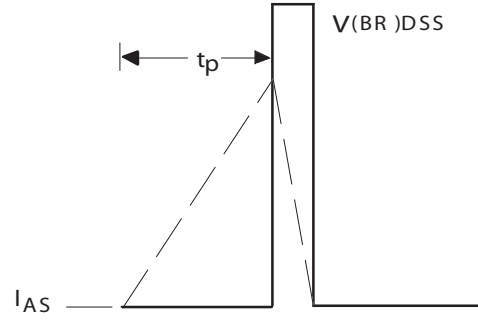


Figure 12. Maximum Safe Operating Area



Unclamped Inductive Test Circuit

Figure 13a.



Unclamped Inductive Waveforms

Figure 13b.

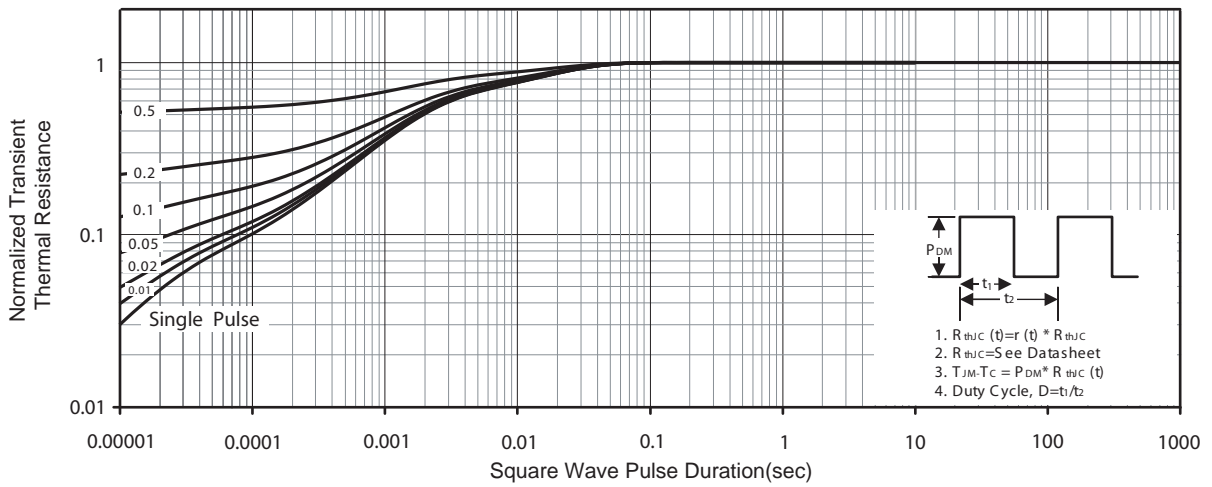


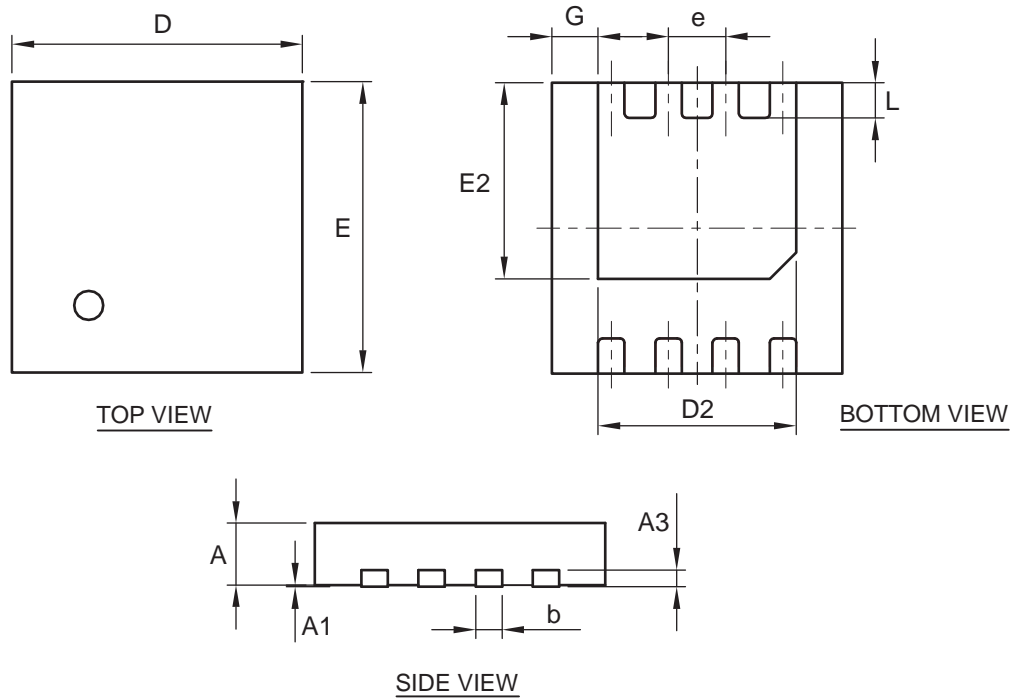
Figure 14. Normalized Thermal Transient Impedance Curve

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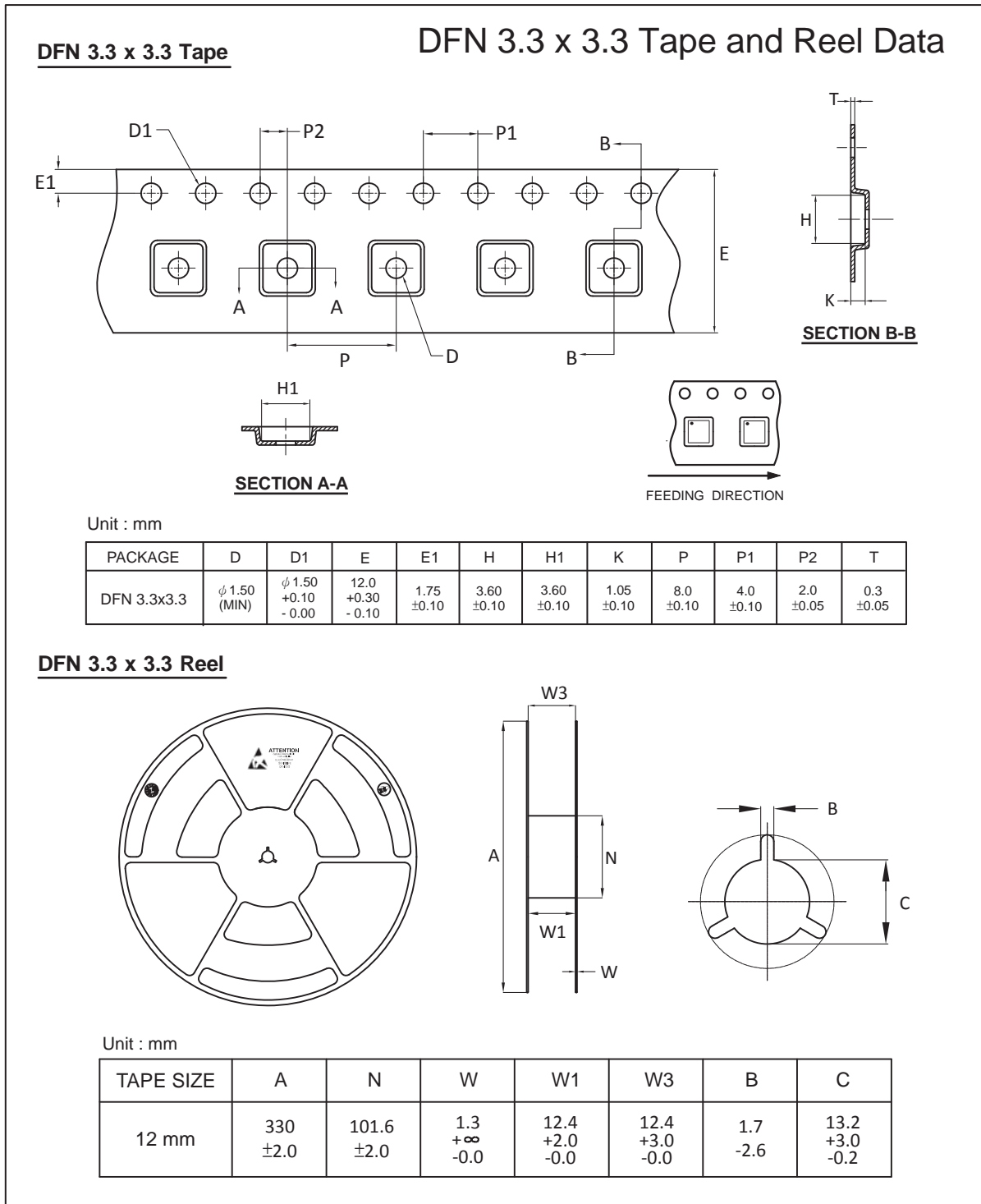
## PACKAGE OUTLINE DIMENSIONS

### DFN 3.3 x 3.3



SYMBOLS	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	—	—	0.05
A3	0.10	0.15	0.25
b	0.24	0.30	0.35
D	3.15	3.30	3.40
D2	2.10	2.25	2.35
E	3.15	3.30	3.40
E2	2.15	2.25	2.35
e	0.60	0.65	0.70
G	0.475	0.525	0.575
L	0.35	0.40	0.45

Jul,21,2015



## TOP MARKING DEFINITION

