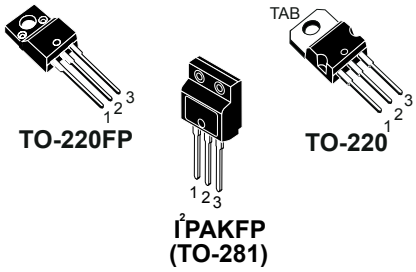
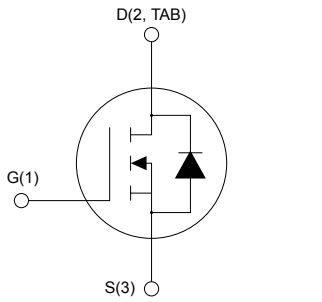
STF11NM65N, STFI11NM65N, STP11NM65N

Datasheet

N-channel 650 V, 425 mΩ typ., 11 A MDmesh II Power MOSFETs in TO-220FP, I²PAKFP and TO-220 packages





Features

Order codes	V_{DS}	$R_{DS(on)}$ max.	I_D
STF11NM65N	650 V	455 mΩ	11 A
STFI11NM65N			
STP11NM65N			

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using the second generation of MDmesh technology. These revolutionary Power MOSFETs associate a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. They are therefore suitable for the most demanding high-efficiency converters.

STPOWER

Product status links
STF11NM65N
STFI11NM65N
STP11NM65N

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		TO-220FP, I²PAKFP	TO-220	
V_{DS}	Drain-source voltage	650		V
V_{GS}	Gate-source voltage	±25		V
I_D	Drain current (continuous) at T_C = 25 °C	11		A
	Drain current (continuous) at T_C = 100 °C	7		
I_{DM} (1)	Drain current (pulsed)	44		A
P_{TOT}	Total power dissipation at T_C = 25 °C	25	110	W
I_{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T_J max)	3		A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	147		mJ
dv/dt (2)	Peak diode recovery voltage slope	15		V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s, T_C = 25 °C)	2.5		kV
T_{stg}	Storage temperature range	-55 to 150		°C
T_J	Operating junction temperature range			°C

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 11 A, di/dt ≤ 400 A/µs, V_{DS} (peak) ≤ $V_{(BR)DSS}$.*

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		TO-220FP, I²PAKFP	TO-220	
R_{thJC}	Thermal resistance, junction-to-case	5	1.14	°C/W
R_{thJA}	Thermal resistance, junction-to-ambient	62.5		°C/W

2 Electrical characteristics

T_C = 25 °C unless otherwise specified.

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	650			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 650 V			1	µA
		V_{GS} = 0 V, V_{DS} = 650 V, T_C = 125 °C (1)			100	
I_{GSS}	Gate body leakage current	V_{GS} = ±25 V, V_{DS} = 0 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 5.5 A		425	455	mΩ

1. *Specified by design, not tested in production.*

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz,V_{GS} = 0 V	-	800	-	pF
C_{oss}	Output capacitance		-	50	-	pF
C_{rss}	Reverse transfer capacitance		-	2.9	-	pF
$C_{oss\ eq.}$ (1)	Equivalent output capacitance	V_{GS} = 0 V, V_{DS} = 0 to 520 V	-	133	-	pF
R_g	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	4.2	-	Ω
Q_g	Total gate charge	V_{DD} = 520 V, I_D = 11 A, V_{GS} = 0 to 10 V (see Figure 16. Test circuit for gate charge behavior)	-	29	-	nC
Q_{gs}	Gate-source charge		-	3.9	-	nC
Q_{gd}	Gate-drain charge		-	16	-	nC

1. *$C_{oss\ eq.}$ is defined as the constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 325 V, I_D = 5.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 15. Test circuit for resistive load switching times and Figure 20. Switching time waveform)	-	15.5	-	ns
t_r	Rise time		-	10.8	-	ns
$t_{d(off)}$	Turn-off delay time		-	11	-	ns
t_f	Fall time		-	47	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		11	A
I_{SDM} (1)	Source-drain current (pulsed)		-		44	A
V_{SD} (2)	Forward on voltage	I_{SD} = 11 A, V_{GS} = 0 V	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 11 A, di/dt = 100 A/µs, V_{DD} = 60 V (see Figure 17. Test circuit for inductive load switching and diode recovery times)	-	418		ns
Q_{rr}	Reverse recovery charge		-	4.4		µC
I_{RRM}	Reverse recovery current		-	21		A
t_{rr}	Reverse recovery time	I_{SD} = 11 A, di/dt = 100 A/µs, V_{DD} = 60 V, T_J = 150 °C (see Figure 17. Test circuit for inductive load switching and diode recovery times)	-	530		ns
Q_{rr}	Reverse recovery charge		-	5.6		µC
I_{RRM}	Reverse recovery current		-	21		A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-220FP and I²PAKFP

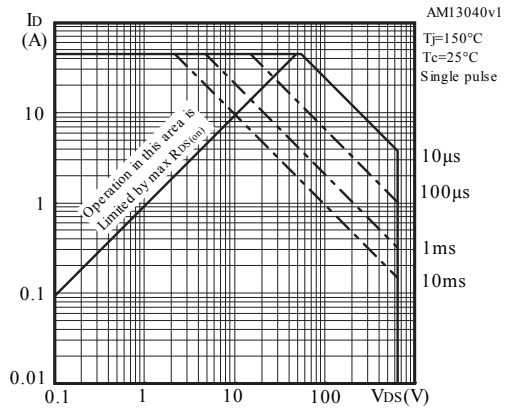


Figure 2. Normalized transient thermal impedance for TO-220FP and I²PAKFP

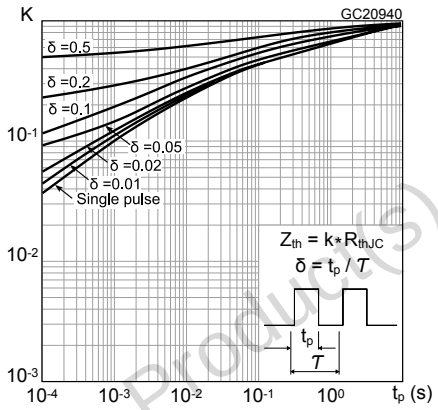


Figure 3. Safe operating area for TO-220

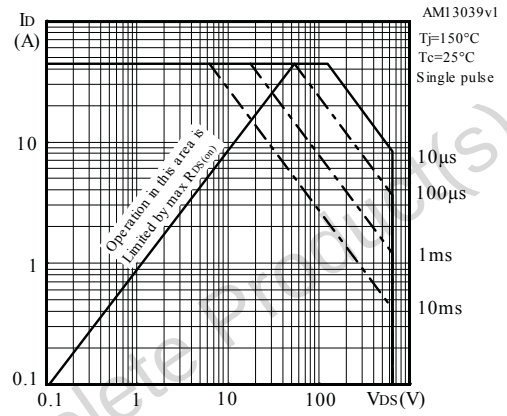


Figure 4. Normalized transient thermal impedance for TO-220

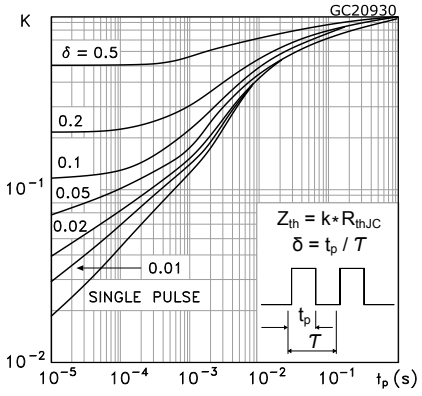


Figure 5. Typical output characteristics

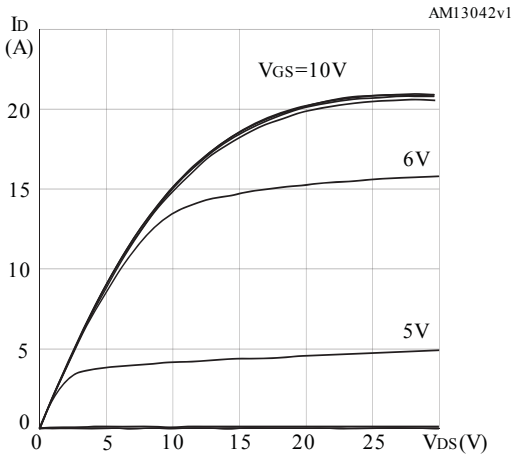


Figure 6. Typical transfer characteristics

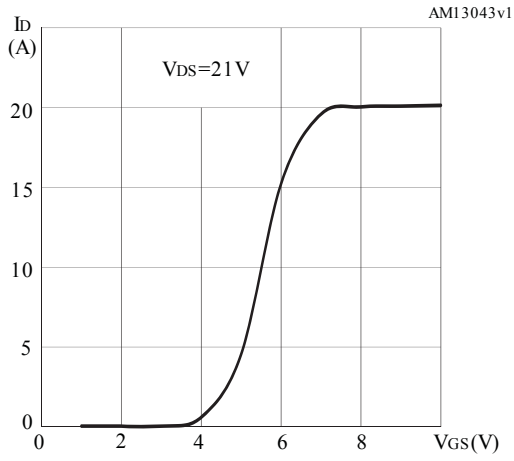


Figure 7. Typical gate charge characteristics

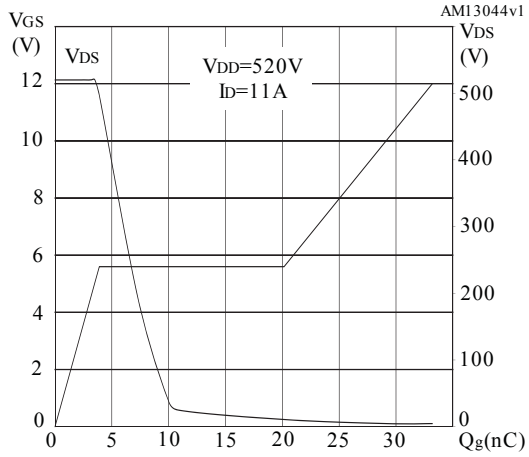


Figure 8. Typical drain-source on-resistance

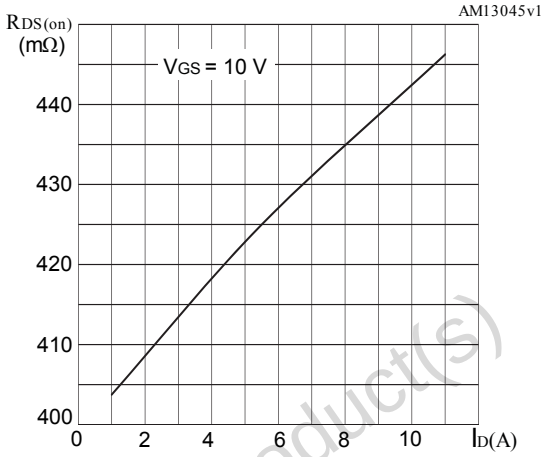


Figure 9. Typical capacitance characteristics

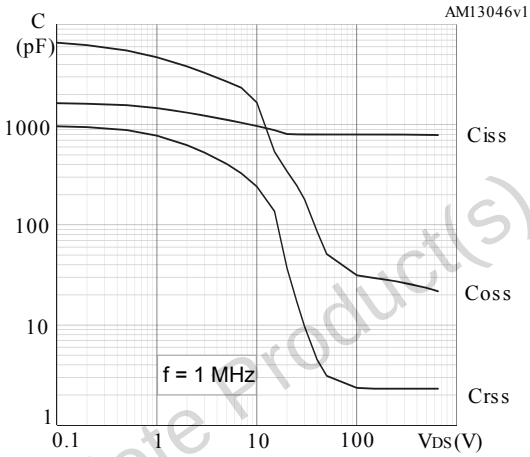


Figure 10. Typical output capacitance stored energy

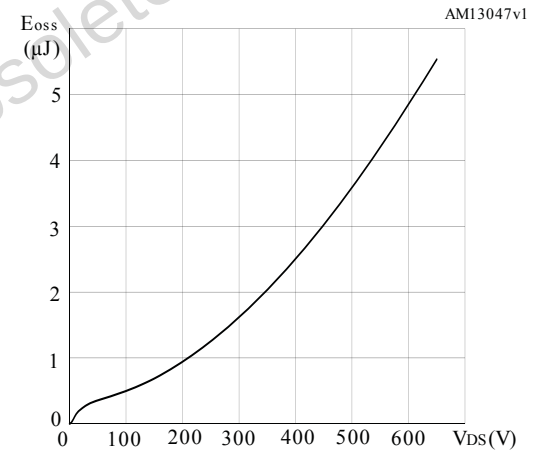


Figure 11. Normalized gate threshold vs temperature

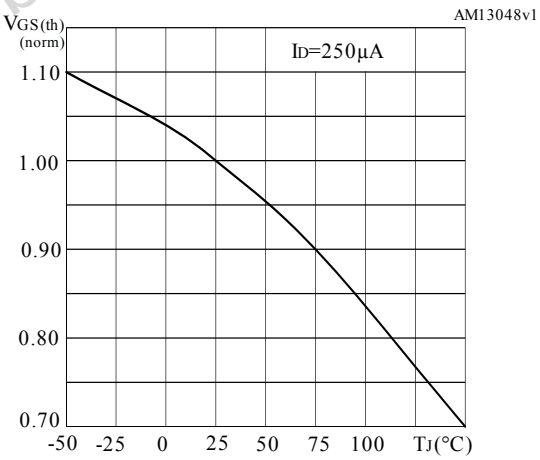


Figure 12. Normalized on-resistance vs temperature

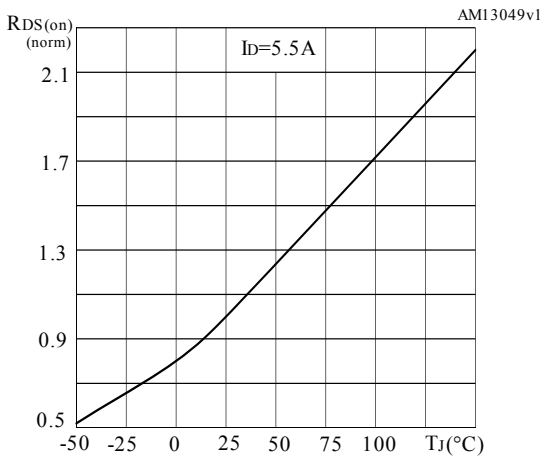


Figure 13. Normalized breakdown voltage vs temperature

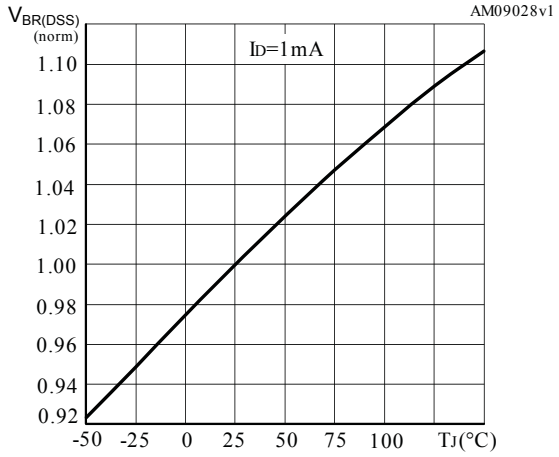
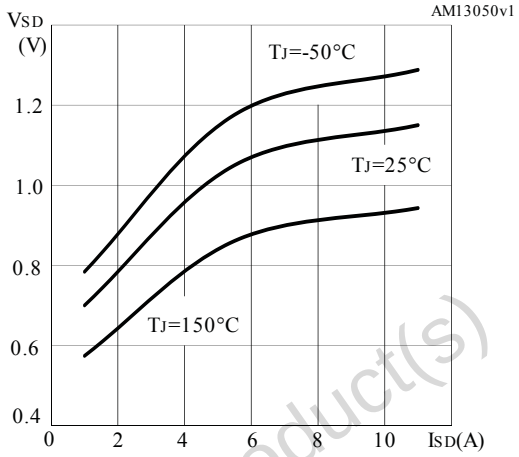


Figure 14. Typical reverse diode forward characteristics



3 Test circuits

Figure 15. Test circuit for resistive load switching times

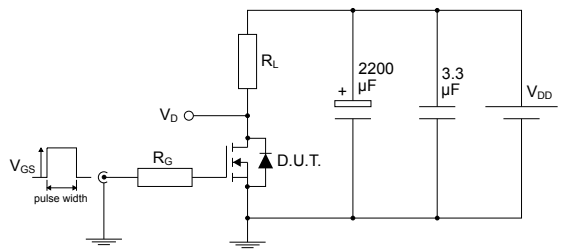


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Figure 16. Test circuit for gate charge behavior

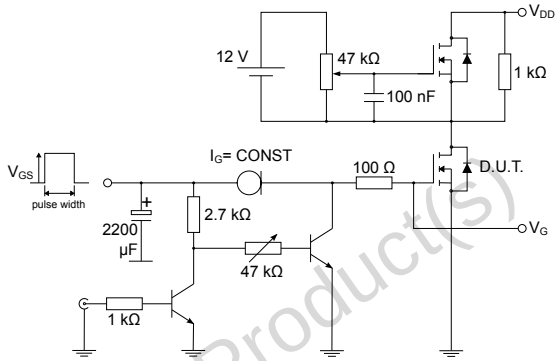

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Figure 17. Test circuit for inductive load switching and diode recovery times

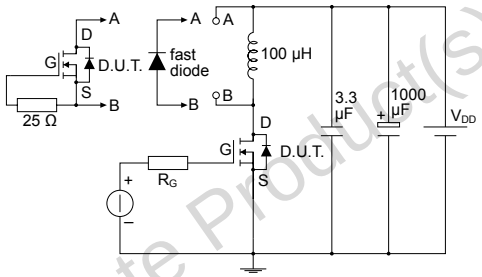

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Figure 18. Unclamped inductive load test circuit

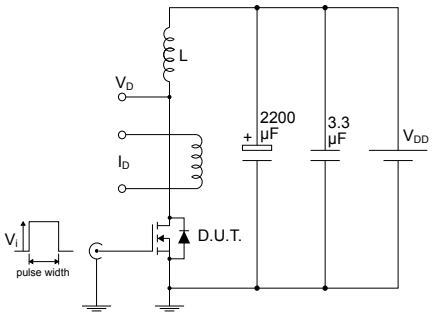

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Figure 19. Unclamped inductive waveform

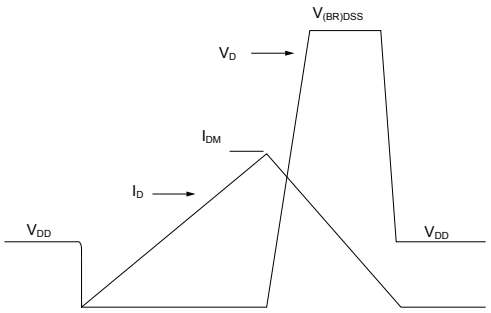

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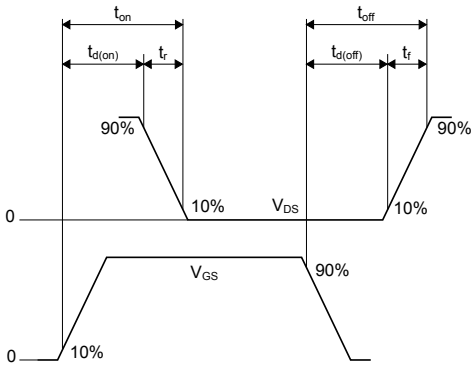
Figure 20. Switching time waveform



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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220FP type B package information

Figure 21. TO-220FP type B package outline

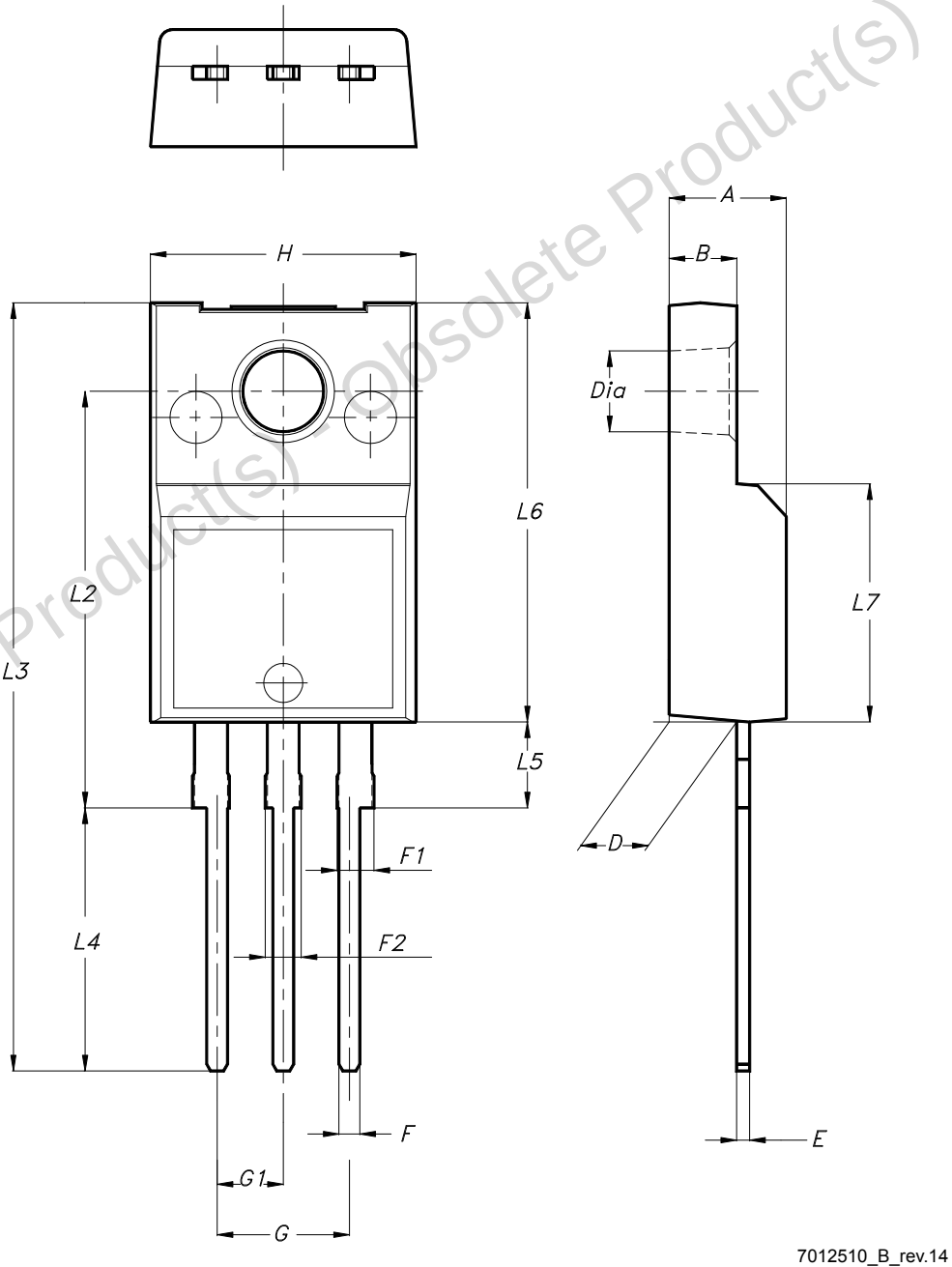

Table 7. **TO-220FP type B package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

4.2 I²PAKFP (TO-281) package information

Figure 22. I²PAKFP (TO-281) package outline

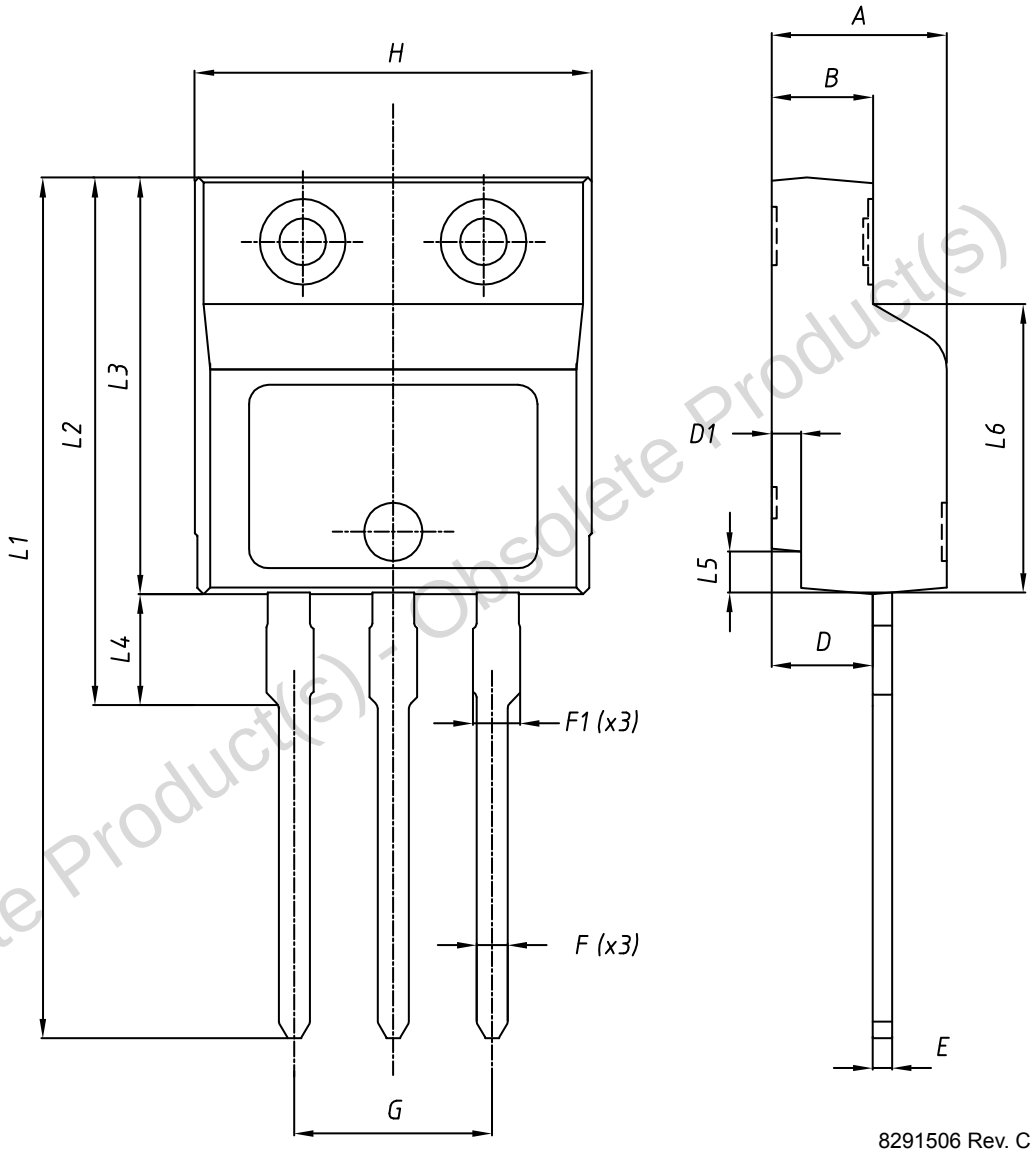

Table 8. I²PAKFP (TO-281) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95		5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.50	7.60	7.70

4.3 TO-220 type A package information

Figure 23. **TO-220 type A package outline**

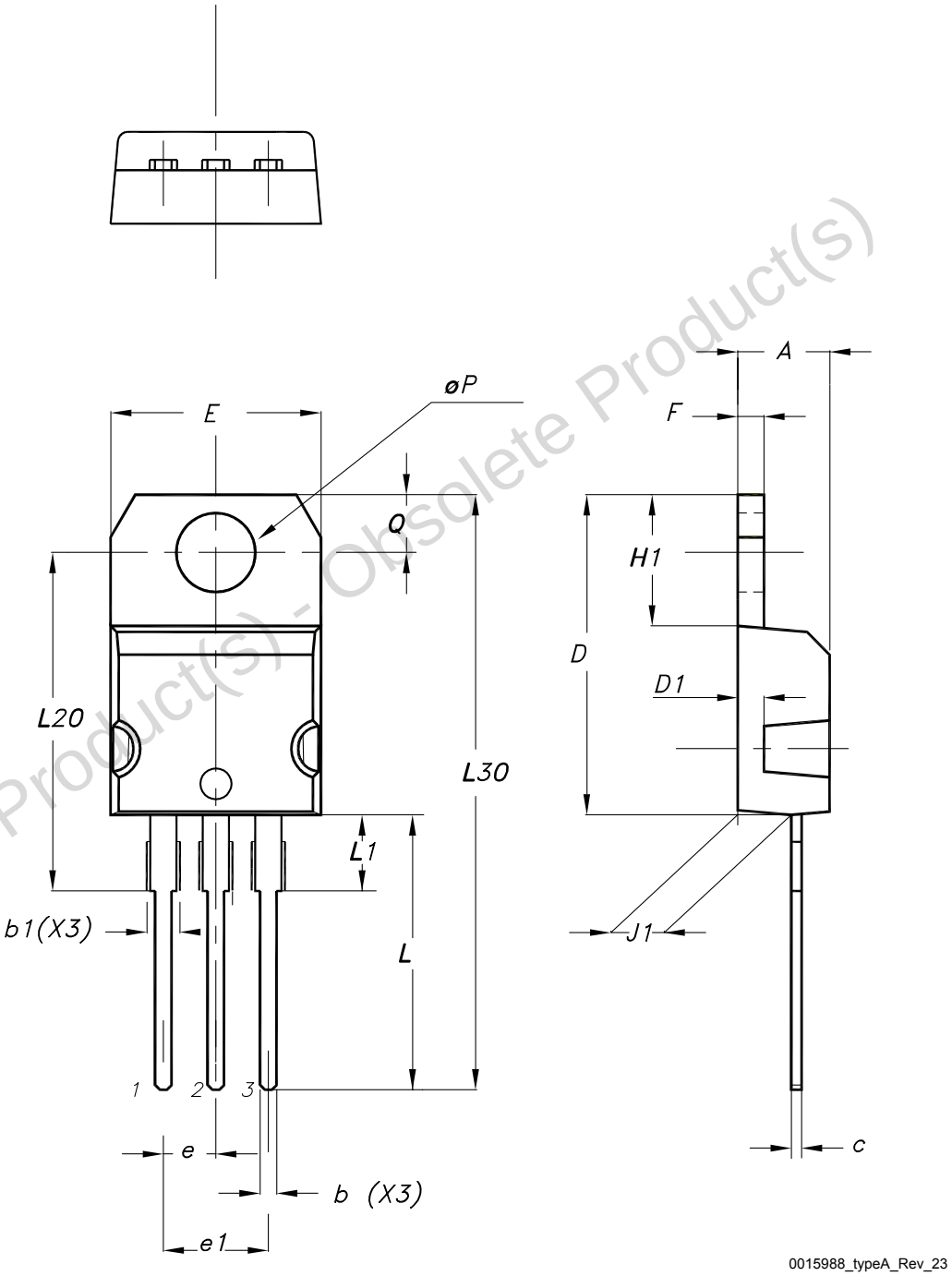

Table 9. **TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

5 Ordering information

Table 10. **Order codes**

Order codes	Marking	Package	Packing
STF11NM65N	11NM65N	TO-220FP	Tube
STFI11NM65N		I²PAKFP	
STP11NM65N		TO-220	

Revision history

Table 11. **Document revision history**

Date	Version	Changes
08-May-2023	1	First release. Part numbers previously included in datasheet DS5257.

Contents