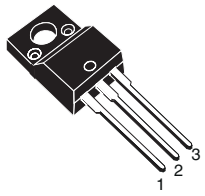
STF12N50U

N-channel 500 V, 0.55 Ω, 10 A TO-220FP Ultrafast MESH™ Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$ max	I_D	Pw
STF12N50U	500 V	< 0.8 Ω	10 A	30 W

- 100% avalanche tested
- Outstanding dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitance
- Very low $R_{DS(on)}$
- Extremely low t_{rr}



TO-220FP

Application

- Switching applications
  - High voltage inverters specific for LCD TV
  - Lighting full bridge topology
  - Motor control

Description

The Ultrafast MESH™ series associates all advantages of reduced on-resistance. Zener gate protection and very high dv/dt capability with an extremely enhanced fast body-drain recovery diode.

Figure 1. Internal schematic diagram

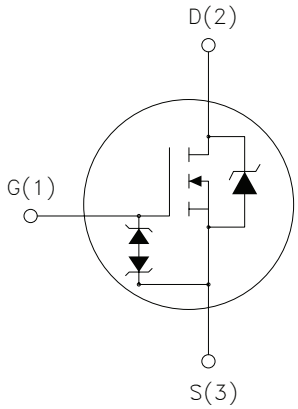


Table 1. Device summary

Order code	Marking	Package	Packaging
STF12N50U	12N50U	TO-220FP	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	500	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at T_C = 25 °C	10 (1)	A
I_D	Drain current (continuous) at T_C = 100 °C	6 (1)	A
I_{DM} (2)	Drain current (pulsed)	40 (1)	A
P_{TOT}	Total dissipation at T_C = 25 °C	30	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	10	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	230	mJ
dv/dt (3)	Peak diode recovery voltage slope	20	V/ns
$V_{ESD-(G-S)}$	G-S EDS (HBM C=100 pF; R=1.5 kΩ)	4000	V
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; Tc = 25 °C)	2500	V
T_{stg}	Storage temperature	-55 to 150	°C
T_j	Max. operating junction temperature	150	°C

1. Current is limited by wire features.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 10$ A, di/dt $\leq$ 400 A/µs, V_{DD} = 80% $V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	4.17	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	°C/W
T_l	Maximum lead temperature for soldering purpose	300	°C

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified).

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	500			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, T_C=125 °C			10 500	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			± 10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	3.75	4.5	V
$R_{DS(on}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 5 A		0.55	0.8	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15 V, I_D = 5 A	-	7		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS} = 0	-	1219 159 40		pF pF pF
$C_{o(tr)}$	Equivalent capacitance time related	V_{GS} = 0, V_{DS} = 0 to 400 V	-	65		pF
$C_{o(er)}$	Equivalent capacitance energy related		-	48		pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	2		Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 400 V, I_D = 10 A, V_{GS} = 10 V (see *Figure 13*)	-	40 7.5 24		nC nC nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r $t_{d(off)}$ t_f	Turn-on delay time Rise time Turn-off-delay time Fall time	V_{DD} = 250 V, I_D = 5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 12*)	-	19 17 43 15	-	ns ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)		-		10 40	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 10 A, V_{GS} = 0	-		1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 10 A, di/dt = 100 A/µs V_{DD} = 35 V (see *Figure 17*)	-	73 182 5		ns nC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 10 A, di/dt = 100 A/µs V_{DD} = 35 V, T_j = 150 °C (see *Figure 17*)	-	118 418 7		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

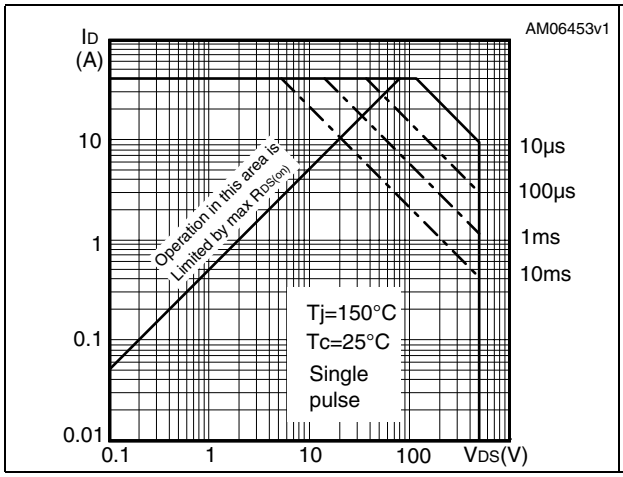


Figure 3. Thermal impedance

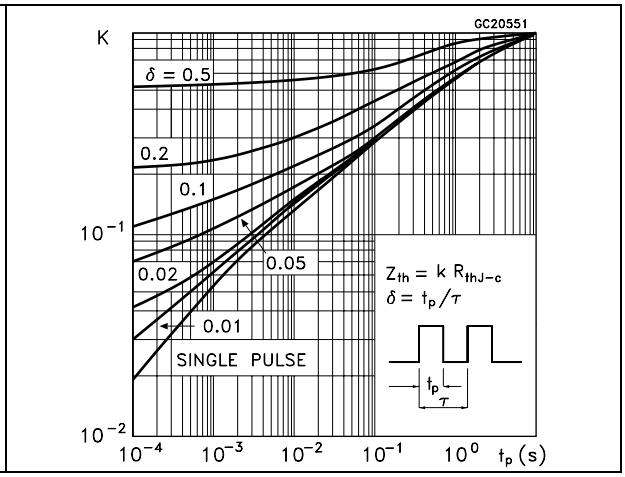


Figure 4. Output characteristics

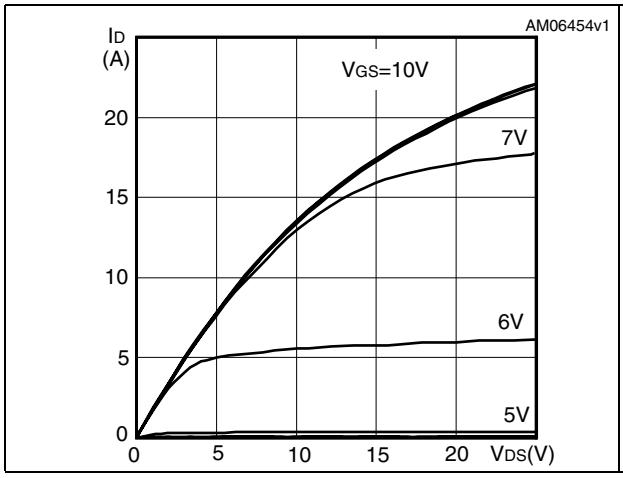


Figure 5. Transfer characteristics

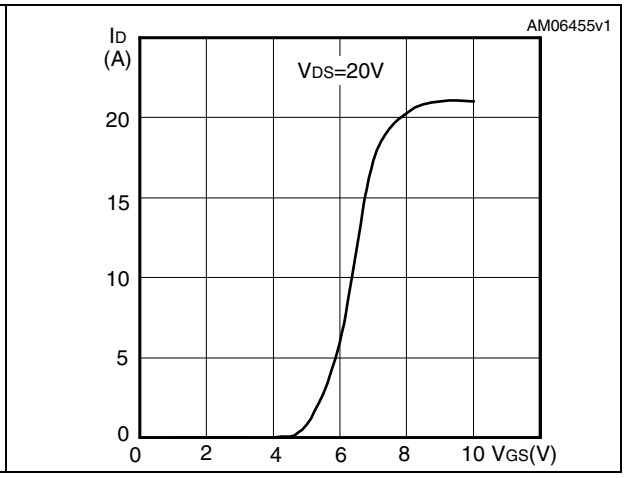


Figure 6. Normalized B_{VDSS} vs temperature

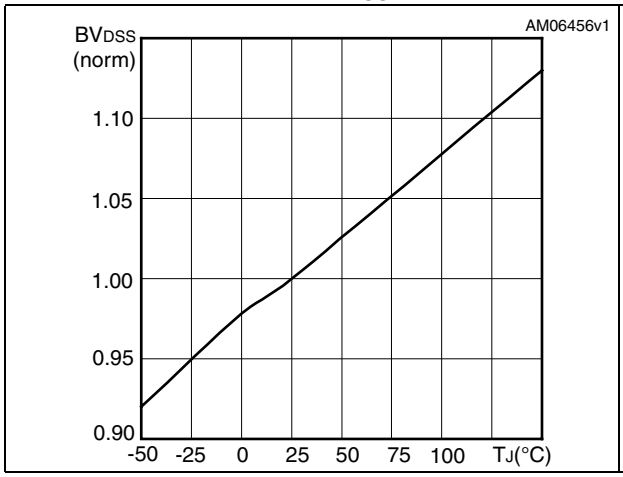


Figure 7. Static drain-source on resistance

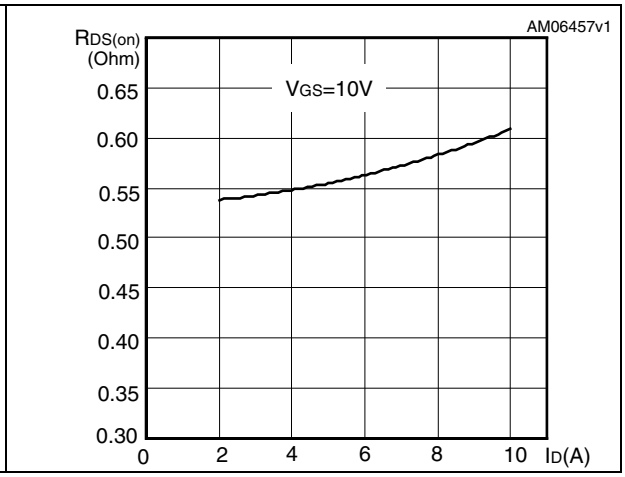


Figure 8. Gate charge vs gate-source voltage

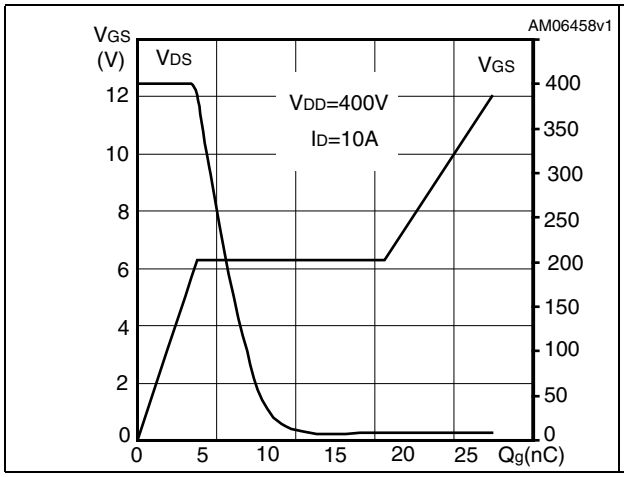


Figure 9. Capacitance variations

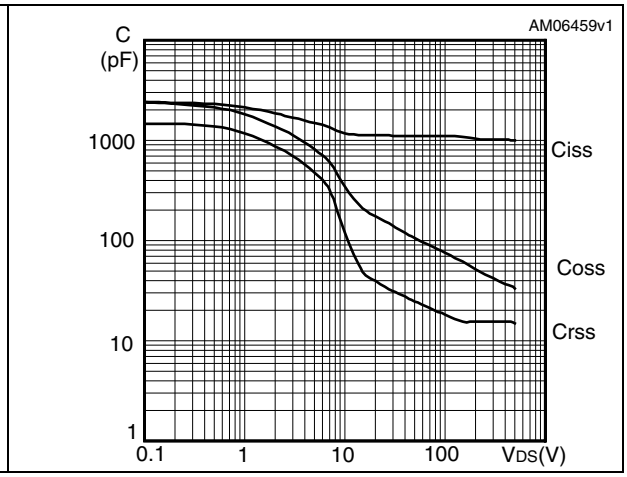


Figure 10. Normalized gate threshold voltage vs temperature

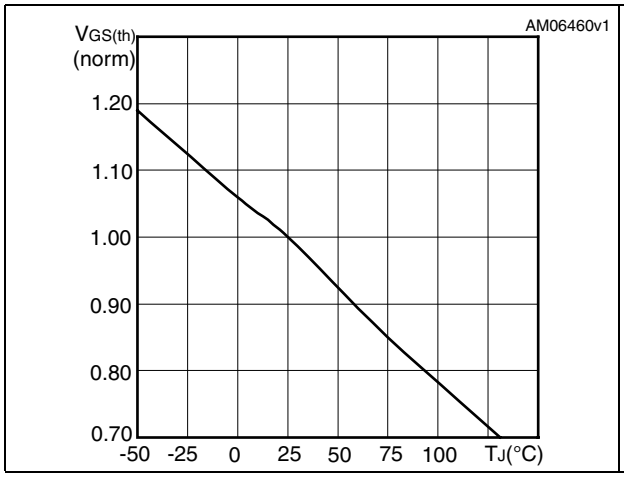
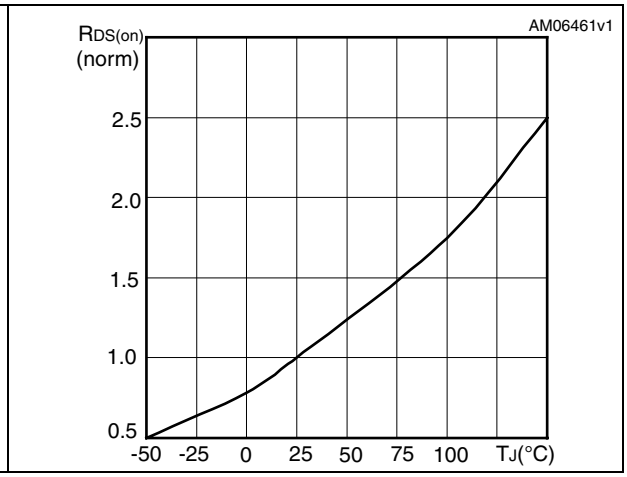


Figure 11. Normalized on resistance vs temperature



3 Test circuits

Figure 12. Switching times test circuit for resistive load

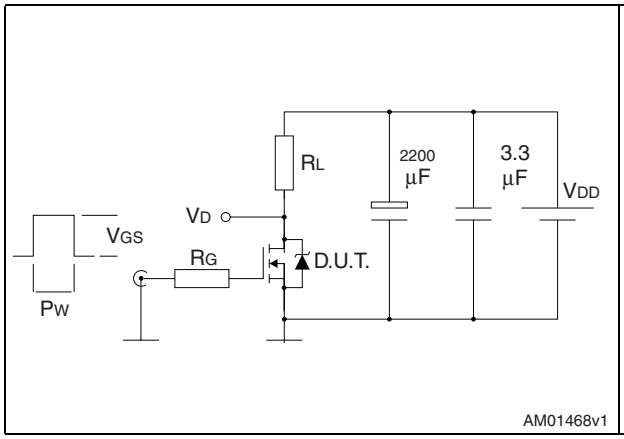


Figure 13. Gate charge test circuit

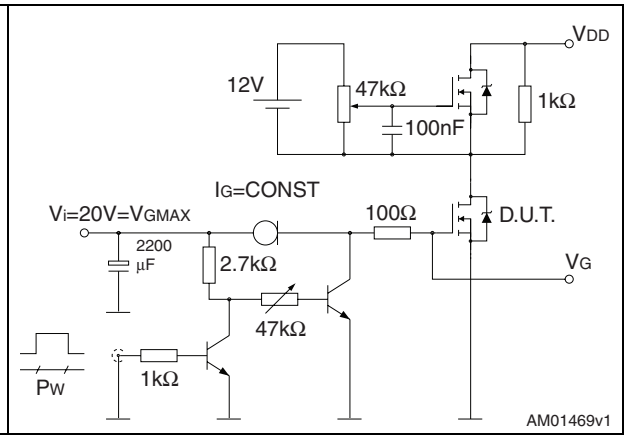


Figure 14. Test circuit for inductive load switching and diode recovery times

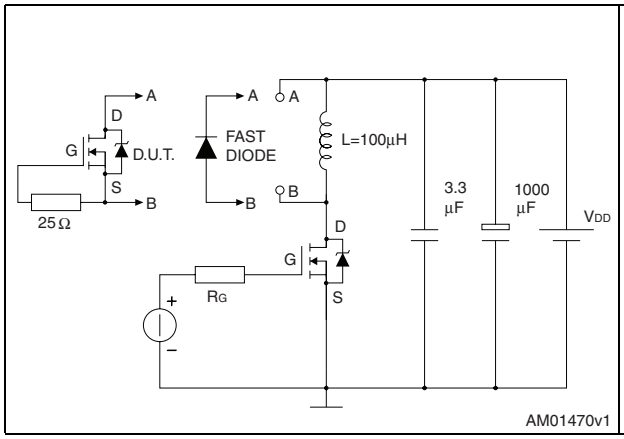


Figure 15. Unclamped inductive load test circuit

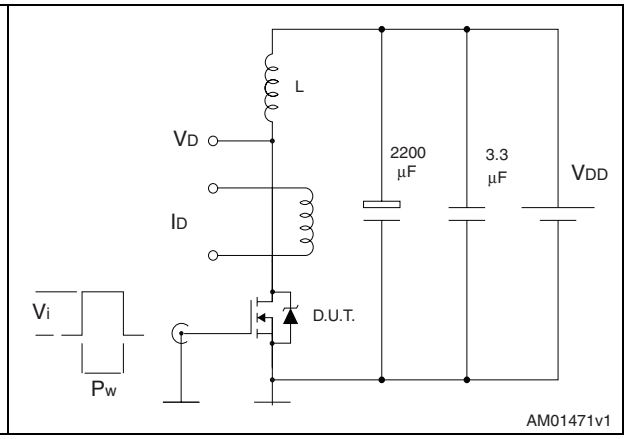


Figure 16. Unclamped inductive waveform

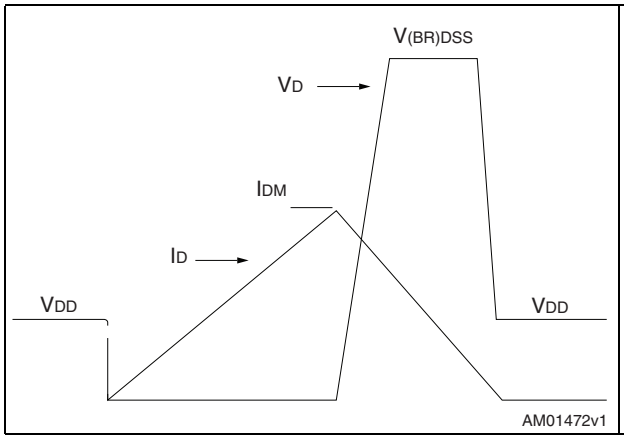
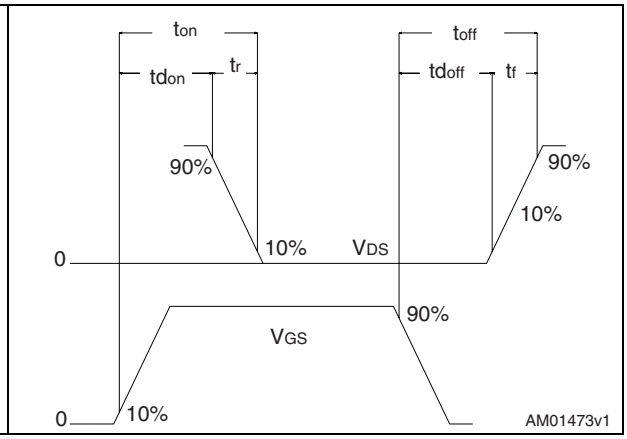


Figure 17. Switching time waveform



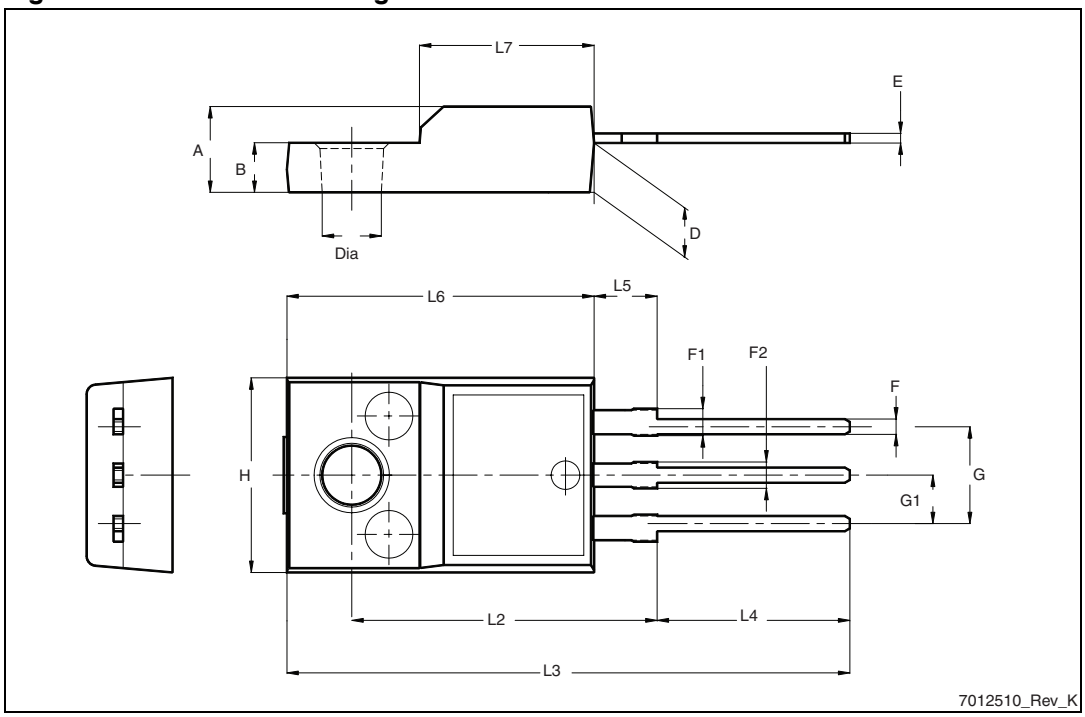
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 8. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 18. TO-220FP drawing



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
15-Mar-2010	1	First release.

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