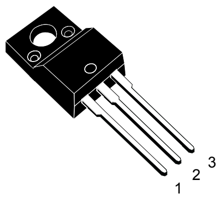
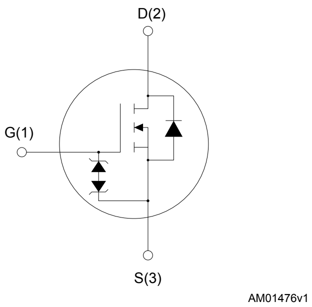
N-channel 600 V, 0.340 Ω typ., 11 A MDmesh™ M2 EP Power MOSFET in a TO-220FP package



TO-220FP



Features

Order code	V_{DS}@T_{Jmax}	$R_{DS(on)}$max.	I_D
STF15N60M2-EP	650 V	0.378 Ω	11 A

- Extremely low gate charge
- Excellent output capacitance (C_{OSS}) profile
- Very low turn-off switching losses
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications
- Tailored for very high frequency converters (f > 150 kHz)

Description

This device is an N-channel Power MOSFET developed using MDmesh™ M2 enhanced performance (EP) technology. Thanks to its strip layout and an improved vertical structure, the device exhibits low on-resistance, optimized switching characteristics with very low turn-off switching losses, rendering it suitable for the most demanding very high frequency converters.

Product status
STF15N60M2-EP

Product summary	
Order code	STF15N60M2-EP
Marking	15N60M2EP
Package	TO-220FP
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D [(1)]	Drain current (continuous) at T_C = 25 °C	11	A
I_D [(1)]	Drain current (continuous) at T_C = 100 °C	7	A
I_{DM} [(2)]	Drain current (pulsed)	44	A
P_{TOT}	Total dissipation at T_C = 25 °C	25	W
dv/dt [(3)]	Peak diode recovery voltage slope	15	V/ns
dv/dt [(4)]	MOSFET dv/dt ruggedness	50	V/ns
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s, T_C = 25 °C)	2500	V
T_{stg}	Storage temperature range	-55 to 150	°C
T_j	Operating junction temperature range		

1. *Limited by maximum junction temperature.*
2. *Pulse width limited by safe operating area.*
3. *I_{SD} ≤ 11 A, di/dt ≤ 400 A/µs, $V_{DS\ peak}$ < $V_{(BR)DSS}$, V_{DD} = 400 V.*
4. *V_{DS} ≤ 480 V*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	5	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	62.5	°C/W

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	2.8	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	125	mJ

2 Electrical characteristics

T_C = 25 °C unless otherwise specified

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	600			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 600 V			1	µA
		V_{GS} = 0 V, V_{DS} = 600 V, T_C = 125 °C(1)			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3.25	4	4.75	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 5.5 A		0.340	0.378	Ω

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS}= 100 V, f = 1 MHz, V_{GS} = 0 V	-	590	-	pF
C_{oss}	Output capacitance		-	30	-	pF
C_{rss}	Reverse transfer capacitance		-	1.1	-	pF
$C_{oss\ eq.}$(1)	Equivalent output capacitance	V_{DS} = 0 to 480 V, V_{GS} = 0 V	-	148	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A	-	7	-	Ω
Q_g	Total gate charge	V_{DD} = 480 V, I_D = 11 A, V_{GS} = 0 to 10 V (see Figure 15. Test circuit for gate charge behavior)	-	17	-	nC
Q_{gs}	Gate-source charge		-	3.1	-	nC
Q_{gd}	Gate-drain charge		-	7.3	-	nC

1. *$C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching energy

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$E_{(off)}$	Turn-off energy (from 90% V_{GS} to 0% I_D)	V_{DD} = 400 V, I_D = 1.5 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	4.7	-	µJ
		V_{DD} = 400 V, I_D = 3.5 A, R_G = 4.7 Ω, V_{GS} = 10 V	-	5.2	-	µJ

Table 7. **Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 300 V, I_D = 5.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	11	-	ns
t_r	Rise time		-	10	-	ns
$t_{d(off)}$	Turn-off delay time		-	40	-	ns
t_f	Fall time		-	15	-	ns

Table 8. **Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		11	A
I_{SDM} (1)	Source-drain current (pulsed)		-		44	A
V_{SD} (2)	Forward on voltage	V_{GS} = 0 V, I_{SD} = 11 A	-		1.6	V
t_{rr}	Reverse recovery time	I_{SD} = 11 A, di/dt = 100 A/μs, V_{DD} = 60 V (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	280		ns
Q_{rr}	Reverse recovery charge		-	2.7		μC
I_{RRM}	Reverse recovery current		-	19.5		A
t_{rr}	Reverse recovery time	I_{SD} = 11 A, di/dt = 100 A/μs, V_{DD} = 60 V, T_j = 150 °C (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	400		ns
Q_{rr}	Reverse recovery charge		-	3.8		μC
I_{RRM}	Reverse recovery current		-	19		A

1. *Pulse width is limited by safe operating area.*
2. *Pulsed: pulse duration = 300 μs, duty cycle 1.5%*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

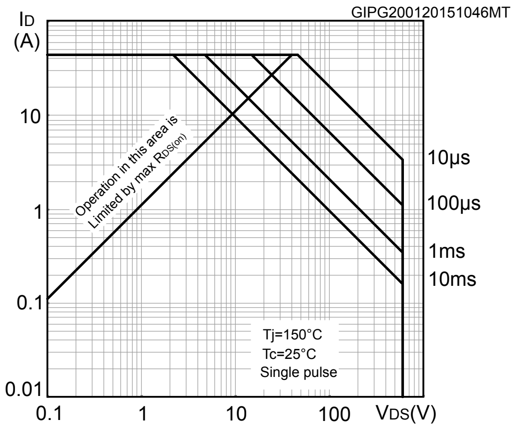


Figure 2. Thermal impedance

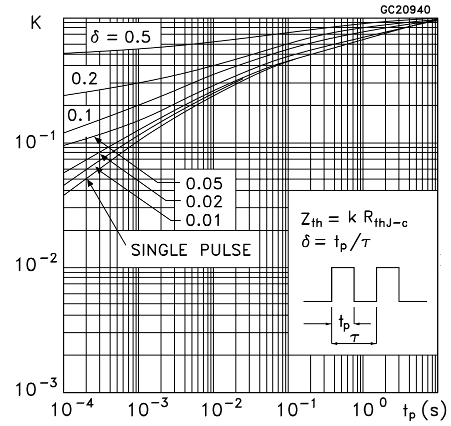


Figure 3. Output characteristics

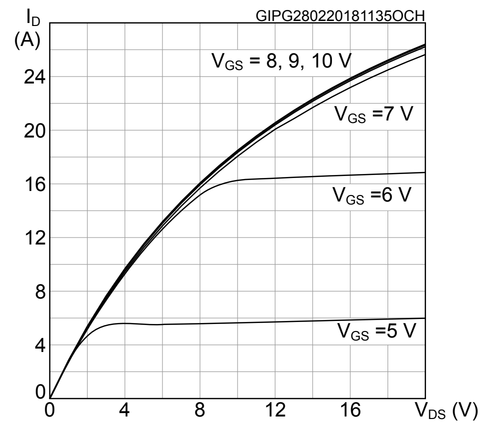


Figure 4. Transfer characteristics

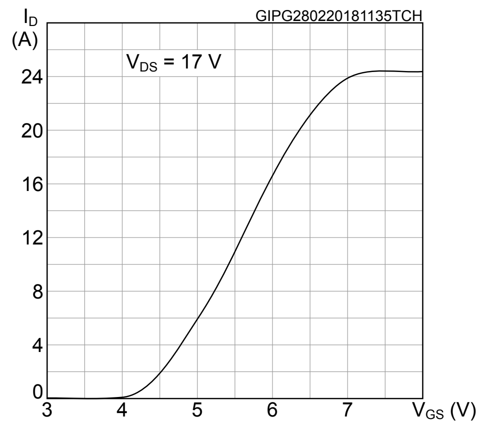


Figure 5. Normalized gate threshold voltage vs temperature

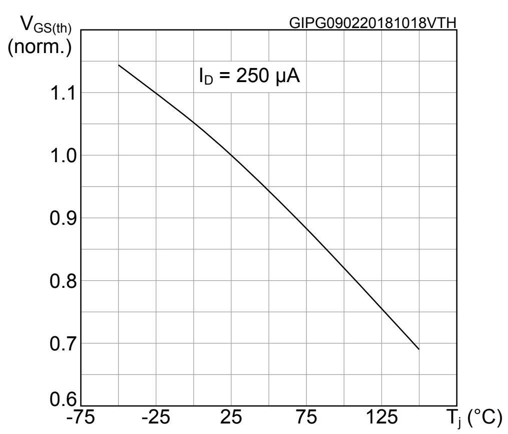


Figure 6. Normalized $V_{(BR)DSS}$ vs temperature

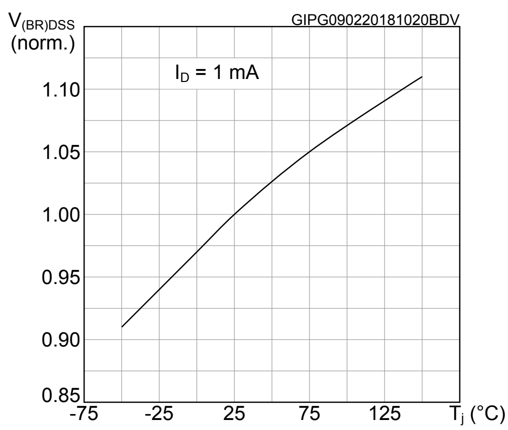


Figure 7. Static drain-source on-resistance

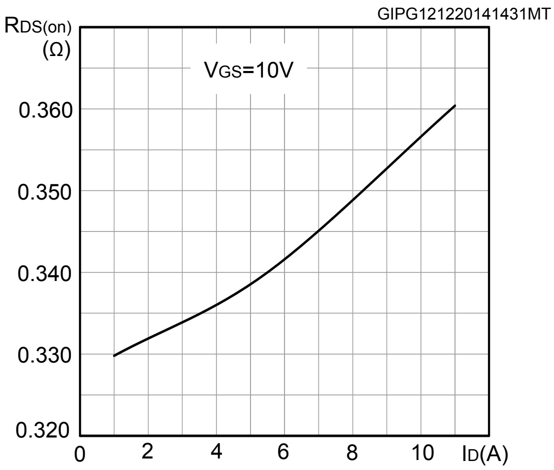


Figure 8. Normalized on-resistance vs temperature

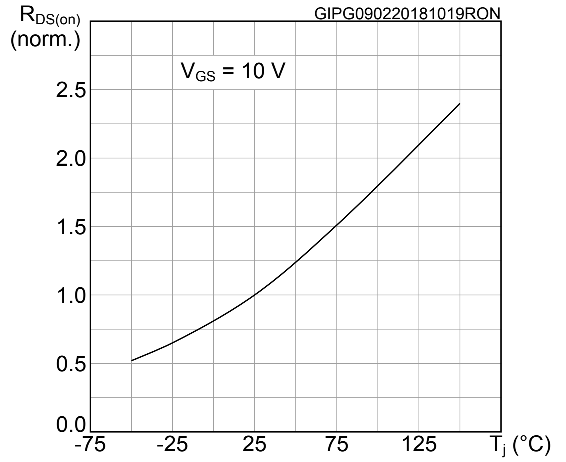


Figure 9. Gate charge vs gate-source voltage

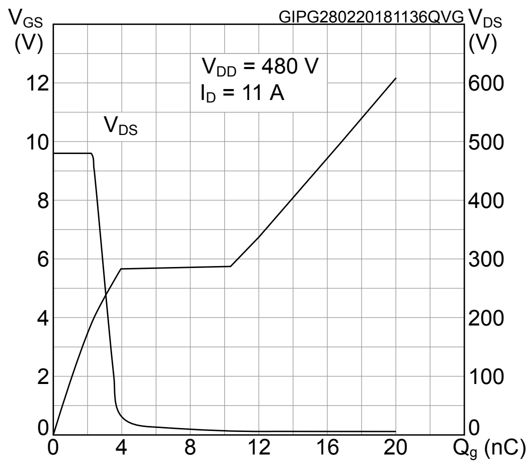


Figure 10. Capacitance variations

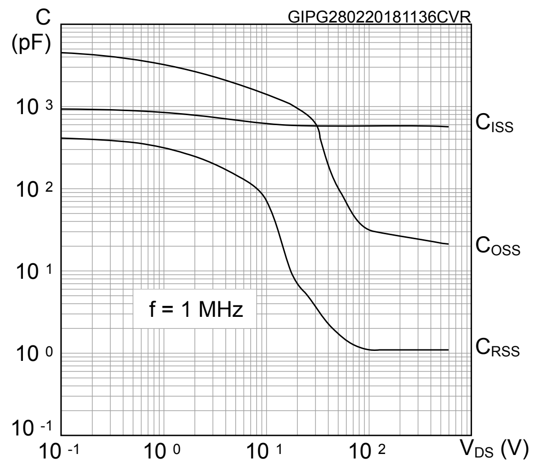


Figure 11. Turn-off switching energy vs drain current

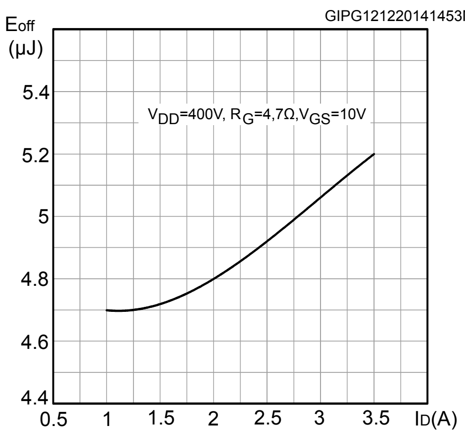


Figure 12. Source-drain diode forward characteristic

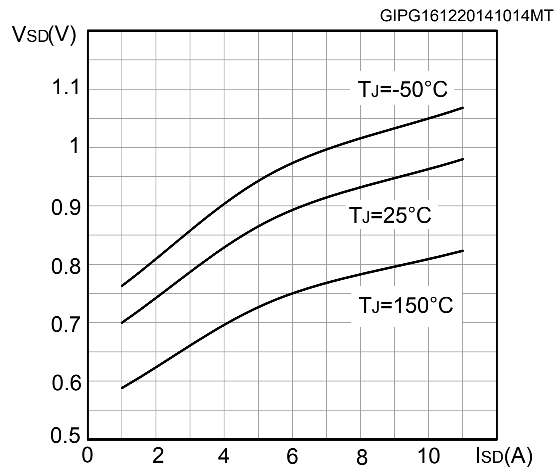
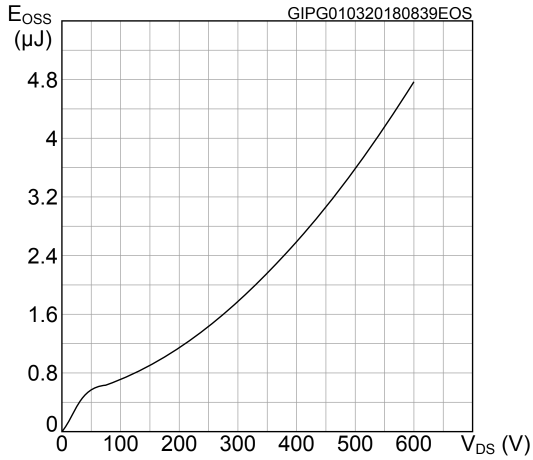


Figure 13. **Output capacitance stored energy**



3 Test circuits

Figure 14. Test circuit for resistive load switching times

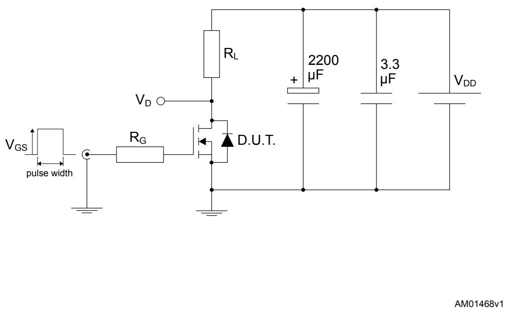


Figure 15. Test circuit for gate charge behavior

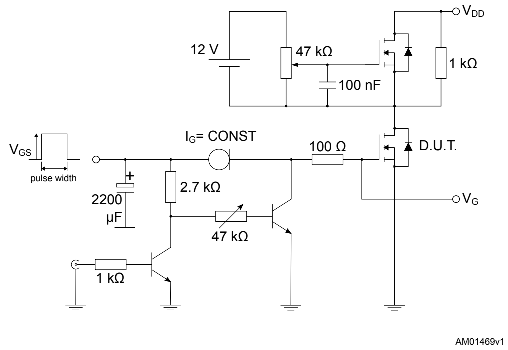


Figure 16. Test circuit for inductive load switching and diode recovery times

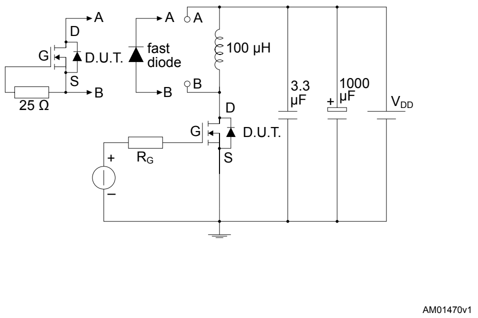


Figure 17. Unclamped inductive load test circuit

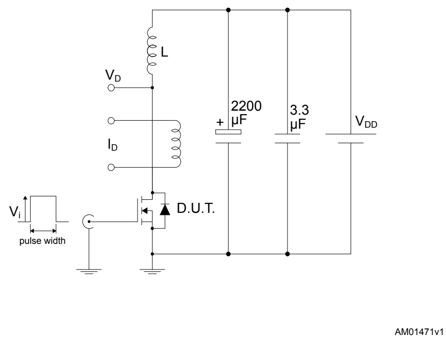


Figure 18. Unclamped inductive waveform

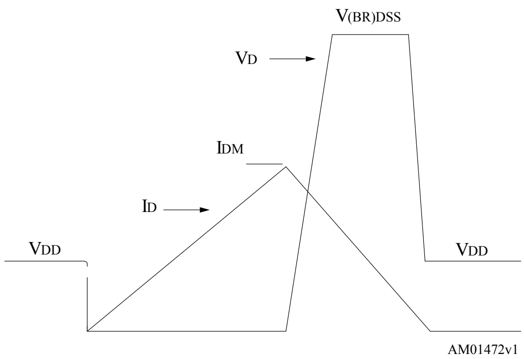
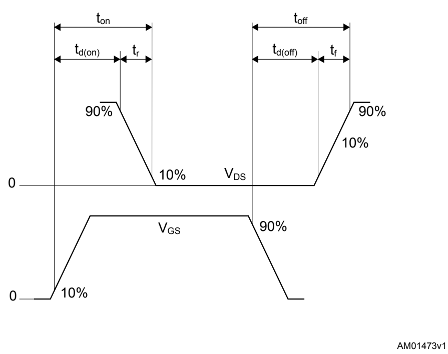


Figure 19. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-220FP package information

Figure 20. **TO-220FP package outline**

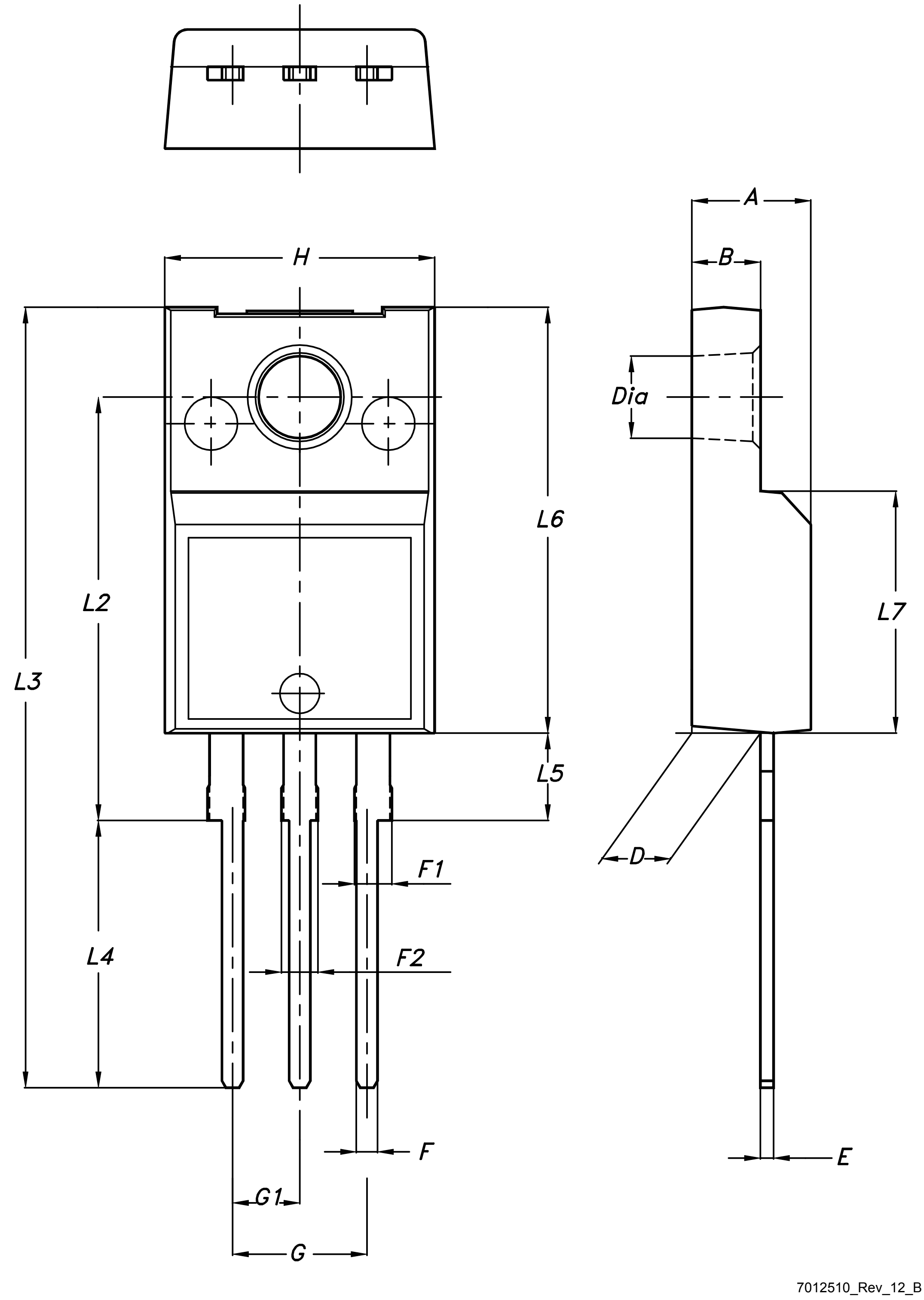


Table 9. **TO-220FP package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Revision history

Table 10. **Document revision history**

Date	Revision	Changes
26-Jan-2015	1	First release.
08-Mar-2018	2	The part number STFI15N60M2-EP has been moved to a separate datasheet and document updated accordingly. Removed maturity status indication from cover page. The document status is production data. Updated *Section 2.1 Electrical characteristics (curves)*. Minor text changes.
05-Jun-2018	3	Updated Table 1. Absolute maximum ratings, Table 5. Dynamic, Table 6. Switching energy and Table 8. Source drain diode. Updated Figure 1. Safe operating area, Figure 2. Thermal impedance and Figure 11. Turn-off switching energy vs drain current. Minor text changes

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