



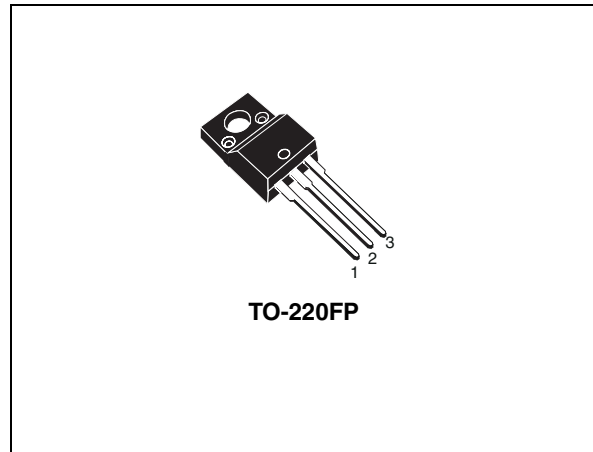
STF16N50U

N-channel 500 V, 0.47 Ω , 15 A TO-220FP
UltraFAST MESH™ Power MOSFET

Features

Type	V _{DSS} @ T _{jmax.}	R _{DS(on)} max.	I _D	P _w
STF16N50U	550 V	< 0.52 Ω	15 A	30 W

- 100% avalanche tested
- Outstanding dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitance
- Very low R_{DS(on)}
- Extremely low t_{rr}



Application

- Switching applications
 - High voltage inverters specific for LCD TV
 - Lighting full bridge topology
 - Motor control

Description

The device is an N-channel Ultrafast MESH™. This technology associates all advantages of reduced on-resistance. Zener gate protection and very high dv/dt capability with an extremely enhanced fast body-drain recovery diode.

Figure 1. Internal schematic diagram

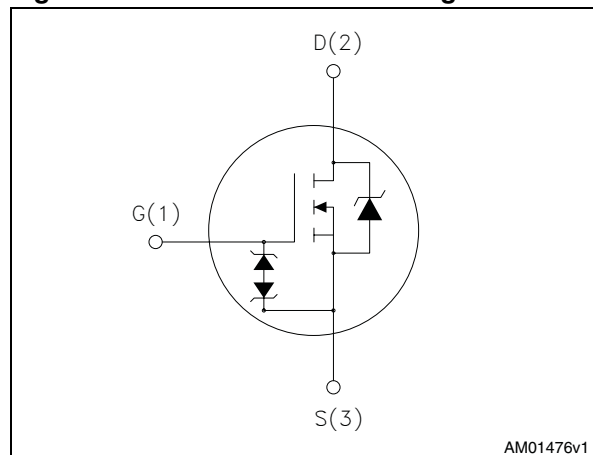


Table 1. Device summary

Order code	Marking	Package	Packaging
STF16N50U	16N50U	TO-220FP	Tube

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
	2.1 Electrical characteristics (curves)	6
3	Test circuits	8
4	Package mechanical data	9
5	Revision history	11

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	500	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_C = 25\text{ °C}$	15 ⁽¹⁾	A
I_D	Drain current (continuous) at $T_C = 100\text{ °C}$	9 ⁽¹⁾	A
I_{DM} ⁽²⁾	Drain current (pulsed)	60 ⁽¹⁾	A
P_{TOT}	Total dissipation at $T_C = 25\text{ °C}$	30	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	11	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ °C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	250	mJ
dv/dt ⁽³⁾	Peak diode recovery voltage slope	20	V/ns
$V_{ESD-(G-S)}$	G-S EDS (HBM $C=100\text{ pF}$; $R=1.5\text{ k}\Omega$)	4000	V
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink ($t = 1\text{ s}$; $T_C = 25\text{ °C}$)	2500	V
T_{stg}	Storage temperature	-55 to 150	$^{\circ}\text{C}$
T_j	Max. operating junction temperature	150	$^{\circ}\text{C}$

1. Current is limited by wire features.
2. Pulse width limited by safe operating area.
3. $I_{SD} \leq 11\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{DD} = 80\% V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	3.29	$^{\circ}\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	$^{\circ}\text{C}/\text{W}$
T_l	Maximum lead temperature for soldering purpose	300	$^{\circ}\text{C}$

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified).

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	500			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$, $T_C = 125\text{ °C}$			1 100	μA μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 100\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 5\text{ A}$		0.47	0.52	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	1950 250 59	-	pF pF pF
$C_{o(tr)}$	Equivalent capacitance time related	$V_{GS} = 0$, $V_{DS} = 0\text{ to }400\text{ V}$	-	78	-	pF
$C_{o(er)}$	Equivalent capacitance energy related		-	58	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	1.9	-	Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 400\text{ V}$, $I_D = 10\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 13)	-	40 7 22	-	nC nC nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 250 \text{ V}$, $I_D = 5.5 \text{ A}$, $R_G = 4.7 \Omega$, $V_{GS} = 10 \text{ V}$ (see Figure 12)		16		ns	
t_r	Rise time			21		ns	
$t_{d(off)}$	Turn-off-delay time				21		ns
t_f	Fall time				15		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		11	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				44	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 11 \text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 11 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 35 \text{ V}$ (see Figure 17)	-	85		ns
Q_{rr}	Reverse recovery charge			280		nC
I_{RRM}	Reverse recovery current			7		A
t_{rr}	Reverse recovery time	$I_{SD} = 11 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 35 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$ (see Figure 17)	-	120		ns
Q_{rr}	Reverse recovery charge			490		nC
I_{RRM}	Reverse recovery current			8		A

1. Pulse width limited by safe operating area.

2. Pulsed: Pulse duration = 300 μs , duty cycle 1.5%.

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-source breakdown voltage	$I_{gs} = \pm 1 \text{ mA}$ (open drain)	30		-	V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

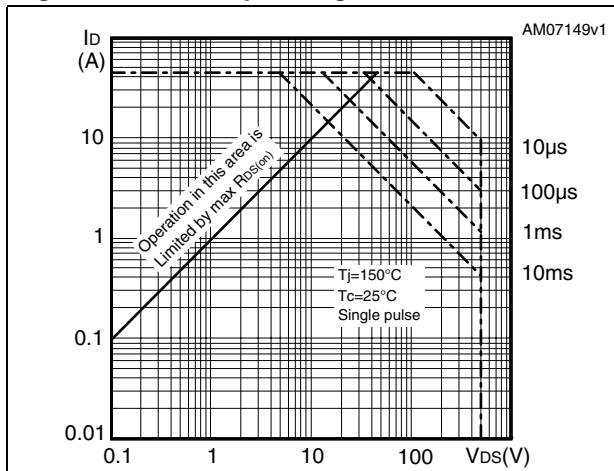


Figure 3. Thermal impedance

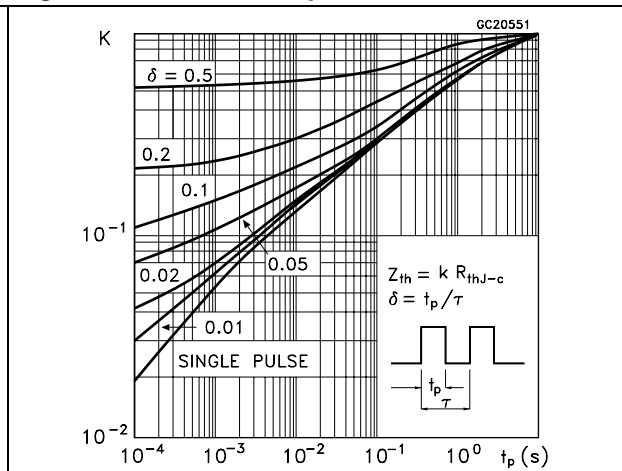


Figure 4. Output characteristics

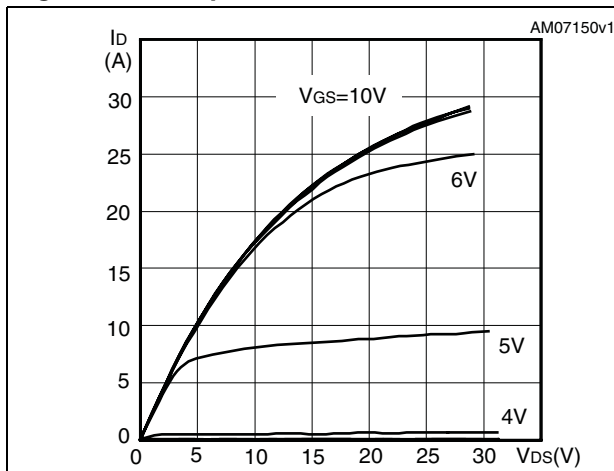


Figure 5. Transfer characteristics

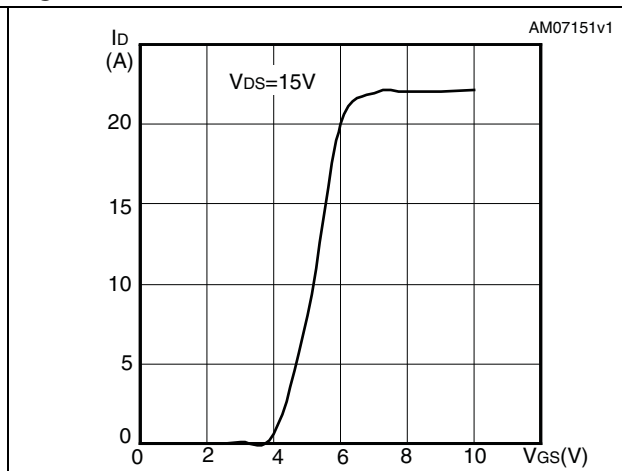


Figure 6. Normalized $B_{V_{DS}}$ vs temperature

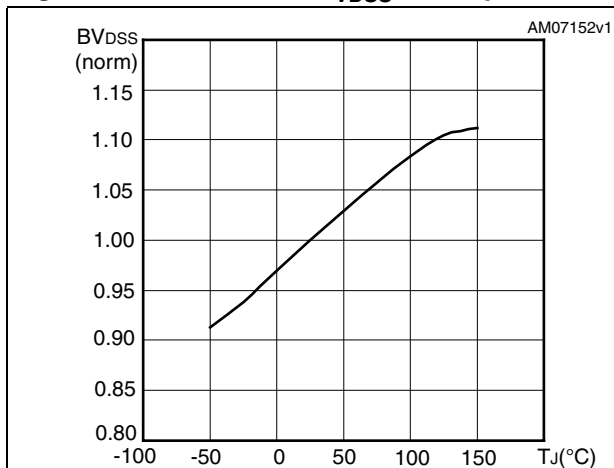


Figure 7. Static drain-source on resistance

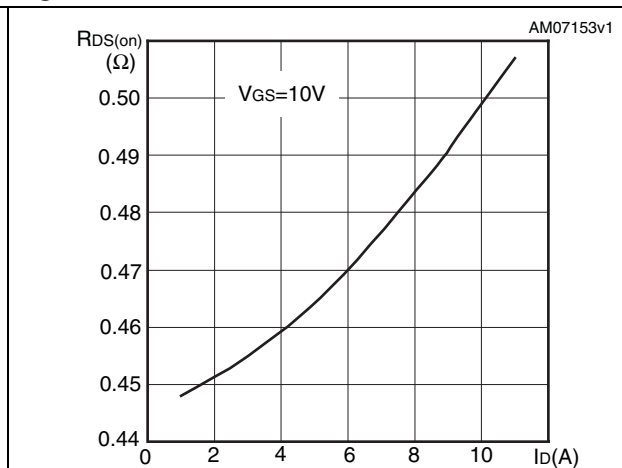


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

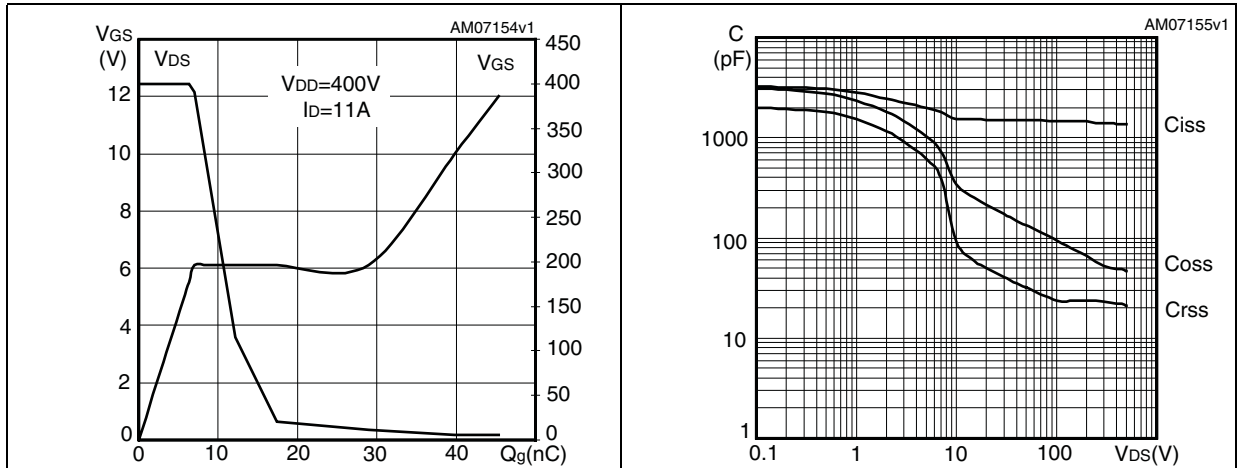
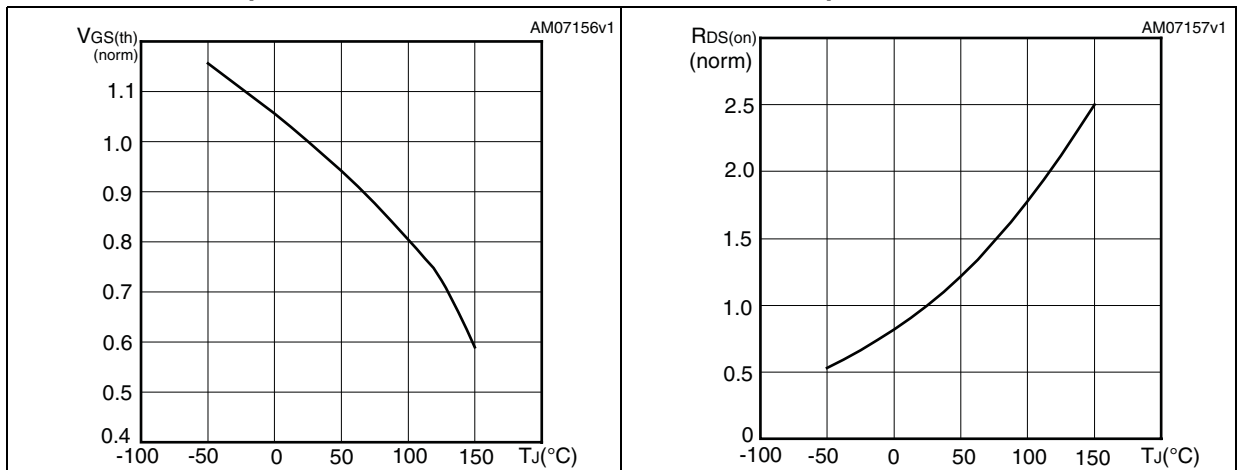


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature



3 Test circuits

Figure 12. Switching times test circuit for resistive load

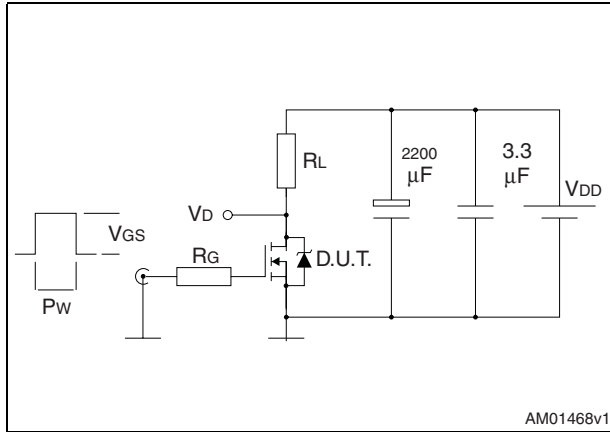


Figure 13. Gate charge test circuit

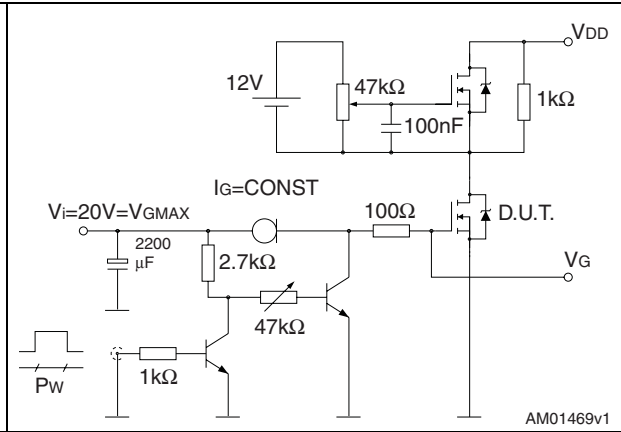


Figure 14. Test circuit for inductive load switching and diode recovery times

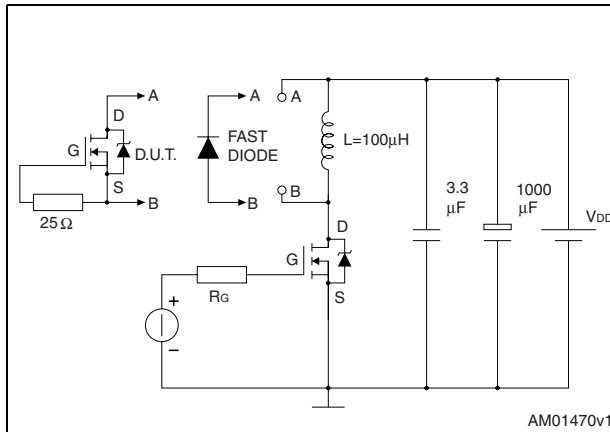


Figure 15. Unclamped inductive load test circuit

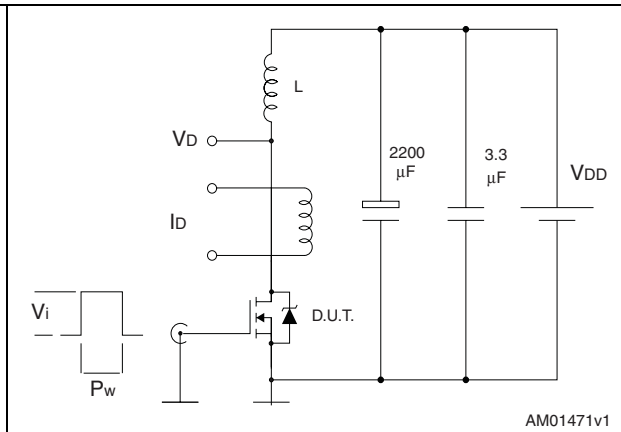


Figure 16. Unclamped inductive waveform

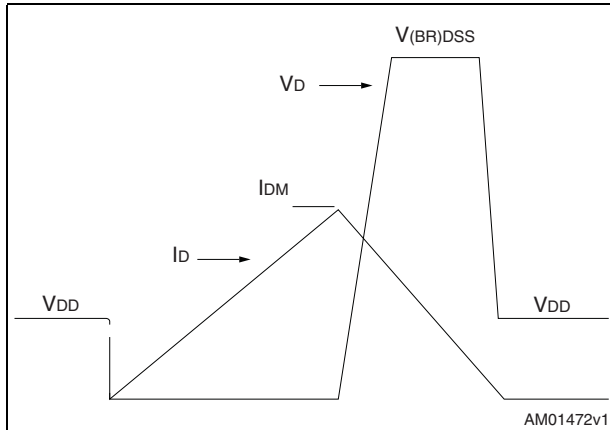
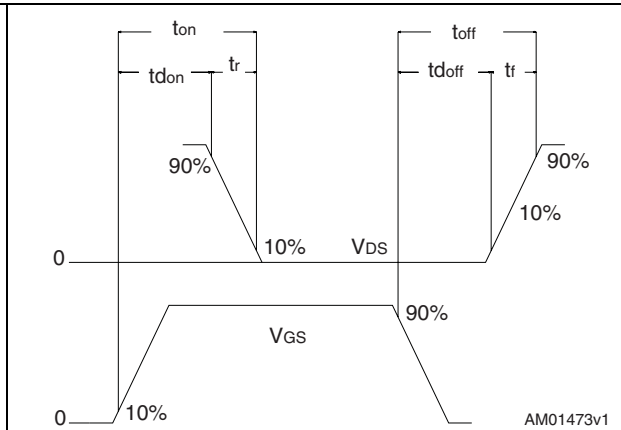


Figure 17. Switching time waveform



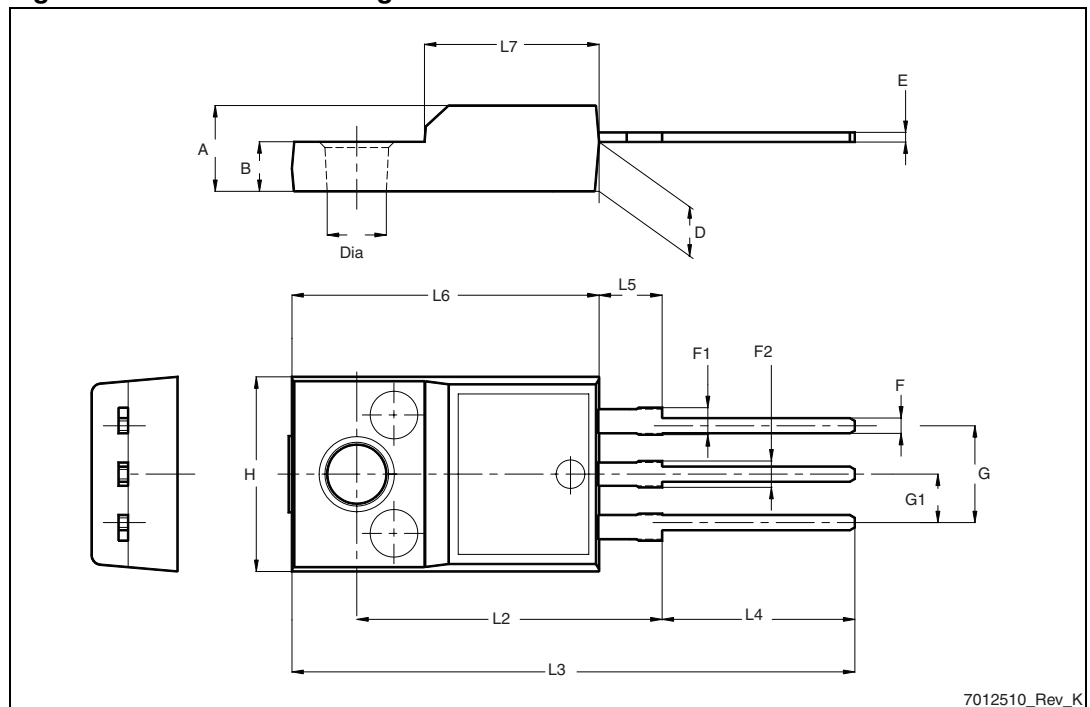
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 18. TO-220FP drawing



7012510_Rev_K

5 Revision history

Table 10. Document revision history

Date	Revision	Changes
09-Sep-2010	1	First release.

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