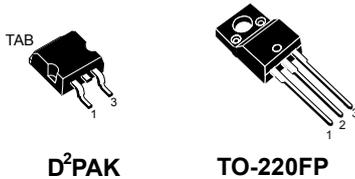
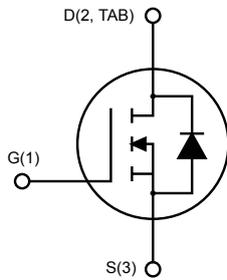


N-channel 550 V, 0.150 Ω typ., 16 A MDmesh™ M5 Power MOSFETs in a D²PAK and TO-220FP packages


D²PAK
TO-220FP


AM01475v1_noZen

Features

Order code	V _{DS} @ T _{jmax.}	R _{DS(on)} max.	Package
STB18N55M5	600 V	0.192 Ω	D ² PAK
STF18N55M5			TO-220FP

- Extremely low R_{DS(on)}
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs based on the MDmesh™ M5 innovative vertical process technology combined with the well-known PowerMESH™ horizontal layout. The resulting products offer extremely low on-resistance, making them particularly suitable for applications requiring high power and superior efficiency.

Product status link

[STB18N55M5](#)
[STF18N55M5](#)

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		D ² PAK	TO-220FP	
V _{GS}	Gate-source voltage	±25		V
I _D	Drain current (continuous) at T _C = 25 °C	16		A
I _D	Drain current (continuous) at T _C = 100 °C	10		A
I _{DM} ⁽¹⁾	Drain current (pulsed)	64		A
P _{TOT}	Total dissipation at T _C = 25 °C	110	25	W
dv/dt ⁽²⁾	Peak diode recovery voltage slope	15		V/ns
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; T _C = 25 °C)	2.5		kV
T _j	Operating junction temperature range	-55 to 150		°C
T _{stg}	Storage temperature range			

1. Pulse width limited by safe operating area.
2. I_{SD} ≤ 16 A, di/dt ≤ 400 A/μs; V_{DS peak} < V_{(BR)DSS}; V_{DD} = 340 V.

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		D ² PAK	TO-220FP	
R _{thj-case}	Thermal resistance junction-case	1.14	5	°C/W
R _{thj-amb}	Thermal resistance junction-ambient		62.5	°C/W
R _{thj-pcb} ⁽¹⁾	Thermal resistance junction-pcb	30		°C/W

1. When mounted on an 1-inch² FR-4, 2oz Cu board.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T _j Max)	4	A
E _{AS}	Single pulse avalanche energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	210	mJ

2 Electrical characteristics

($T_{CASE} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	$I_D = 1\text{ mA}, V_{GS} = 0\text{ V}$	550			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}, V_{DS} = 550\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}, V_{DS} = 550\text{ V}, T_C = 125\text{ }^{\circ}\text{C}^{(1)}$			100	μA
I_{GSS}	Gate body leakage current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}, I_D = 8\text{ A}$		0.150	0.192	Ω

1. Defined by design, not subject to production test.

Table 5. Dynamic

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}, f = 1\text{ MHz}, V_{GS} = 0\text{ V}$	-	1260	-	pF
C_{oss}	Output capacitance			42		
C_{rss}	Reverse transfer capacitance			3.6		
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ to }440\text{ V}, V_{GS} = 0\text{ V}$	-	103	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related			35		
R_g	Gate input resistance	$f = 1\text{ MHz}$ open drain	-	2.8	-	Ω
Q_g	Total gate charge	$V_{DD} = 440\text{ V}, I_D = 8\text{ A}, V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 18. Test circuit for gate charge behavior)	-	31	-	nC
Q_{gs}	Gate-source charge			8.3		
Q_{gd}	Gate-drain charge			14.2		

1. Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

2. Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	$V_{DD} = 400\text{ V}$, $I_D = 10.5\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 19. Test circuit for inductive load switching and diode recovery times and Figure 22. Switching time waveform)	-	37	-	ns
$t_{r(v)}$	Voltage rise time			7		
$t_{c(off)}$	Crossing time			10.3		
$t_{f(i)}$	Current fall time			8.3		

Table 7. Source drain diode

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	
I_{SD}	Source-drain current		-		16	A	
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				64		
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 16\text{ A}$, $V_{GS} = 0\text{ V}$	-		1.5	V	
t_{rr}	Reverse recovery time	$I_{SD} = 16\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$ (see Figure 19. Test circuit for inductive load switching and diode recovery times)	-	244		ns	
Q_{rr}	Reverse recovery charge			2.8			A
I_{RRM}	Reverse recovery current			23			
t_{rr}	Reverse recovery time	$I_{SD} = 16\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 100\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 19. Test circuit for inductive load switching and diode recovery times)	-	295		ns	
Q_{rr}	Reverse recovery charge			3.7			A
I_{RRM}	Reverse recovery current			25			

1. Pulse width limited by safe operating area.

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics curves

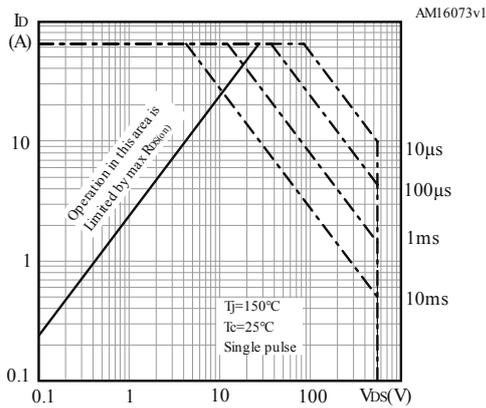
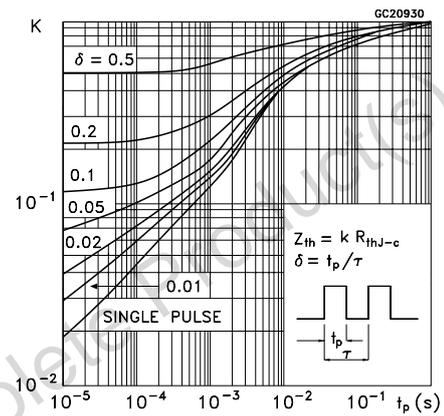
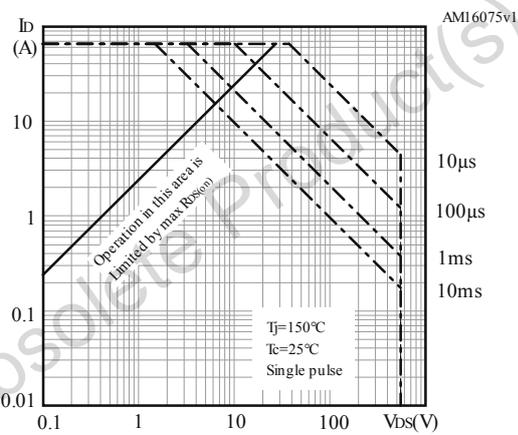
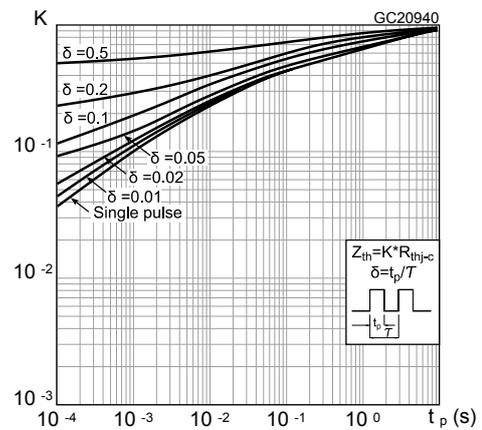
Figure 1. Safe operating area for D²PAK

Figure 2. Thermal impedance for D²PAK

Figure 4. Safe operating area for TO-220FP

Figure 5. Thermal impedance for TO-220FP


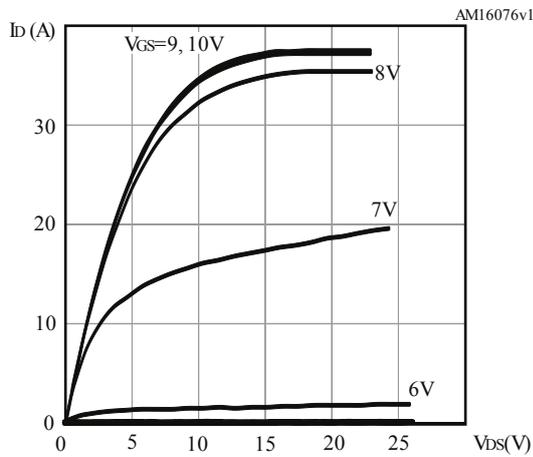
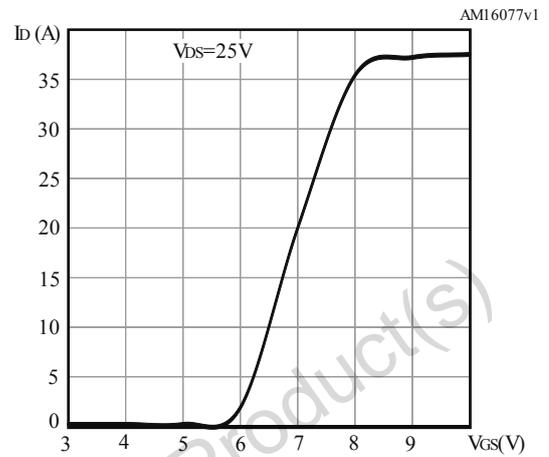
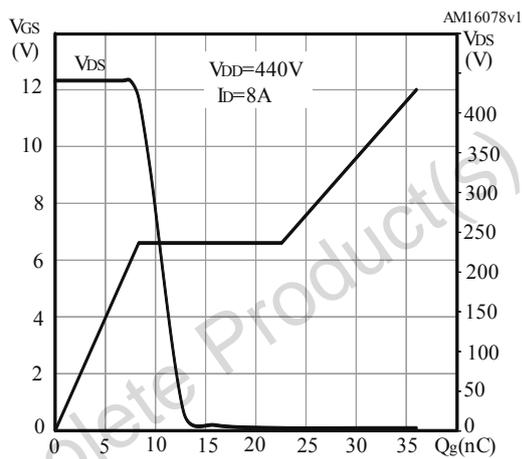
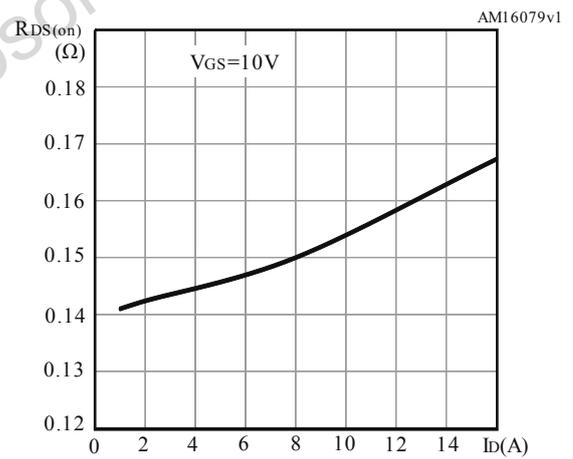
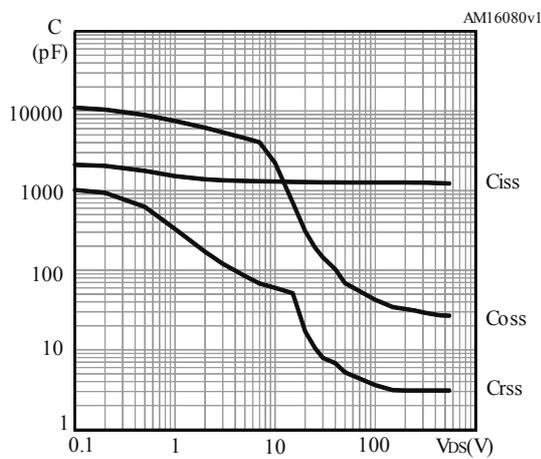
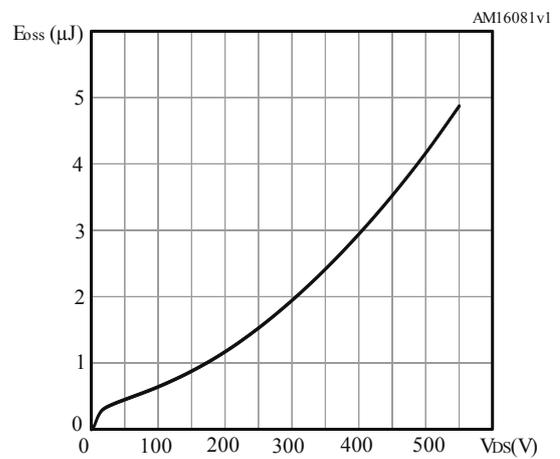
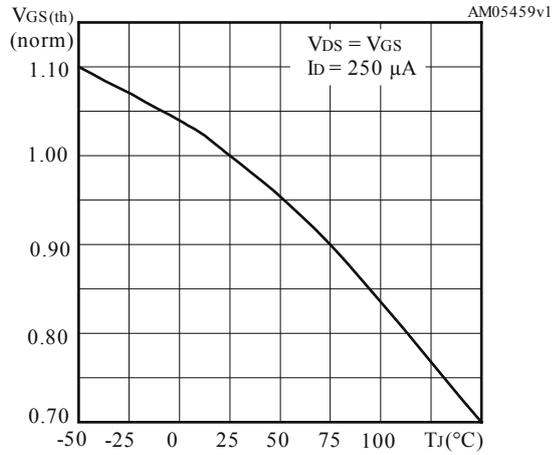
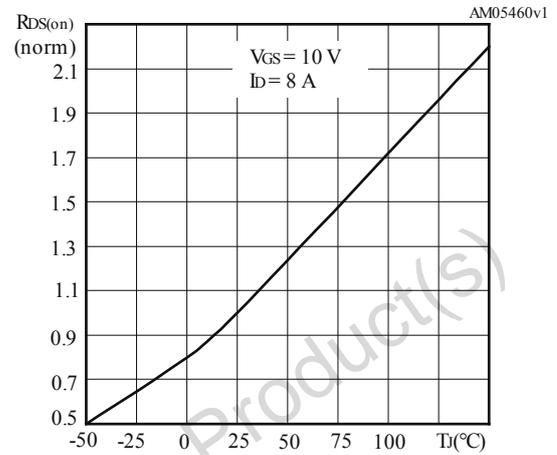
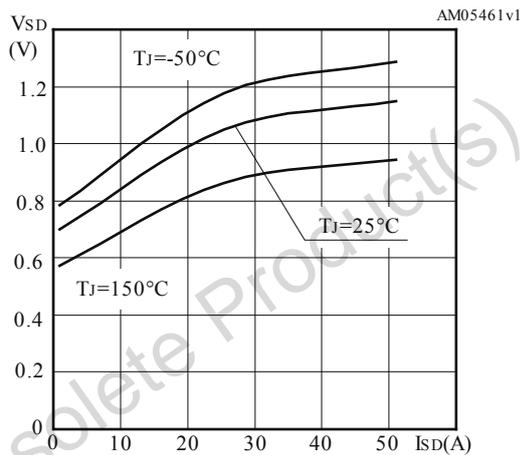
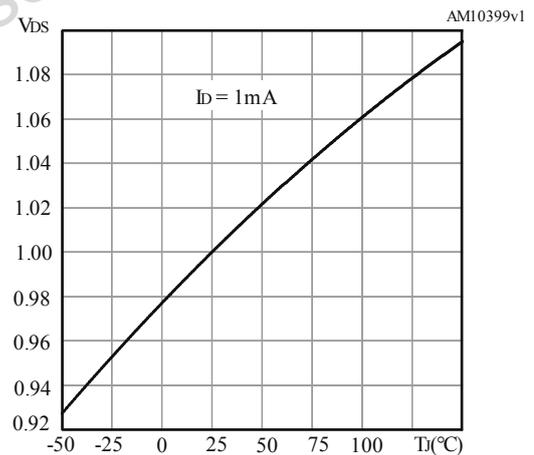
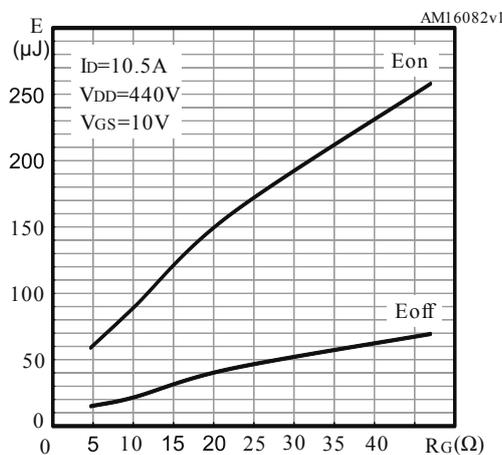
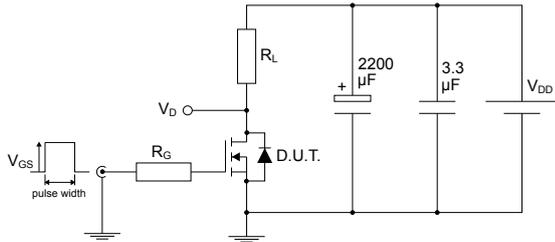
Figure 6. Output characteristics

Figure 7. Transfer characteristics

Figure 8. Gate charge vs gate-source voltage

Figure 9. Static drain-source on resistance

Figure 10. Capacitance variations

Figure 11. Output capacitance stored energy


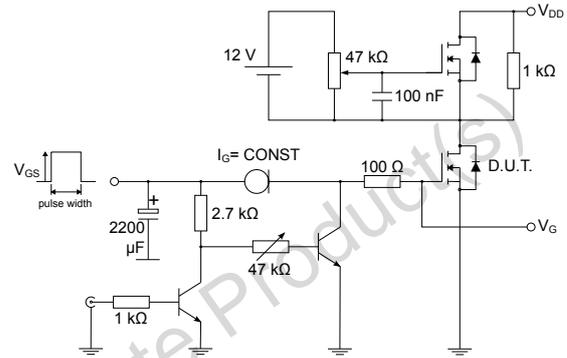
Figure 12. Normalized on-resistance vs temperature

Figure 13. Normalized gate threshold voltage vs temperature

Figure 14. Drain-source diode forward characteristics

Figure 15. Normalized $V_{(BR)DSS}$ vs temperature

Figure 16. Switching energy vs gate resistance


* E_{on} including reverse recovery of a SiC diode

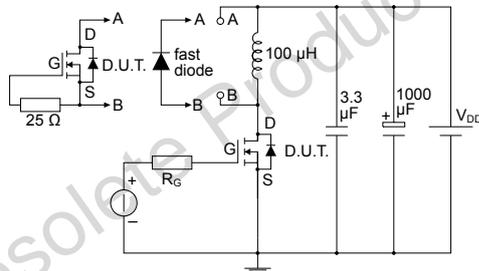
3 Test circuits

Figure 17. Test circuit for resistive load switching times


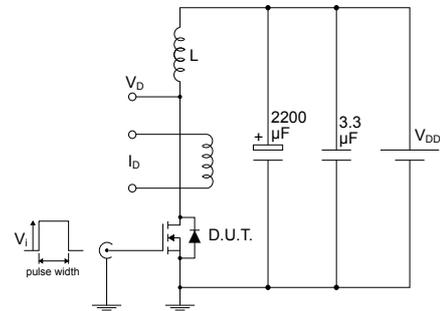
AM01488v1

Figure 18. Test circuit for gate charge behavior


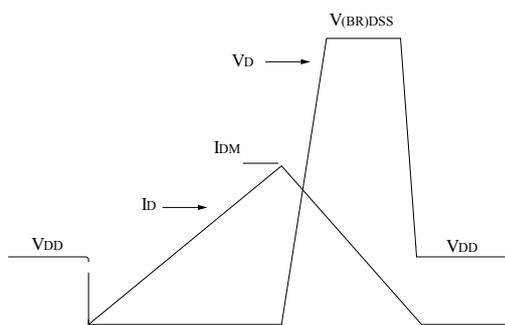
AM01469v1

Figure 19. Test circuit for inductive load switching and diode recovery times


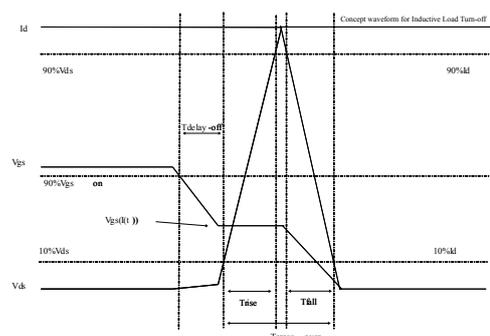
AM01470v1

Figure 20. Unclamped inductive load test circuit


AM01471v1

Figure 21. Unclamped inductive waveform


AM01472v1

Figure 22. Switching time waveform


AM05540v2

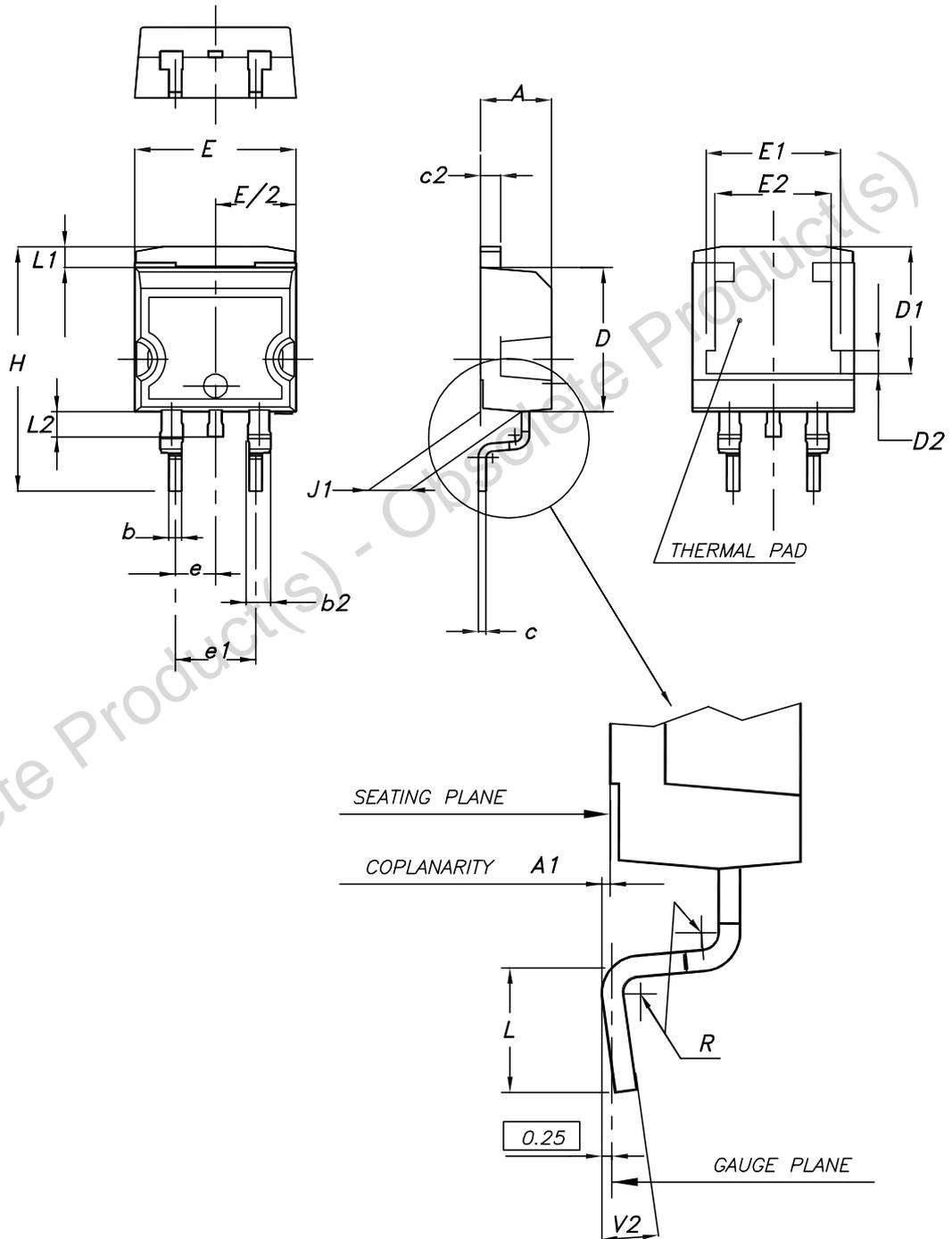
4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Obsolete Product(s) - Obsolete Product(s)

4.1 D²PAK (TO-263) type A package information

Figure 23. D²PAK (TO-263) type A package outline

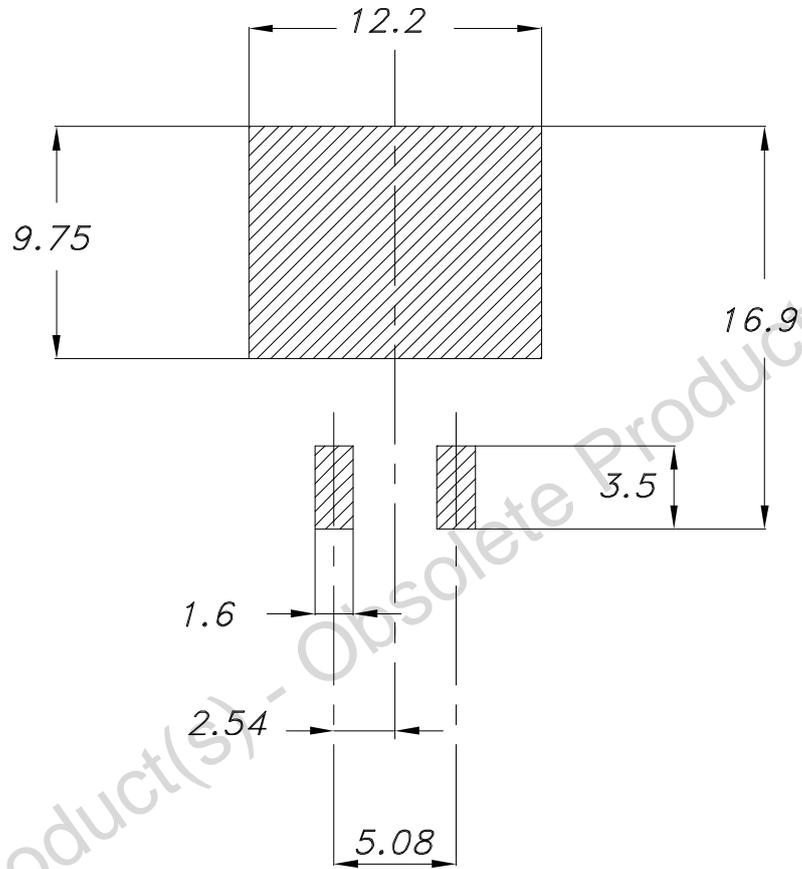


0079457_25

Table 8. D²PAK (TO-263) type A package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10.00		10.40
E1	8.30	8.50	8.70
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15.00		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.40	
V2	0°		8°

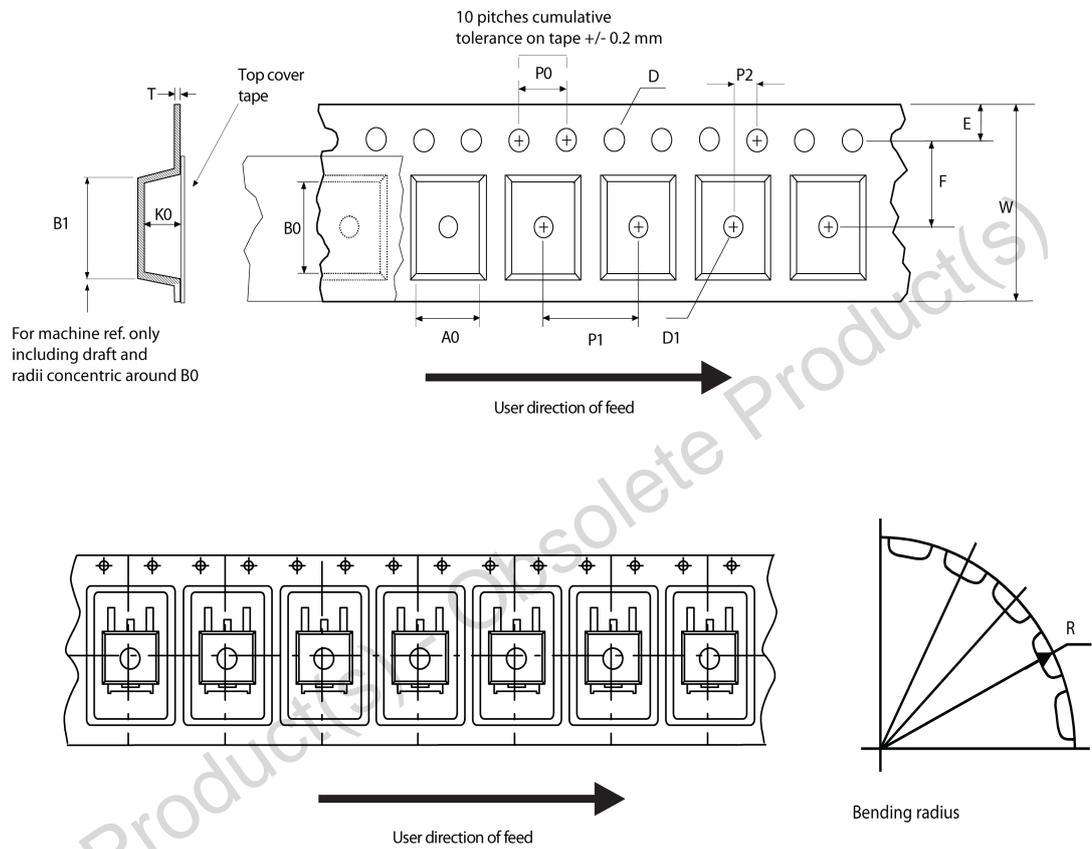
Figure 24. D²PAK (TO-263) recommended footprint (dimensions are in mm)



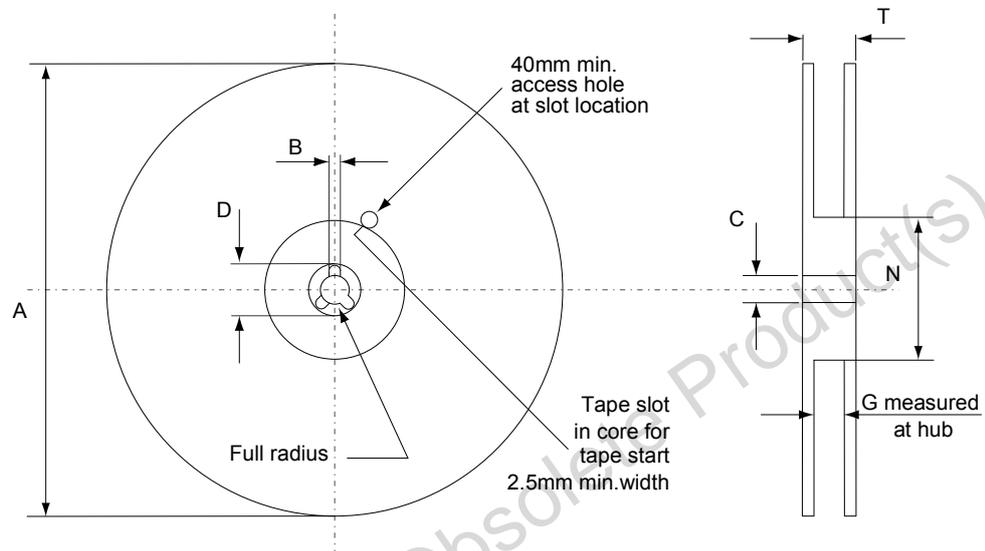
Footprint

4.2 D²PAK packing information

Figure 25. D²PAK tape outline



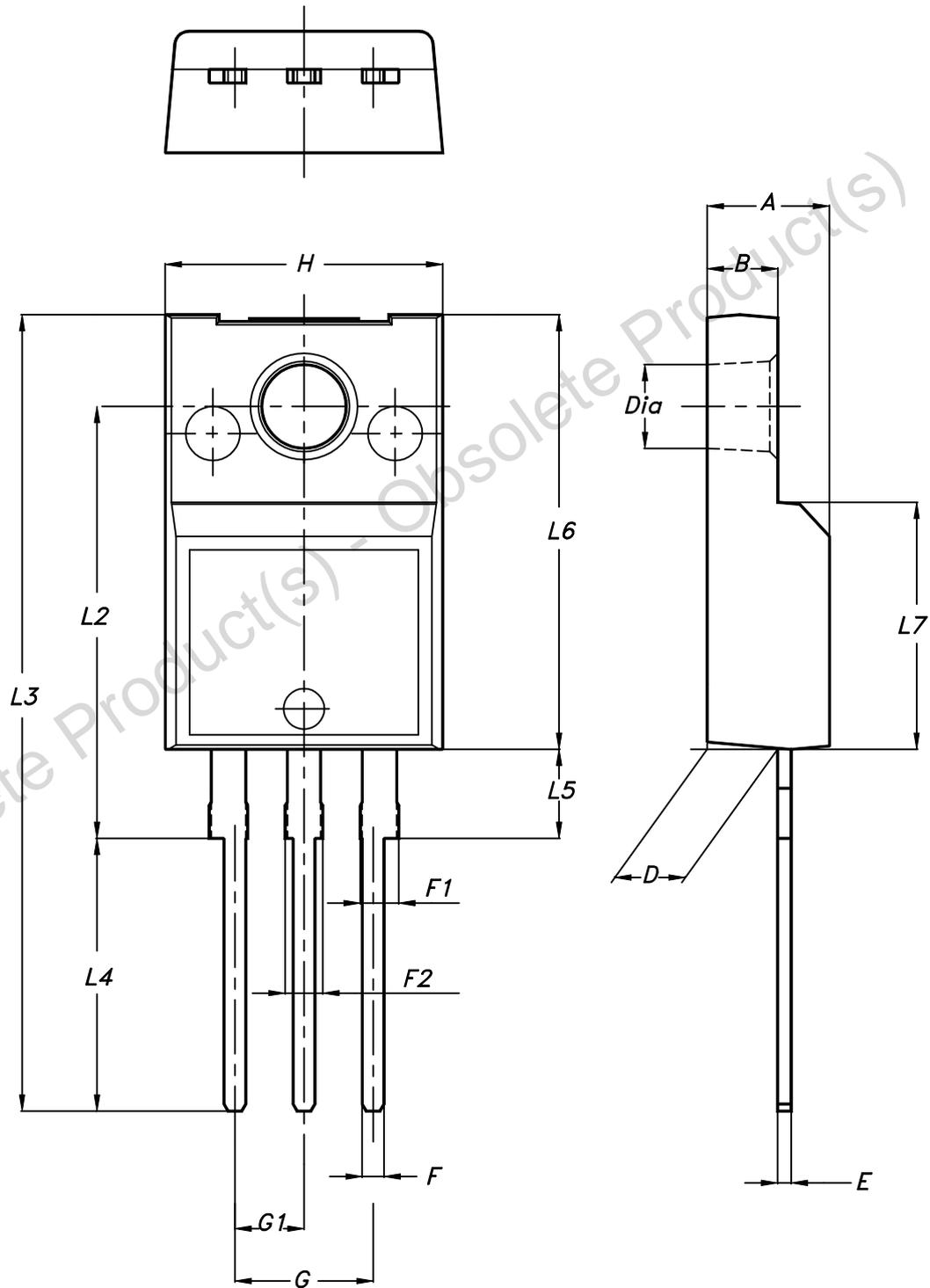
AM08852v1

Figure 26. D²PAK reel outline


AM06038v1

Table 9. D²PAK tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1	Base quantity		1000
P2	1.9	2.1	Bulk quantity		1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

4.3 TO-220FP package information
Figure 27. TO-220FP package outline


7012510_Rev_12_B

Table 10. TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

5 Ordering information

Table 11. Order codes

Order code	Marking	Package	Packing
STB18N55M5	18N55M5	D ² PAK	Tape and reel
STF18N55M5		TO-220FP	Tube

Obsolete Product(s) - Obsolete Product(s)

Revision history

Table 12. Document revision history

Date	Version	Changes
27-Aug-2018	1	First release. Part numbers previously included in datasheet DocID17078.

Obsolete Product(s) - Obsolete Product(s)

Contents

1	Electrical ratings	2
2	Electrical characteristics	3
2.1	Electrical characteristics curves	5
3	Test circuits	8
4	Package information	9
4.1	D²PAK (TO-263) type A package information	9
4.2	D²PAK packing information	12
4.3	TO-220FP package information	14
5	Ordering information	17
	Revision history	18

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2018 STMicroelectronics – All rights reserved