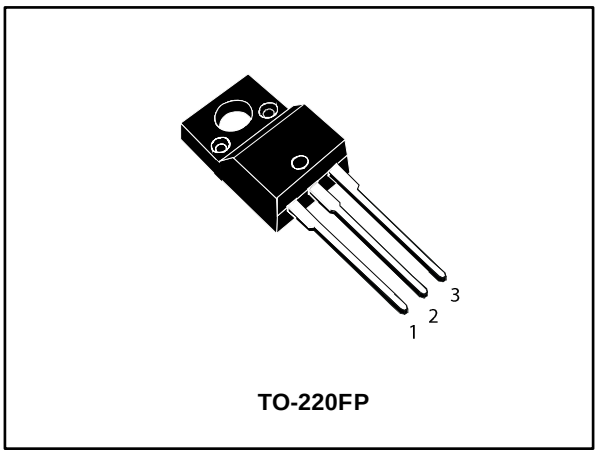
STF21P6LLF6

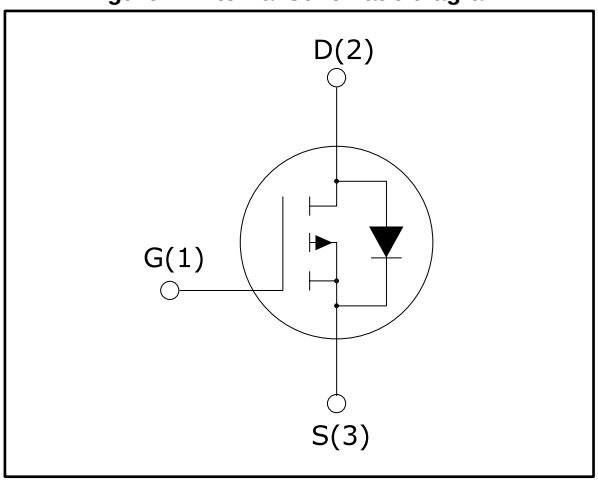
P-channel -60 V, 25.5 mΩ typ., -21 A STripFET™ F6 Power MOSFET in a TO-220FP package

Datasheet - production data



TO-220FP

Figure 1: Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D	P_{TOT}
STF21P6LLF6	-60 V	28.5 mΩ	-21 A	25 W

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is a P-channel Power MOSFET developed using the STripFET™ F6 technology, with a new trench gate structure. The resulting Power MOSFET exhibits very low $R_{DS(on)}$ in all packages.

Table 1: Device summary

Order code	Marking	Package	Packing
STF21P6LLF6	21P6LLF6	TO-220FP	Tape and reel

Contents

1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	-60	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) at T_C = 25 °C	-21	A
I_D	Drain current (continuous) at T_C = 100 °C	-15	A
I_{DM}(1)	Drain current (pulsed)	-84	A
P_{TOT}	Total dissipation at T_C = 25 °C	25	W
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s; TC = 25 °C)	2.5	kV
T_{stg}	Storage temperature range	-55 to 175	°C
T_j	Operating junction temperature range		

Notes:

(1)Pulse width limited by safe operating area.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	6	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	62.5	°C/W

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = -250 µA	-60			V
I_{DSS}	Zero gate voltage Drain current	V_{GS} = 0 V, V_{DS} = -60 V			-1	µA
		V_{GS} = 0 V, V_{DS} = -60 V, T_C = 125 °C(1)			-10	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = ± 20 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = -250 µA	-1		-2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = -10 V, I_D = -10.5 A		25.5	28.5	mΩ
		V_{GS} = -4.5 V, I_D= -10.5 A		30.5	36.5	

Notes:

(1)Defined by design, not subject to production test.

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = -25 V, f = 1 MHz, V_{GS} = 0 V	-	3780	-	pF
C_{oss}	Output capacitance		-	262	-	pF
C_{rss}	Reverse transfer capacitance		-	170	-	pF
Q_g	Total gate charge	V_{DD} = -30 V, I_D = -21 A, V_{GS} = -4.5 V (see *Figure 14: "Gate charge test circuit"*)	-	30	-	nC
Q_{gs}	Gate-source charge		-	10.8	-	nC
Q_{gd}	Gate-drain charge		-	10.5	-	nC
R_G	Gate input resistance	I_D = 0 A, gate DC bias = 0 V, f = 1 MHz, magnitude of alternative signal = 20 mV	-	1.7	-	Ω

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = -30 V, I_D = -10 A, R_G = 4.7 Ω, V_{GS} = -10 V (see *Figure 13: "Switching times test circuit for resistive load"*)	-	51.4	-	ns
t_r	Rise time		-	39	-	ns
$t_{d(off)}$	Turn-off-delay time		-	171	-	ns
t_f	Fall time		-	21	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD} (1)	Forward on voltage	V_{GS} = 0 V, I_{SD} = -21 A	-		-1.1	V
t_{rr}	Reverse recovery time	I_{SD} = -35 A, di/dt = 100 A/µs, V_{DD} = -48 V, (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*)	-	34		ns
Q_{rr}	Reverse recovery charge		-	48		nC
I_{RRM}	Reverse recovery current		-	-2.8		A

Notes:

(1)Pulse test: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

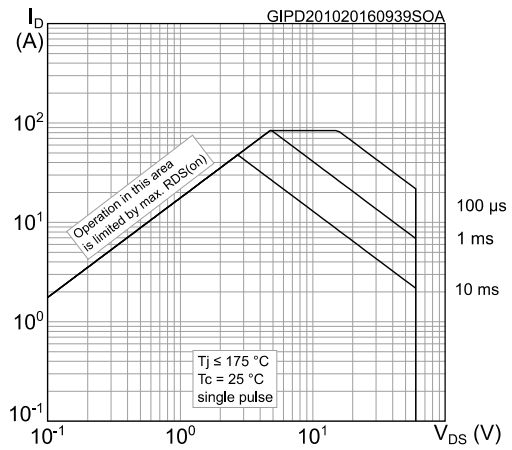


Figure 3: Thermal impedance

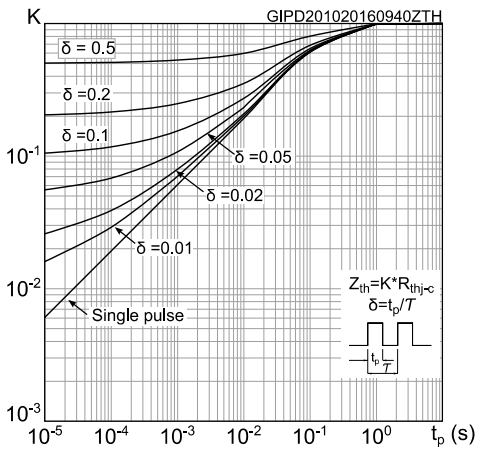


Figure 4: Output characteristics

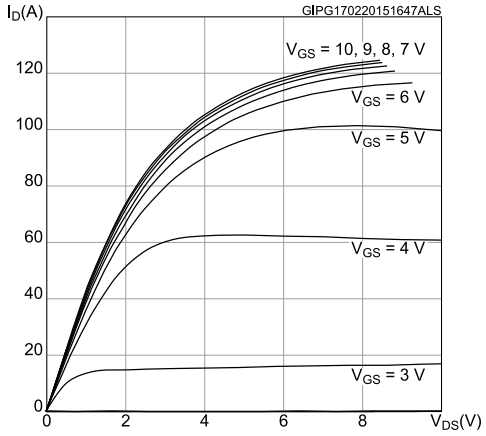


Figure 5: Transfer characteristics

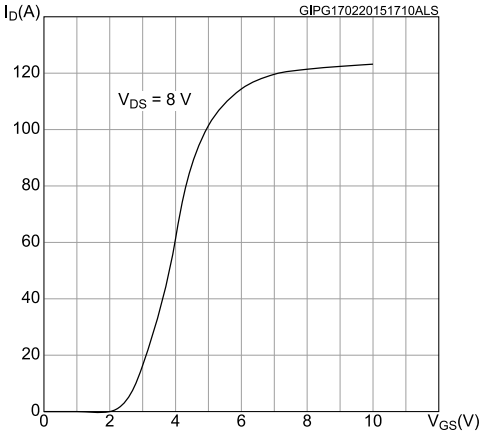


Figure 6: Normalized gate threshold voltage vs temperature

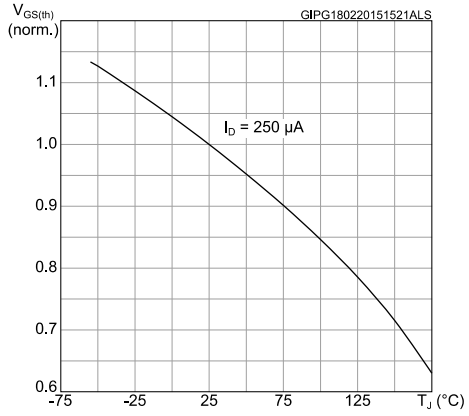


Figure 7: Normalized $V_{(BR)DSS}$ vs temperature

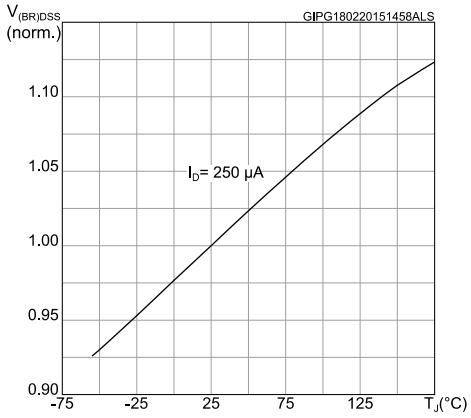


Figure 8: Static drain-source on-resistance

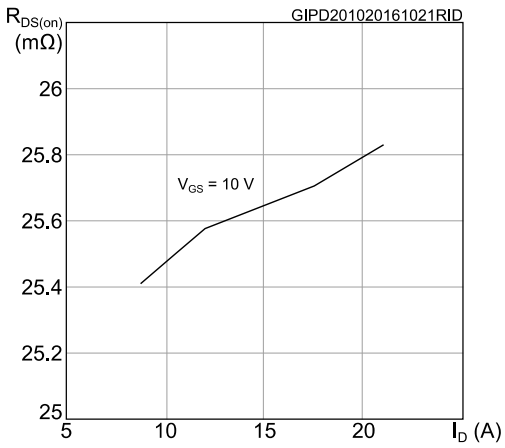


Figure 9: Normalized on-resistance vs. temperature

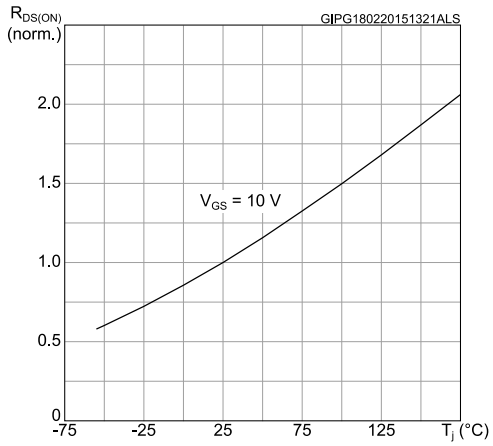


Figure 10: Gate charge vs gate-source voltage

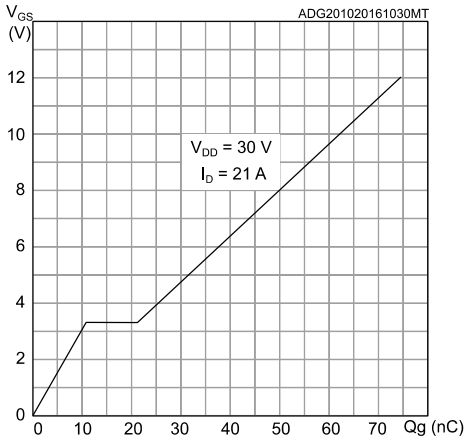


Figure 11: Capacitance variations voltage

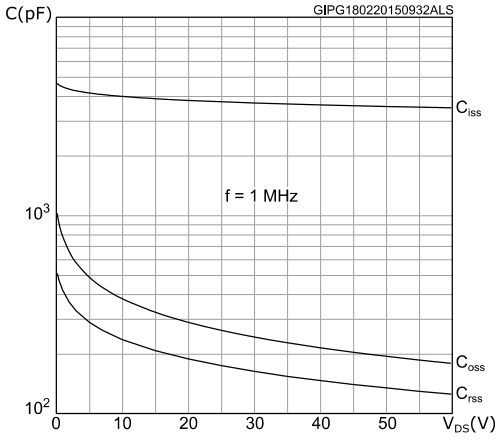
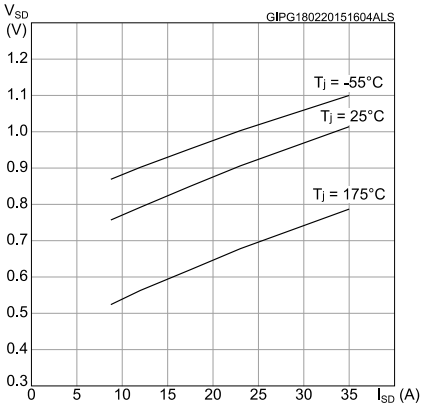


Figure 12: Source-drain diode forward characteristics



For the P-channel Power MOSFET, current polarity of voltages and current have to be reversed.

3 Test circuits

Figure 13: Switching times test circuit for resistive load

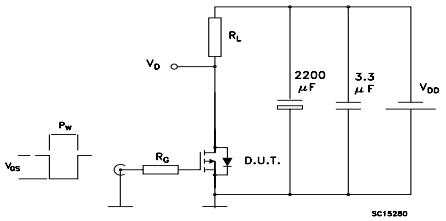


Figure 14: Gate charge test circuit

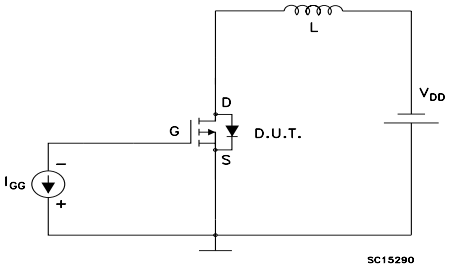
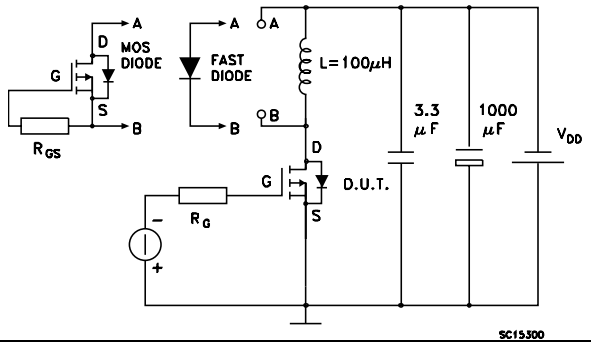


Figure 15: Test circuit for inductive load switching and diode recovery times



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 TO-220FP package information

Figure 16: TO-220FP package outline

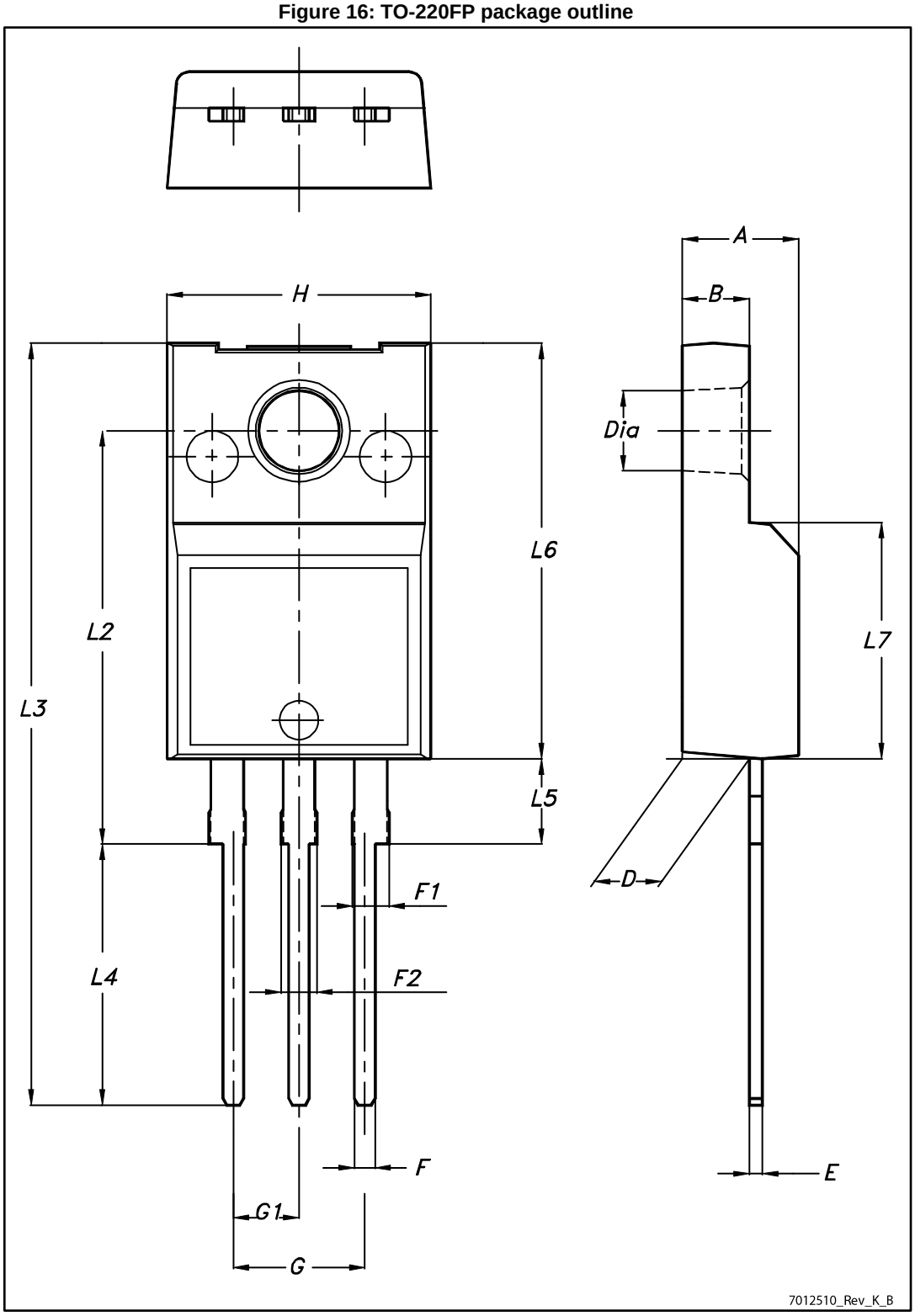


Table 8: TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
11-Nov-2016	1	First release.

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