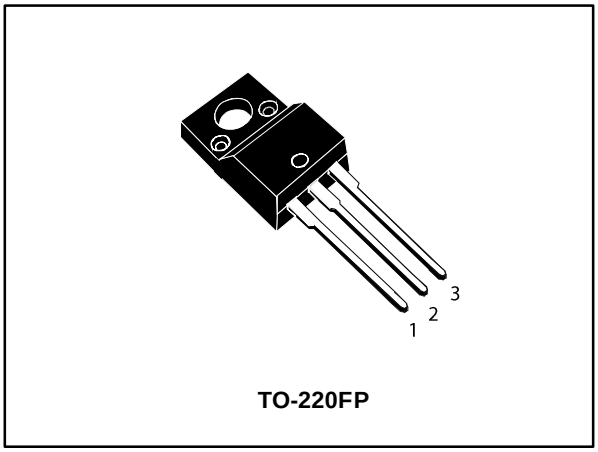
STF30N10F7

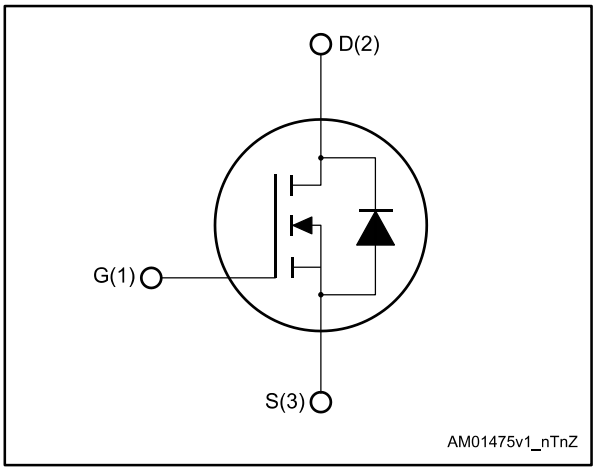
N-channel 100 V, 0.02 Ω typ., 24 A STripFET™ F7 Power MOSFET in a TO-220FP package

Datasheet - production data



TO-220FP

Figure 1: Internal schematic diagram



Features

- Among the lowest $R_{DS(on)}$ on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1: Device summary

Order code	Marking	Package	Packing
STF30N10F7	30N10F7	TO-220FP	Tube

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate source voltage	20	V
I_D(1)	Drain current (continuous) at T_C = 25 °C	24	A
I_D(1)	Drain current (continuous) at T_C = 100 °C	16	A
I_{DM}(1)(2)	Drain current (pulsed)	96	A
P_{TOT}	Total dissipation at T_C = 25 °C	25	W
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s; T_C=25 °C)	2500	V
T_J	Operating junction temperature range	-55 to 175	°C
T_{stg}	Storage temperature range		

Notes:

(1)Current is limited by package.

(2)Pulse width limited by safe operating area.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	6	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	62.5	°C/W

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4: On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D= 250 µA	100			V
I_{DSS}	Zero gate voltage drain current	V_{GS}= 0 V , V_{DS}=100 V			1	µA
		V_{GS}= 0 V, V_{DS}=100 V, T_C= 125 °C(1)			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0 V, V_{GS} = +20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 16 A		0.02	0.024	Ω

Notes:

(1)Defined by design, not subject to production test

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz,V_{GS}= 0 V	-	1270	-	pF
C_{oss}	Output capacitance		-	290	-	pF
C_{rss}	Reverse transfer capacitance		-	24	-	pF
Q_g	Total gate charge	V_{DD} = 50 V, I_D = 32 A, V_{GS} = 10 V (see *Figure 14: "Test circuit for gate charge behavior"*)	-	19	-	nC
Q_{gs}	Gate-source charge		-	9	-	nC
Q_{gd}	Gate-drain charge		-	4.5	-	nC

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 50 V, I_D = 16 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 13: "Test circuit for resistive load switching times"*)	-	12	-	ns
t_r	Rise time		-	17.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	22	-	ns
t_f	Fall time		-	5.6	-	ns

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}(1)	Forward on voltage	I_{SD} = 24 A, V_{GS} = 0	-		1.1	V
I_{rr}	Reverse recovery time	I_{SD} = 24 A, di/dt = 100 A/µs V_{DD}= 80 V, T_J= 150 °C, (see *Figure 15: "Test circuit for inductive load switching and diode recovery times"*)	-	41		ns
Q_{rr}	Reverse recovery charge		-	47		nC
I_{RRM}	Reverse recovery current		-	2.3		A

Notes:

(1)Pulsed: pulse duration = 300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2: Safe operating area

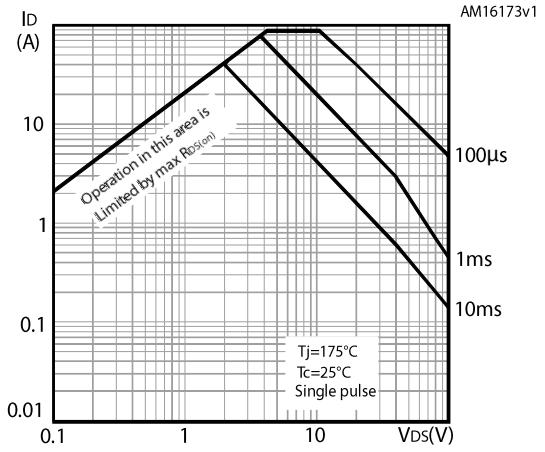


Figure 3: Thermal impedance

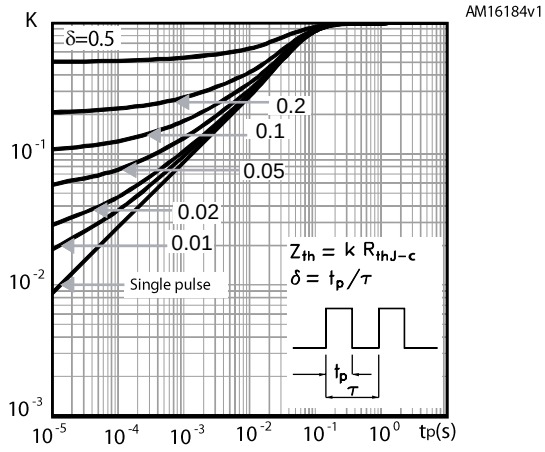


Figure 4: Output characteristics

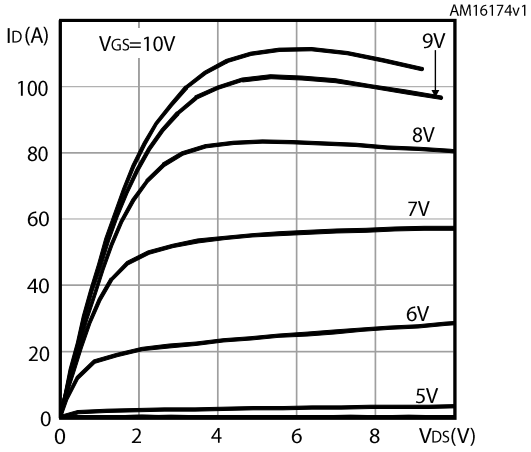


Figure 5: Transfer characteristics

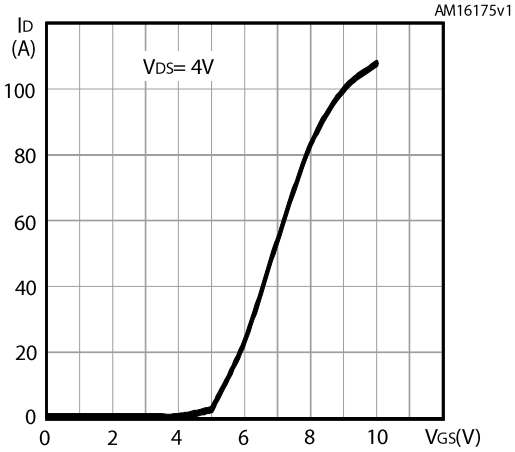


Figure 6: Gate charge vs gate-source voltage

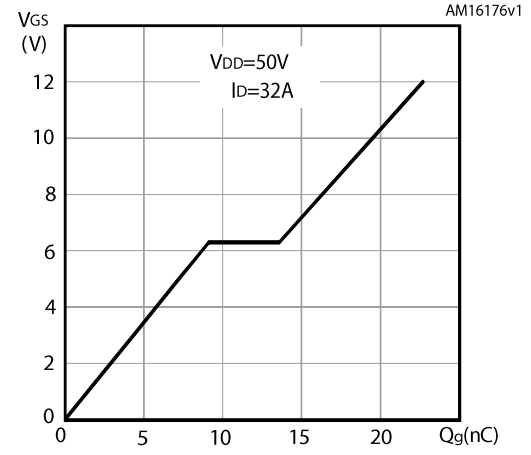


Figure 7: Static drain-source on-resistance

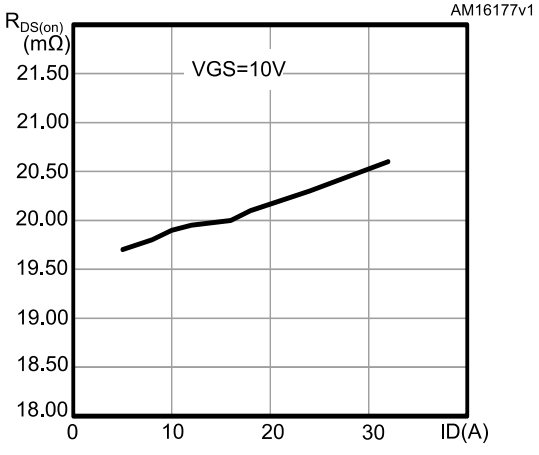


Figure 8: Capacitance variations

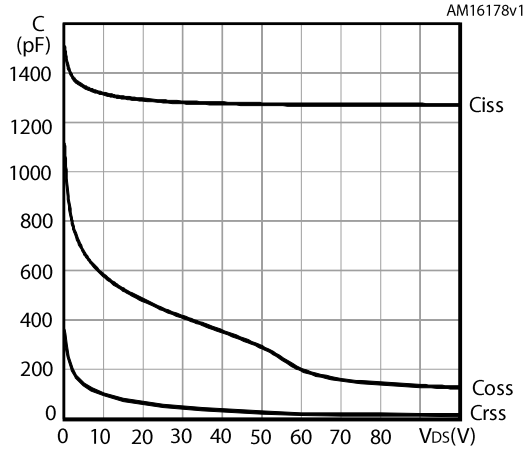


Figure 9: Normalized gate threshold voltage vs temperature

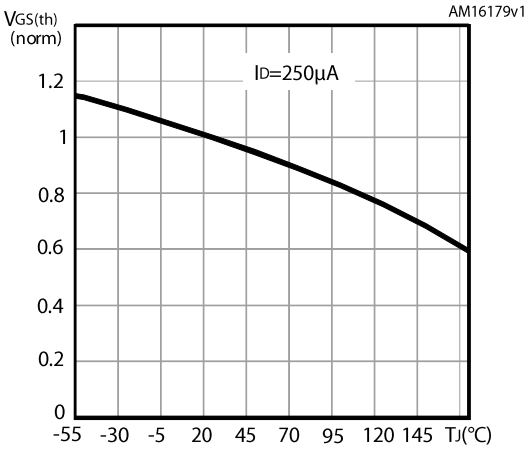


Figure 10: Normalized on-resistance vs temperature

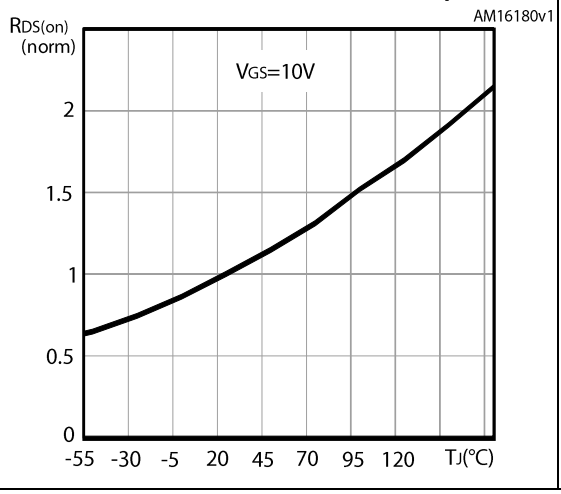


Figure 11: Normalized V(BR)DSS vs temperature

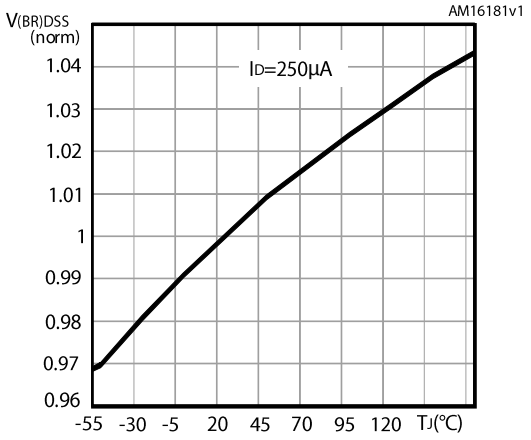
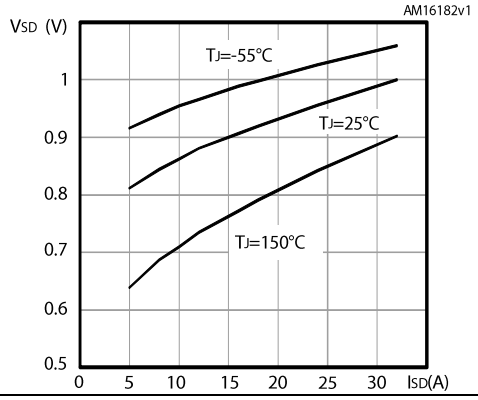


Figure 12: Source-drain diode forward characteristics



3 Test circuits

Figure 13: Test circuit for resistive load switching times

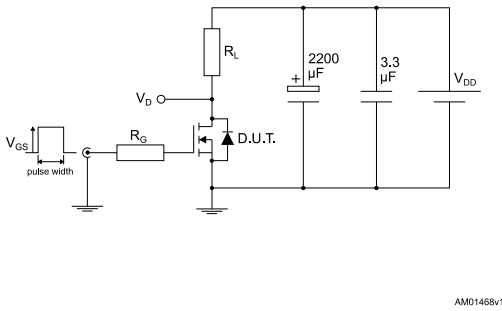


Figure 14: Test circuit for gate charge behavior

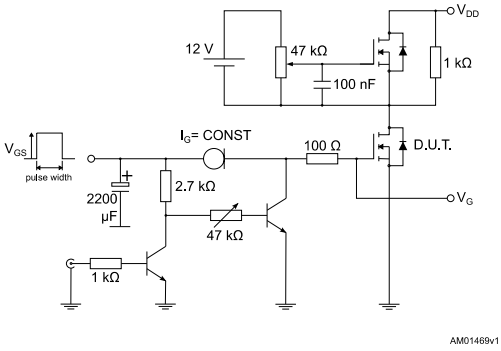


Figure 15: Test circuit for inductive load switching and diode recovery times

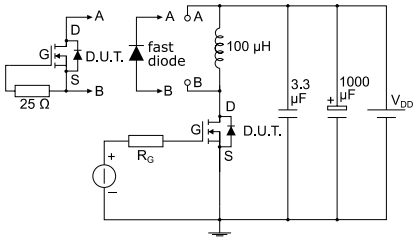


Figure 16: Unclamped inductive load test circuit

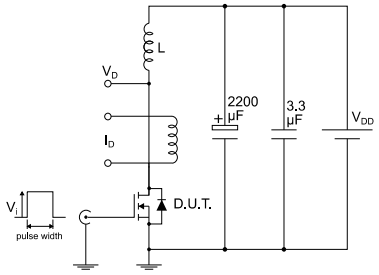


Figure 17: Unclamped inductive waveform

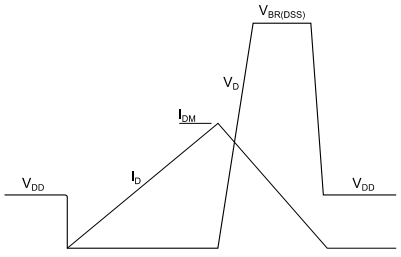
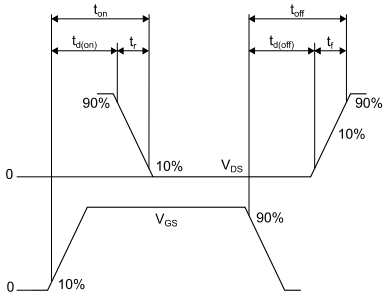


Figure 18: Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: ***www.st.com***. ECOPACK® is an ST trademark.

4.1 TO-220FP type A package information

Figure 19: TO-220FP package outline

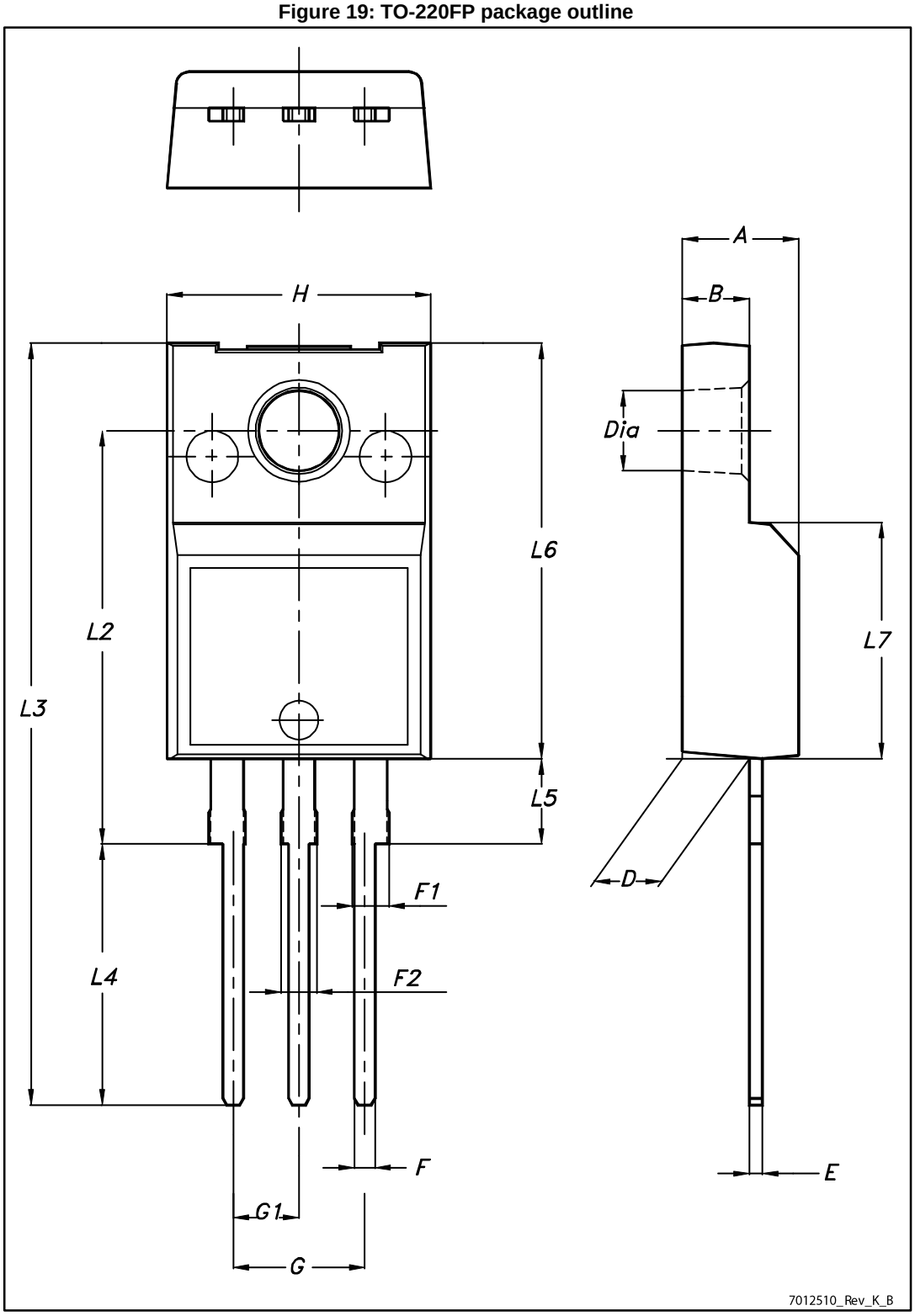


Table 8: TO-220FP package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

5 Revision history

Table 9: Document revision history

Date	Revision	Changes
15-Sep-2016	1	First release.

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