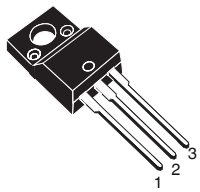
STF45N10F7

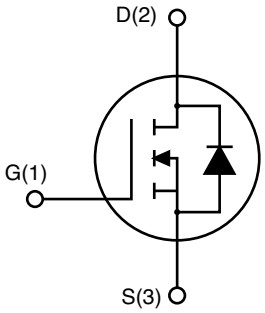
N-channel 100 V, 0.0145 Ω typ., 30 A, STripFET™ VII DeepGATE™ Power MOSFET in a TO-220FP package

Datasheet - production data



TO-220FP

Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.(1)	I_D	P_{TOT}
STF45N10F7	100 V	0.018 Ω	30 A	25 W

1. @ VGS = 10 V

- Ultra low on-resistance
- 100% avalanche tested

Applications

- Switching applications

Description

This device utilizes the 7th generation of design rules of ST's proprietary STripFET™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest $R_{DS(on)}$ in all packages.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STF45N10F7	45N10F7	TO-220FP	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	100	V
V_{GS}	Gate-source voltage	20	V
I_D	Drain current (continuous) at T_C = 25 °C	30	A
I_D	Drain current (continuous) at T_C = 100 °C	21.4	A
I_{DM}(1)	Drain current (pulsed)	120	A
P_{TOT}	Total dissipation at T_c = 25 °C	25	W
V_{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t=1 s;TC=25 °C)	2500	V
T_J	Operating junction temperature	-55 to 175	°C
T_{stg}	Storage temperature		°C

1. Pulse width limited by safe operating area.

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	6	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	62.5	°C/W

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage (V_{GS}= 0)	I_D = 1 mA	100		-	V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 100 V			10	µA
		V_{DS} = 100 V; T_C =125 °C			100	µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 15 A		0.0145	0.018	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f =1 MHz, V_{GS} = 0	-	1640	-	pF
C_{oss}	Output capacitance		-	360	-	pF
C_{rss}	Reverse transfer capacitance		-	25	-	pF
Q_g	Total gate charge	V_{DD} = 50 V, I_D = 30 A V_{GS} = 10 V *Figure 14*	-	25	-	nC
Q_{gs}	Gate-source charge		-	5.1	-	nC
Q_{gd}	Gate-drain charge		-	12.2	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 50 V, I_D = 15 A, R_G = 4.7 Ω, V_{GS} = 10 V *Figure 13*	-	15	-	ns
t_r	Rise time		-	17	-	ns
$t_{d(off)}$	Turn-off delay time		-	24	-	ns
t_f	Fall time		-	8	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		30	A
I_{SDM} (1)	Source-drain current (pulsed)		-		120	A
V_{SD} (2)	Forward on voltage	I_{SD} = 30 A, V_{GS} = 0	-		1.1	V
t_{rr}	Reverse recovery time	I_{SD} = 30 A, di/dt = 100 A/µs, V_{DD} = 80 V, T_j = 150 °C	-	53		ns
Q_{rr}	Reverse recovery charge		-	67		nC
I_{RRM}	Reverse recovery current		-	2.5		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration=300 µs, duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

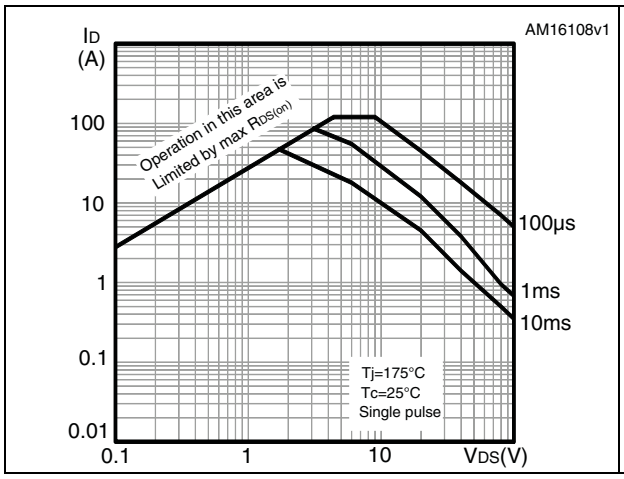


Figure 3. Thermal impedance

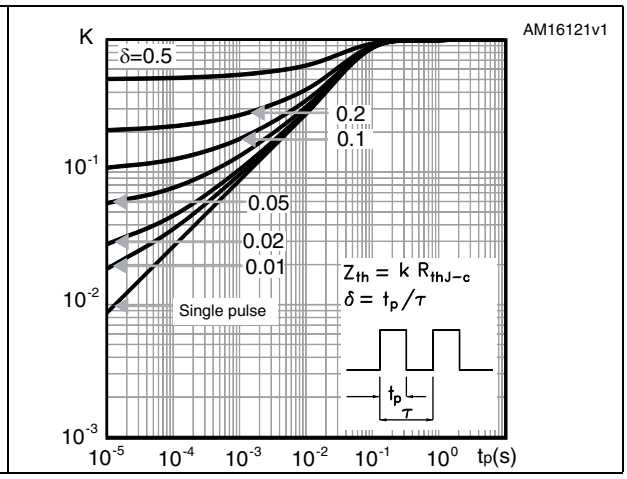


Figure 4. Output characteristics

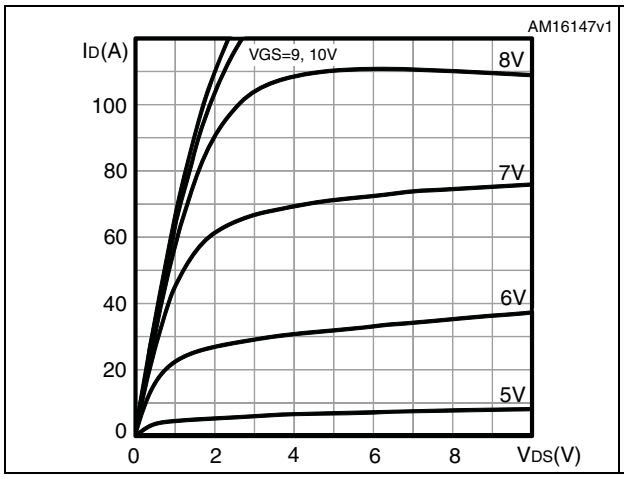


Figure 5. Transfer characteristics

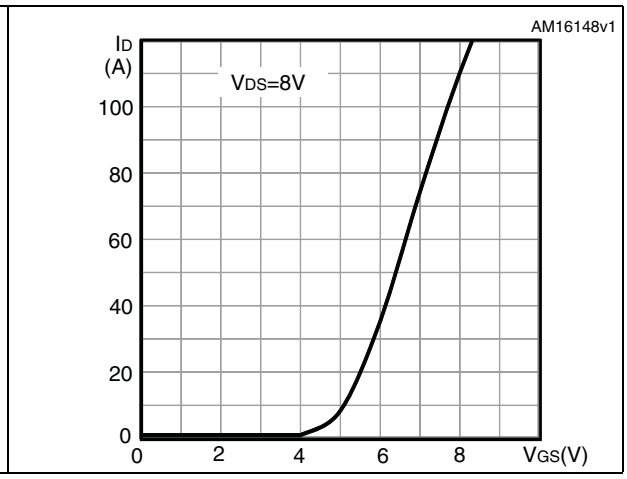


Figure 6. Gate charge vs gate-source voltage

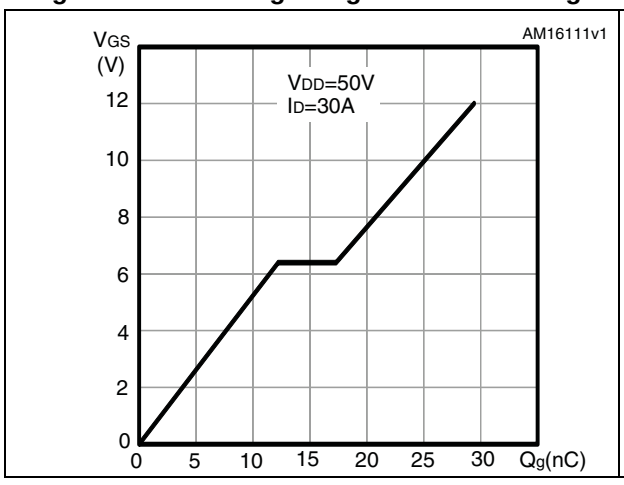


Figure 7. Static drain-source on-resistance

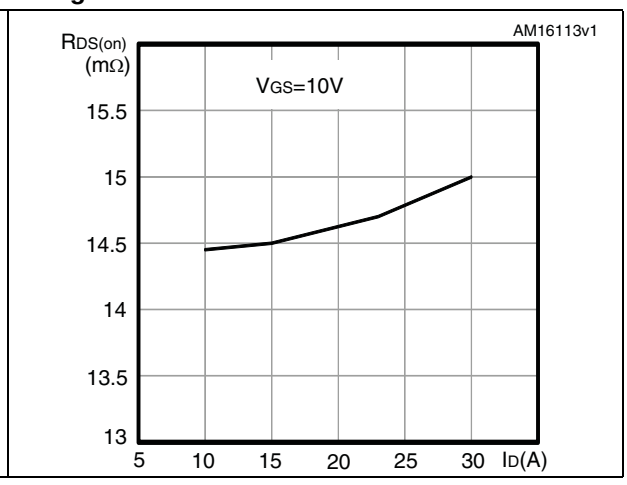


Figure 8. Capacitance variations

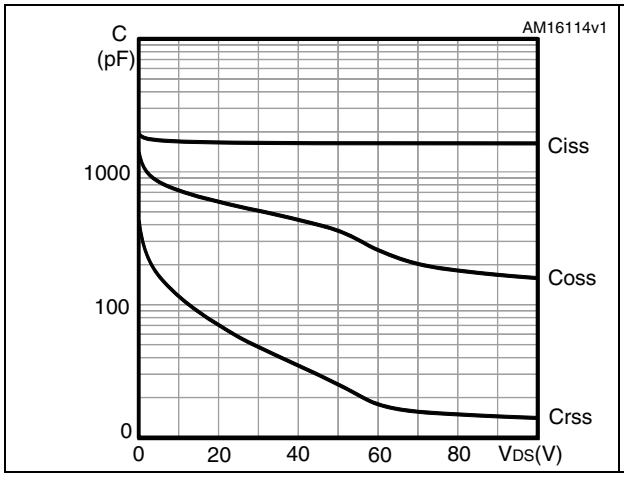


Figure 9. Normalized gate threshold voltage vs temperature

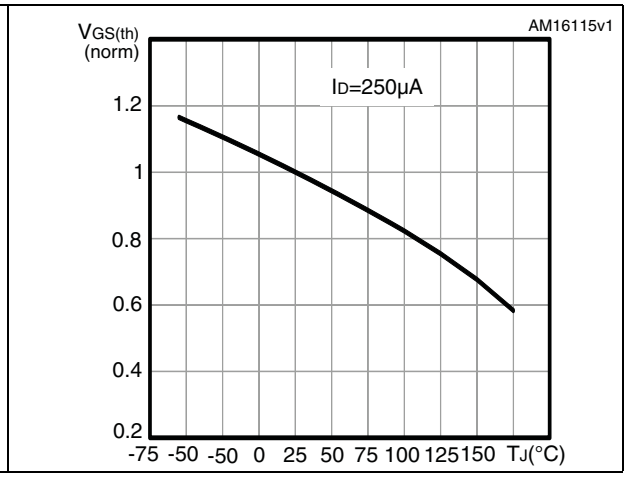


Figure 10. Normalized on-resistance vs temperature

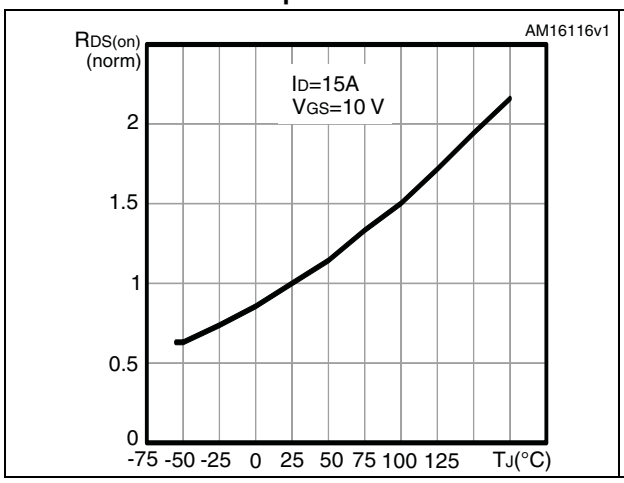


Figure 11. Normalized $V_{(BR)DS}$ vs temperature

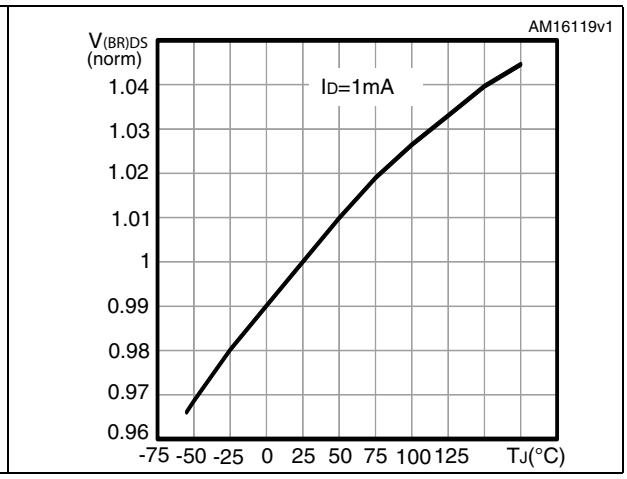
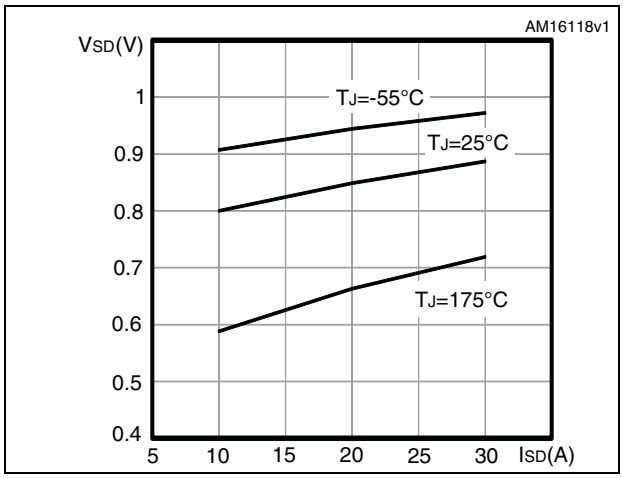


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load

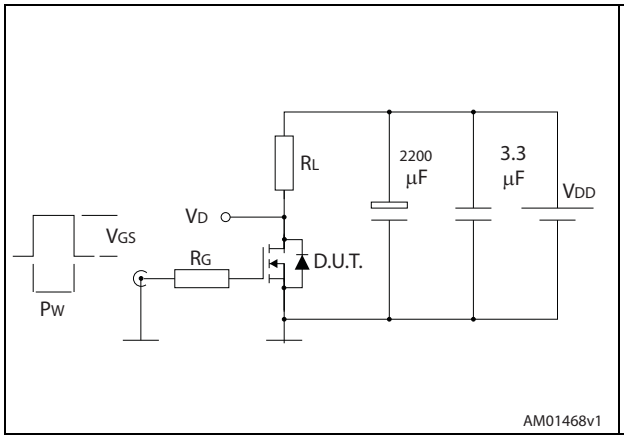


Figure 14. Gate charge test circuit

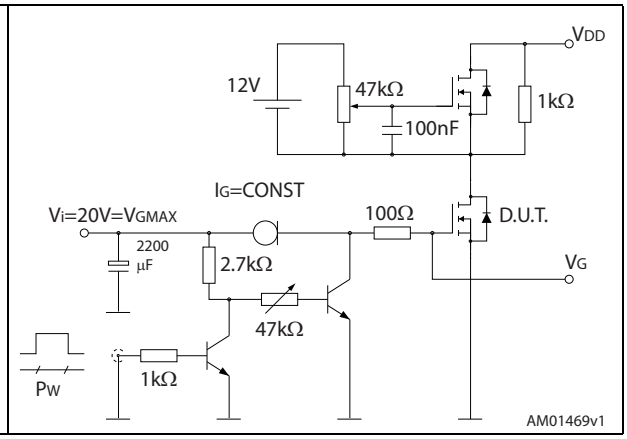


Figure 15. Test circuit for inductive load switching and diode recovery times

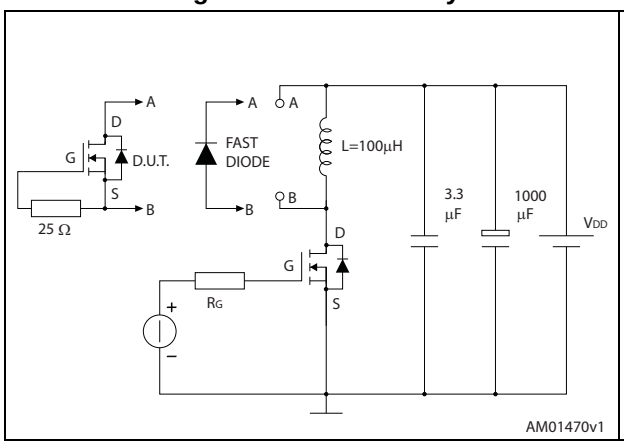


Figure 16. Unclamped inductive load test circuit

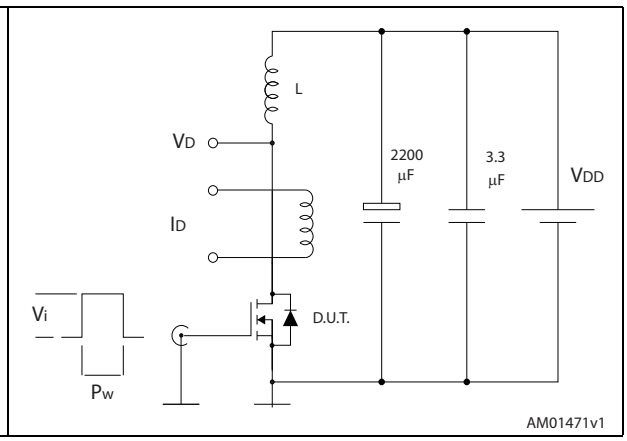


Figure 17. Unclamped inductive waveform

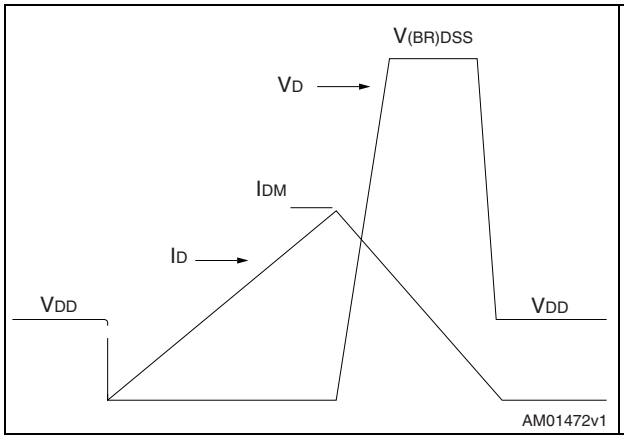
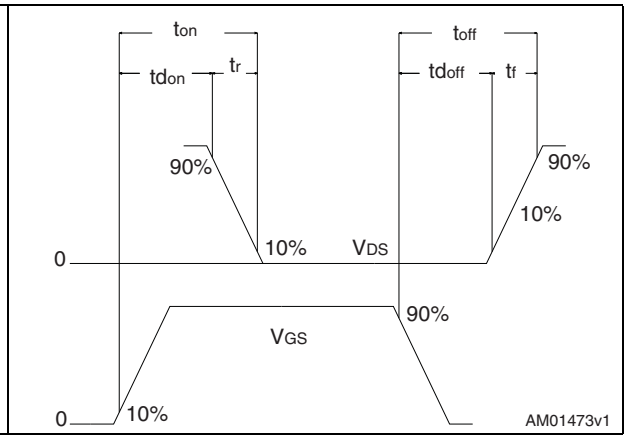


Figure 18. Switching time waveform



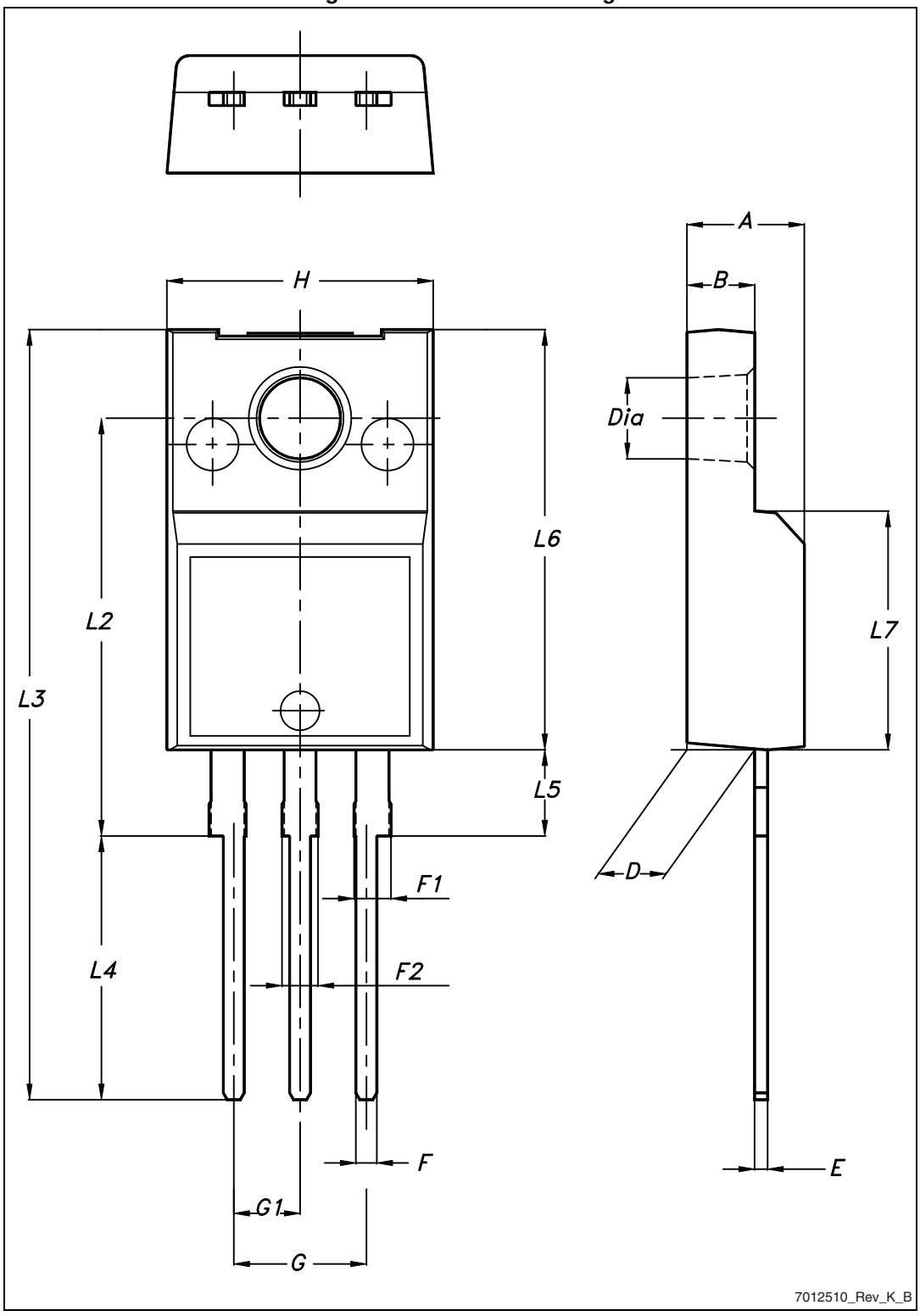
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK® is an ST trademark.

Table 8. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

Figure 19. TO-220FP drawing



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
03-Dec-2012	1	First release.
06-Dec-2012	2	Minor text changes The part number STH110N10F7-2 has been moved to a separate datasheet The part number STP110N10F7 has been moved to a separate datasheet
11-Nov-2013	3	Document status promoted from preliminary to production data.

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